QUANTUM WELL DIODE FREQUENCY MULTIPLIER STUDY

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Abstract

Quantum well devices which show negative resistance in the I-V characteristic offer very strong nonlinearity for efficient frequency harmonics generation. Furthermore, the structure can be tailored to eliminate unwanted harmonics and optimize higher harmonics in the same device. The Wafer uniformity is a key issue when making an array and requires more study.

Quantum Well Diode Odd Harmonic Frequency Multipliers

The varactor diode multiplier is extensively used for generating power at millimeter-wave frequencies, and it has been shown theoretically to be quite efficient in doubler to quintupler configurations [1]. However, the theoretical calculations assume that the input and output impedances are matched and that optimum reactive loads at all idler frequencies are realized, a requirement which in practical cases is not possible to implement fully due to a number of limitations. Thus, measured efficiencies are often considerably smaller than those theoretically estimated [1]. By using a device with a symmetrical current-voltage and/or capacitance-voltage characteristic, only odd harmonics are generated. Thus, for example, using such a device in a quintupler configuration, there is only one idler at the third harmonic to consider. This can be compared to the three idlers needed in a Schottky varactor quintupler.

The presence of a peak and valley in the I-V curve combined with the overall antisymmetry of the I-V curve about the origin [i.e., I(V) = -I(-V)], offers the potential for efficient odd-harmonic generation with an unbiased quantum well diode [2]. The key lies in pumping the diode so that the peak amplitude of the voltage across the diode occurs above the resonant current peak. This will produce, at least, three local maxima to occur in the diode current waveform over one cycle, corresponding to third or higher odd harmonic generation. The quantum well resonant tunneling multiplier has two distinct advantages over existing resistive multipliers, which are usually based on Schottky barrier diodes. First, the symmetrical response provides the potential for efficient odd harmonic frequency multiplication with an unbiased resonant-tunneling diode due to cancellation of the even harmonics, therefore greatly simplifying the circuit design. Second, the maximum harmonic generation efficiency of a quantum well device is significantly higher than the $1/n^2$ (n is the harmonic number) value that applies to standard resistive multipliers because of its negative resistance [3] (i.e., nonmonotonically increasing function I-V characteristic).

To demonstrate the feasibility of this analysis, Fig. 1 shows the polynomial I-V curve ($I = aV + bV^3 + cV^5$) which is used in the large-signal multiplier study [4,5]. It should be mentioned that the large-signal multiplier analysis has been performed under the zero-bias condition to preserve the symmetrical polarity characteristic of the I-V curve. A constant capacitance was assumed in the computation to ensure that the diode is operating in the purely varistor mode. The delivered power values at the third and fifth harmonic frequencies have been plotted versus frequency as can be seen in Figs. 2 and 3, respectively. The embedding impedances at the fundamental and third harmonic frequencies are optimized for each frequency case. The tripling and quintupling efficiencies corresponding to these power relations are shown in Figs. 4 and 5 to facilitate the comparison. Based upon these results, it is seen that the output power decreases dramatically with increasing frequency for both cases. Harmonic conversion efficiency, therefore, decreases significantly as frequency increases. As also can be seen from these

plots, the maximum tripling efficiency is actually very close to the maximum quintupling efficiency. This illustrates that the cut-off frequency of negative resistance diode frequency multipliers is not determined by the $1/n^2$ (n is the output harmonic number) limitation as for the standard positive resistance varistor diode. It can also be seen that the highest efficiency has been obtained in the negative conductance region of the device.

Power and Stability Considerations

Biasing in the Negative Differential Resistance Region

As discussed in previous publications [6,7], the diode-grid array approach is attractive because a grid is monolithically integrated with thousands of solid state diodes thereby overcoming the power limitations of a single diode multiplier since the power is distributed among the many diodes making possible watt-level CW output power throughout the millimeter-wave region. However, the pumping power for a diode grid is significantly higher than that for a single diode (proportional to the number of the diodes). Therefore, it is important to minimize the amount of input power required to pump each individual diode. In order to efficiently utilize the symmetrical I-V characteristic of a quantum well multiplier, one needs to pump the diode sufficiently hard so that the peak amplitude of the voltage across the diode occurs above the resonant current peak. This means an input power higher than 10 mW for each diode which, most likely, is too high for the diode grid concept as thousands of diodes are integrated and need to be pumped at the same time. The major thrust of this section is to investigate the possibility of minimizing the amount of power required to efficiently pump each individual diode without losing multiplication capability. For example, the almost symmetrical characteristic of the quantum well diode at the center of the negative resistance region can also be used in odd harmonic mode multiplication. This arrangement requires a dc bias. However, highly

efficient frequency multiplication can be achieved with relatively small pumping power for each diode.

To study the possibility of biasing the diode to minimize the pumping power level, the I-V curve of a quantum well diode is modelled with a fifth order polynomial (Fig. 6). The efficiency for a quantum well tripler to 100 GHz, using the I-V curve shown in Fig. 6, was calculated. The calculations are made using a large-signal nonlinear circuit analysis program for multipliers. The curves are calculated assuming a 1.5 ohm series resistance and a constant capacitance of 10 fF. By pumping the unbiased quantum well diode using a sinusoidal signal (peak voltage of 3.0 V), the tripling efficiency of the diode was analyzed as a function of pumping voltage as shown in Fig. 7. Maximum tripling efficiency can be obtained when the diode is pumped with a high power level of close to 10 mW (V_p = 2.0 V). The same calculation has been performed for the doubling efficiency which is always very close to zero. It can be seen from this result that the even harmonics are cancelled and reduced at the symmetrical I-V point along the I-V curve.

As can be seen from Fig. 8, the almost symmetrical characteristic of the quantum well diode near the center of the negative resistance region provides highly efficient odd harmonic mode multiplication. The tripling efficiency drops quickly as the dc bias point moves away from the center of the negative resistance region. In addition, the power required to achieve the maximum tripling efficiency reduces to 5 mW (V_p = 1.414 V) for each diode.

Biasing in the Positive Differential Resistance Region

The difficulty of operating in the negative differential resistance region can be seen from the stability consideration. However, if one biases the device in the positive differential resistance region, the conditions are considerably relaxed. The positive differential resistance can be utilized to relax the stringent requirements.

As can be seen from the results shown in Fig. 9, if the diode is biased in the positive differential resistance region close to the resonant current peak, the diode can be easily driven into the negative differential resistance region to achieve a high multiplication efficiency of 20%. This arrangement minimizes the required pumping power and relaxes the stringent requirements on the stability consideration. However, the tripling efficiency is lower than can be expected from biasing the device near the center of the negative differential resistance region. The doubling efficiency which can be obtained from this operation is also calculated and shown in Fig. 10. A maximum doubling efficiency of 30% can be achieved which is slightly higher than the maximum tripling efficiency from the same operation. This efficient doubling operation can be explained by the symmetrical behavior of the I-V characteristic at the peak resonant current region.

Another biasing possibility for utilizing the positive differential resistance region to relax the stability condition is to operate around the voltage region right above the occurrence of the valley current. The tripling efficiency of the quantum well diode multiplier has been calculated assuming a DC bias value of 2.2 V and is shown in Fig. 11. The maximum tripling efficiency of this operation is much lower than the above mentioned biasing cases due to the high dc current conduction and power dissipation (see Fig. 6). The positive varistor mode dominates in this bias region which can also be seen from the point that the maximum tripling efficiency is actually limited to 11% (i.e., $1/n^2$, n = output harmonic number).

Summary

The shape of the I-V curve suggests that there should be large harmonic content to the current waveform, and the antisymmetry implies that only odd harmonics should be present. From the large-signal nonlinear circuit results, the differential negative resistance allows efficiencies greater than the limit $1/n^2$ for monotonically increasing I-V curves. In conclusion, the Q factor (f_c/f_o) is the major parameter on determining the multiplication

efficiency of a quantum well diode. It is clear that the multiplication performance of a negative resistance quantum well diode is determined by the capacitance, series resistance and negative differential resistance at the operating point. However, detailed studies need to be conducted to obtain a better understanding of this phenomenon.

Power and stability considerations have been carried out for the quantum well diode multiplier application. Highly efficient odd harmonic generation can be obtained when operating a quantum well diode at the origin and the center of the negative resistance region. The power requirement for operating at the origin and the stability consideration for operating in the negative resistance region suggest the alternative choice of biasing the diode at the positive resistance region. This arrangement requires less pumping power and relaxes the stability condition; however, the odd harmonic generation efficiency is reduced due to the loss of the symmetry characteristic.

References

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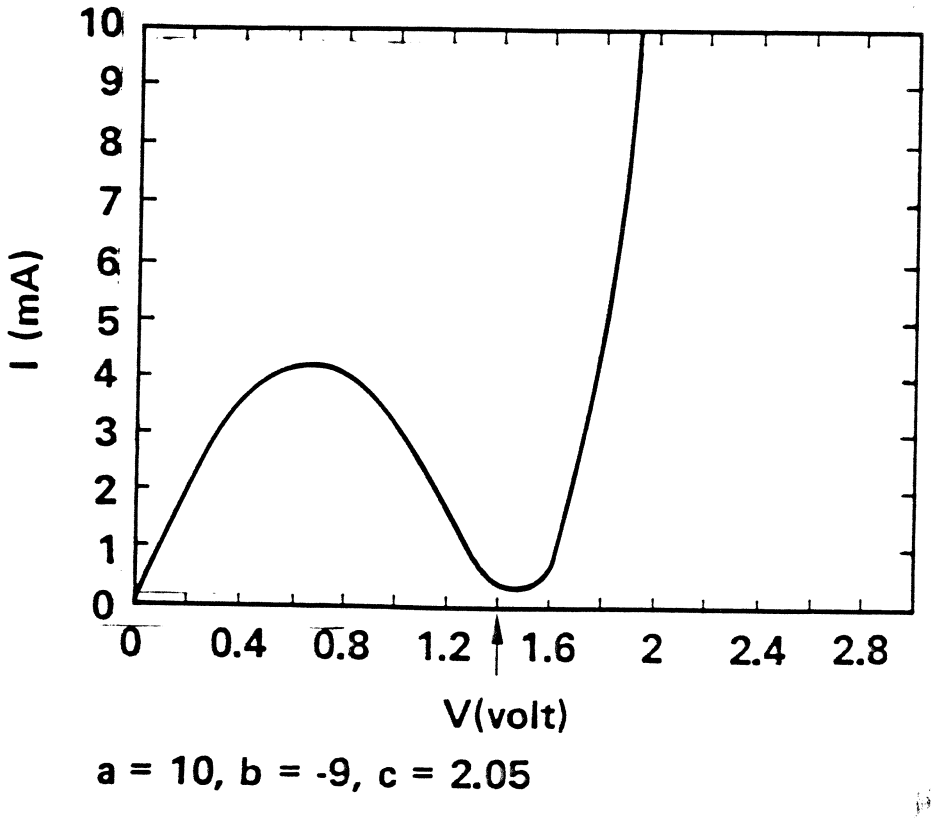

Fig. 1 The polynomial I-V curve used in the initial large-signal negative resistance quantum well diode multiplier study.

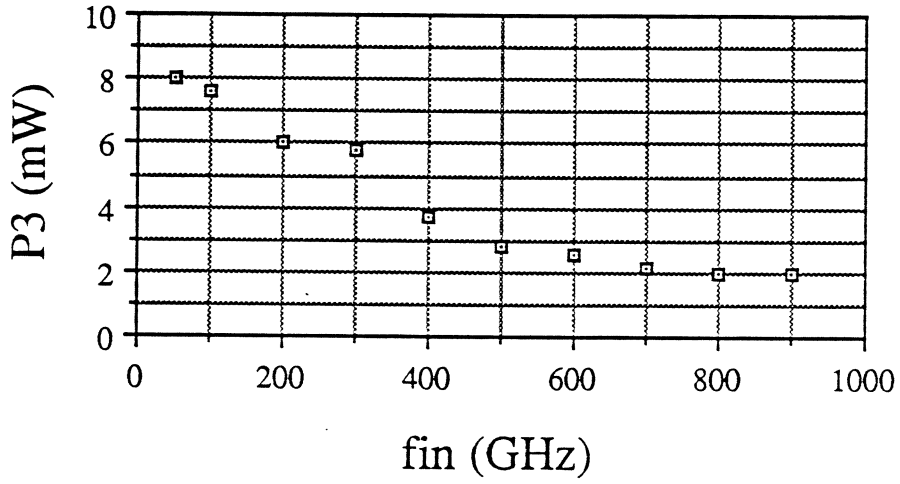

Fig. 2 Delivered power versus frequency for quantum well tripler.

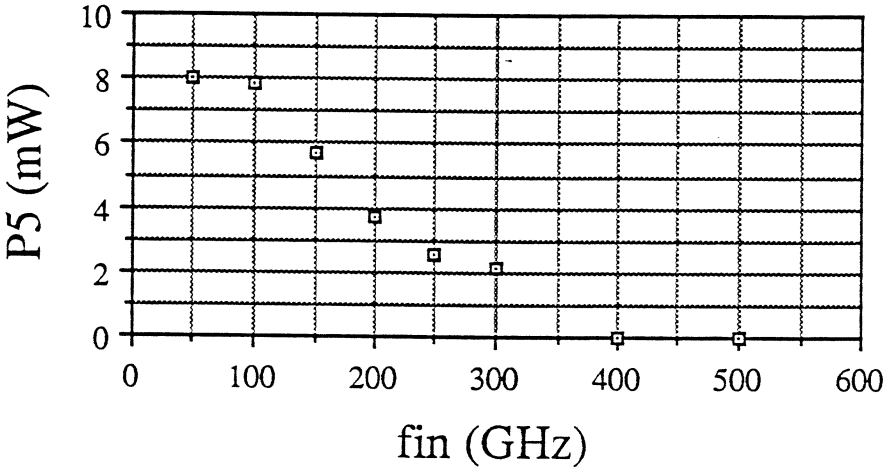

Fig. 3 Delivered power versus frequency for quantum well quintupler.

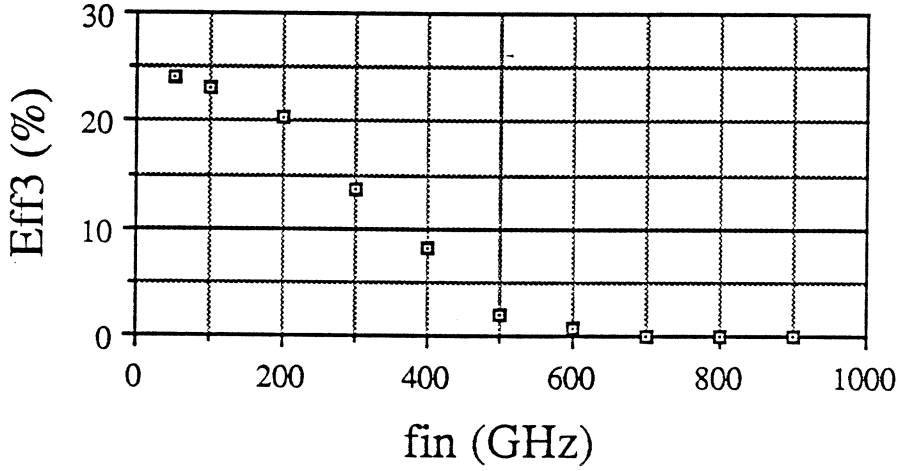

Fig. 4 Tripling efficiency versus frequency corresponding to the power shown in Fig. 7.2.

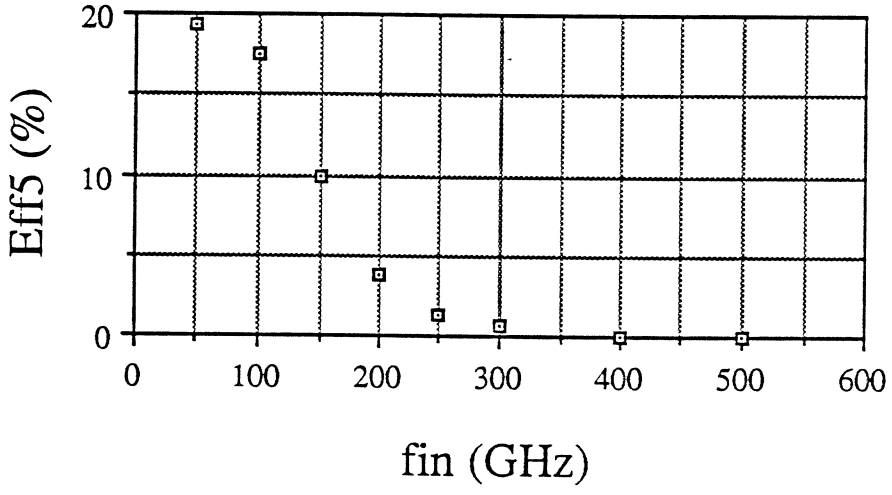

Fig. 5 Quintupling efficiency versus frequency corresponding to the power shown in Fig. 7.3.

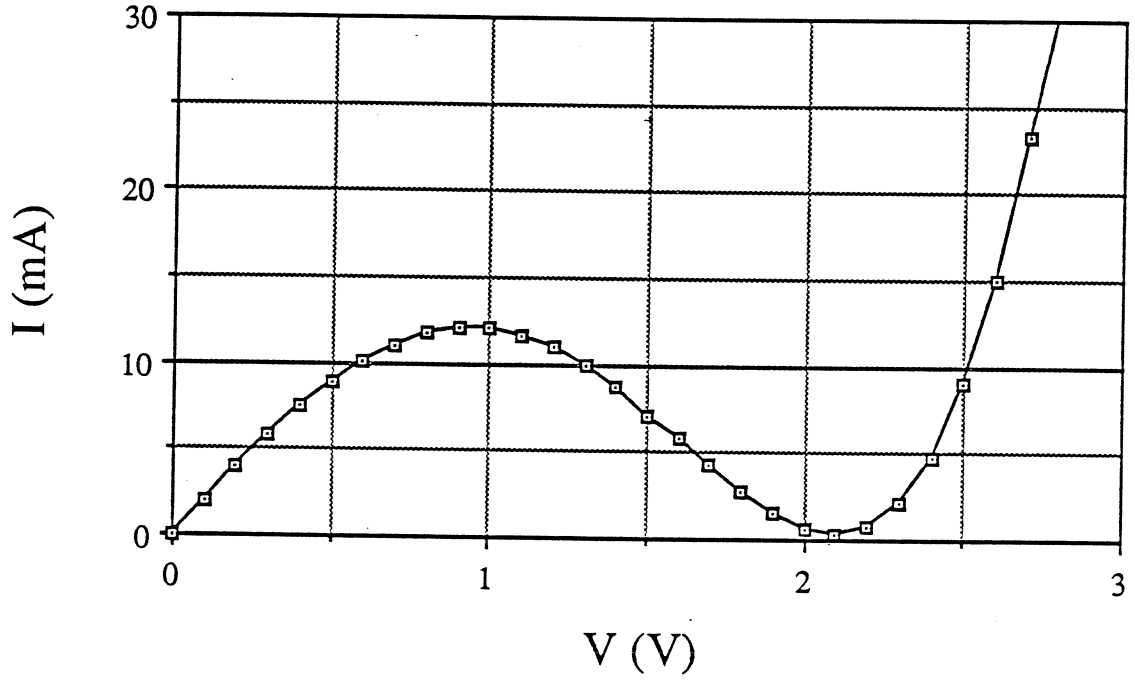

Fig. 6 The polynomial I-V curve used for the following large-signal nonlinear circuit analysis.

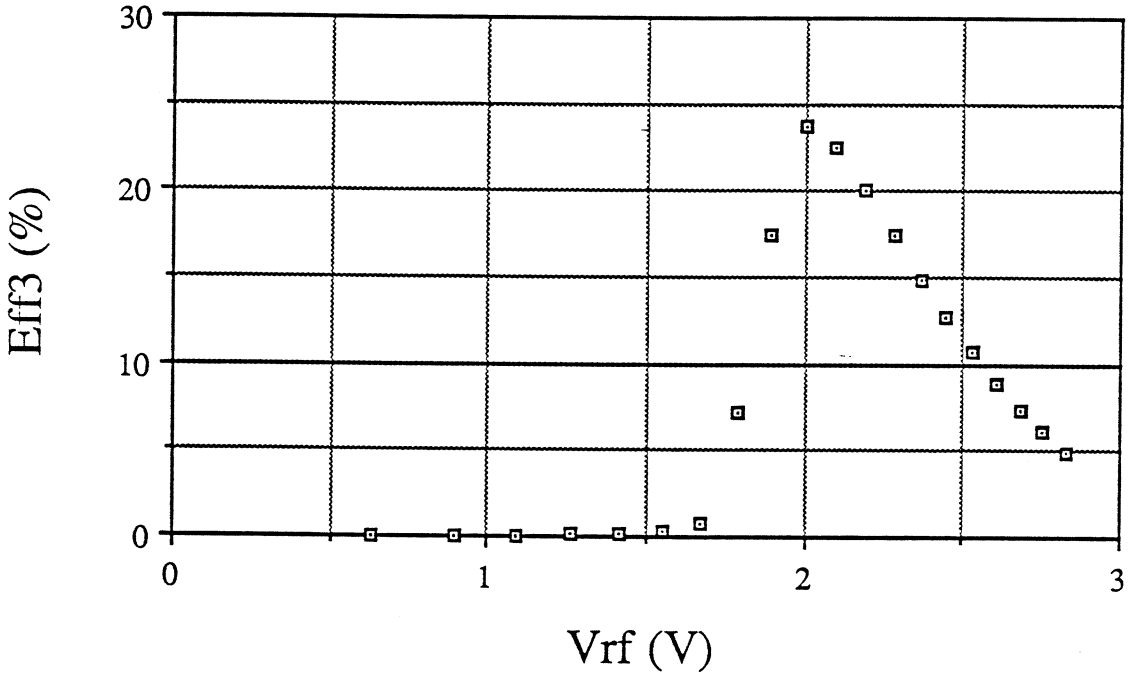

Fig. 7 Tripling efficiency versus RF voltage for the quantum well diode with zero DC bias.

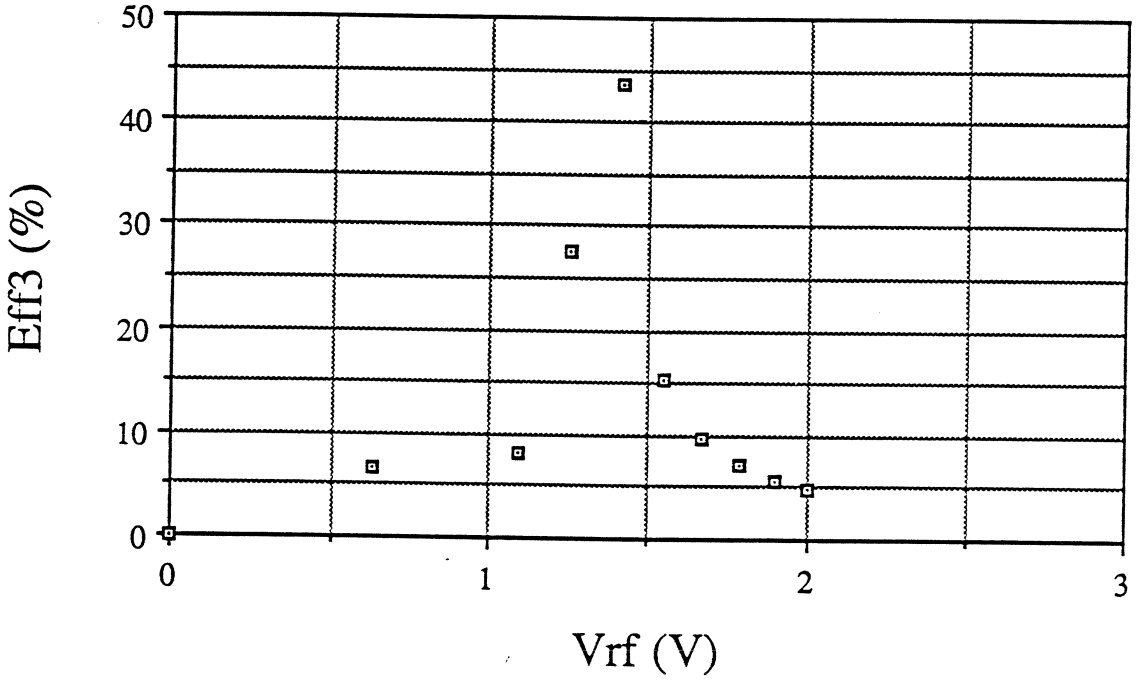

Fig. 8 Tripling efficiency versus input power for the quantum well diode biased at 1.5 V.

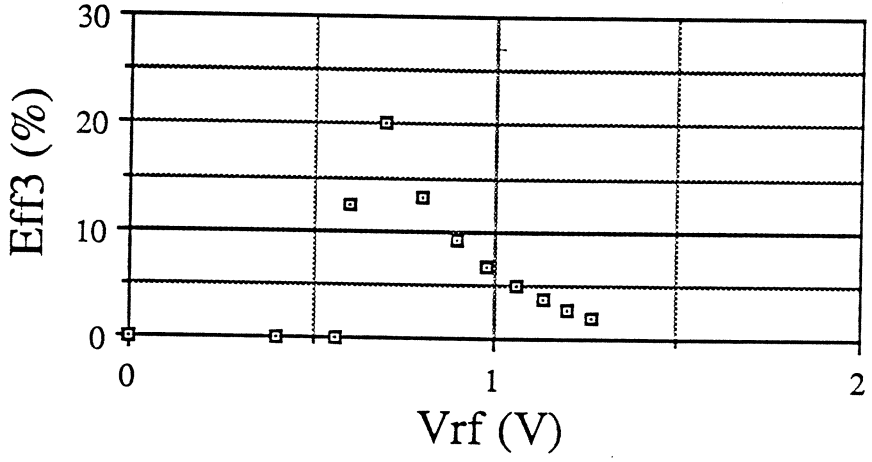

Fig. 9 Tripling efficiency versus input power for the quantum well diode biased at 0.8 V.

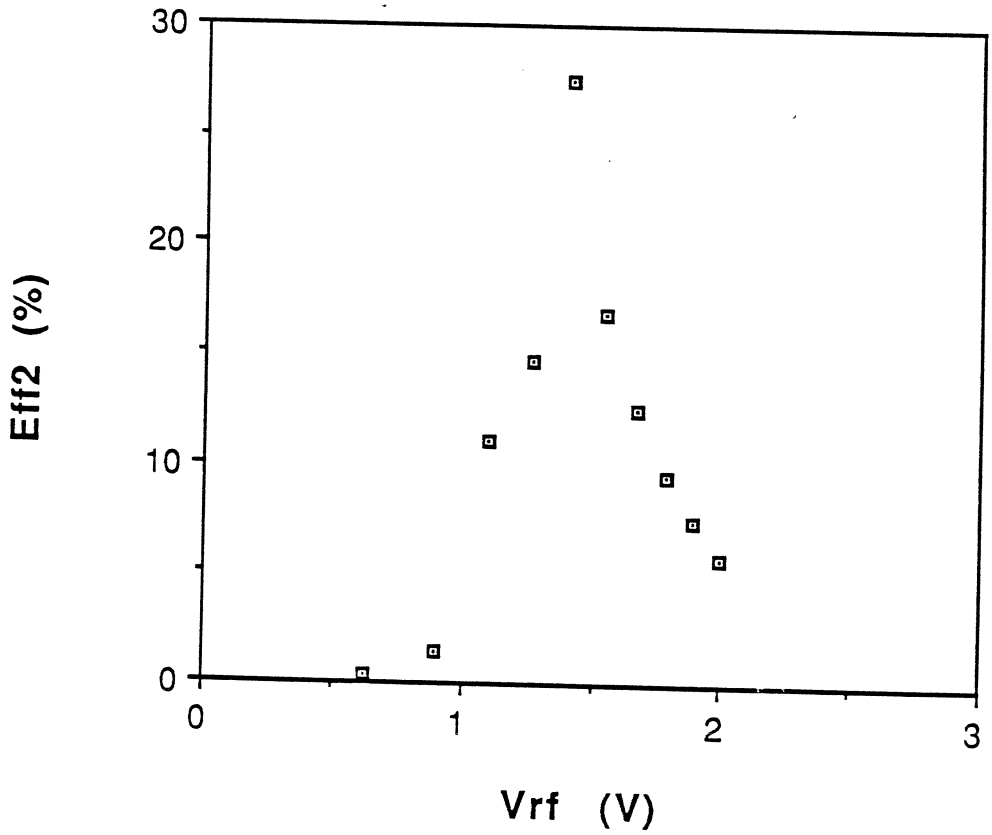

Fig. 10 Doubling efficiency versus input power for the quantum well diode biased at 0.8 V.

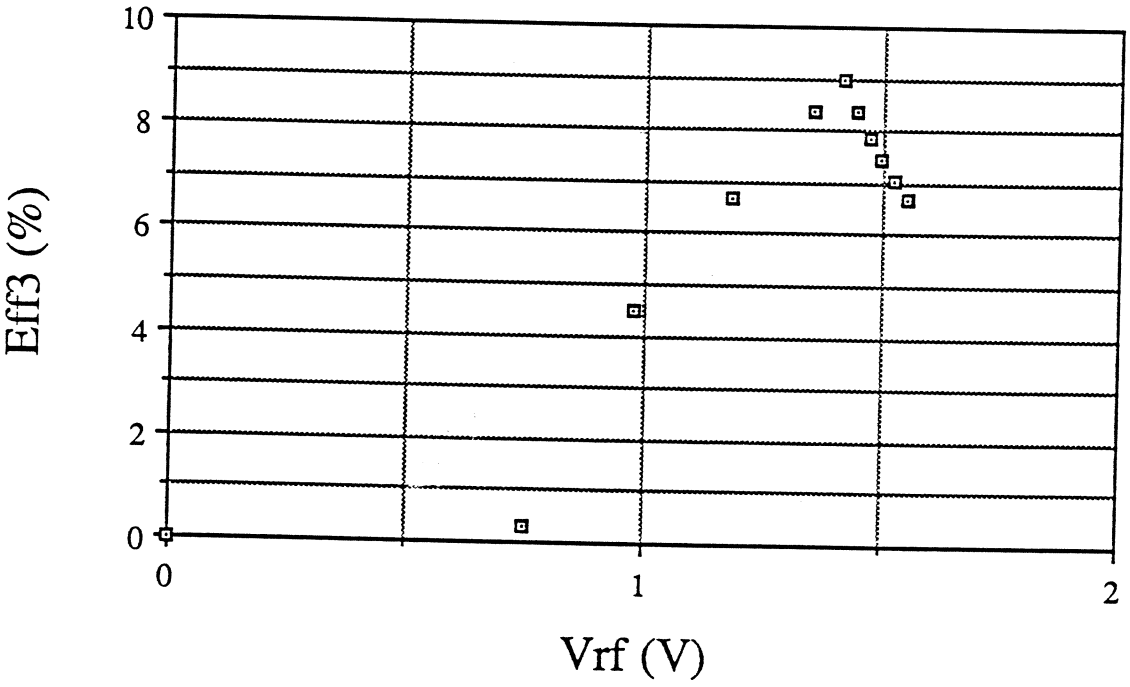

Fig. 11 Tripling efficiency versus input power for the quantum well diode biased at 2.2 V.