InGaAs/InP HETEROEPITAXIAL SCHOTTKY BARRIER DIODES FOR TERAHERTZ APPLICATIONS

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ABSTRACT

This paper explores the feasibility of planar, sub-harmonically pumped, anti-parallel InGaAs/InP heteroepitaxial Schottky diodes for terahertz applications. We present calculations of the (I-V) characteristics of such diodes using a numerical model that considers tunneling. We also present noise and conversion loss predictions of diode mixers operated at 500 GHz, and obtained from a multi-port mixer analysis, using the I-V characteristics predicted by our model.

Our calculations indicate that InGaAs/InP heteroepitaxial Schottky barrier diodes are expected to have an I-V characteristic with an ideality factor comparable to that of GaAs Schottky diodes. However, the reverse saturation current of InGaAs/InP diodes is expected to be much greater than that of GaAs diodes. These predictions are confirmed by experiment. The mixer analyses predict that sub-harmonically pumped anti-parallel InGaAs/InP diode mixers are expected to offer a 2 dB greater conversion loss and a somewhat higher single sideband noise temperature than their GaAs counterparts. More importantly, the InGaAs/InP devices are predicted to require only one-tenth of the local oscillator power required by similar GaAs diodes.

This work has been supported by the National Science Foundation under Grant ECS-9113123 and by NASA through the University of Michigan under Grant Z-25251.

I. Introduction

GaAs Schottky diodes are frequently used as mixer elements in heterodyne receivers for the few hundred gigahertz to few terahertz frequency range [1]. At present a major limitation on these devices for space-based applications is the difficulty in obtaining sufficient local oscillator (LO) power from solid state sources; the maximum available LO power decreases sharply with increasing LO frequency. One approach to overcoming this limitation is to use sub-harmonically pumped, anti-parallel diode pairs, which halves the frequency at which the LO power is needed to a range where obtaining sufficient LO power is less of an obstacle. Standard GaAs Schottky diodes have a large turn-on voltage, and consequently require a substantial applied bias to minimize LO power requirements and conversion loss. Unfortunately, it is not feasible for each diode to be biased individually in an anti-parallel configuration. To reduce the LO power requirement, InGaAs has been proposed as a material for use in sub-harmonically pumped, anti-parallel diode structures [2]. Schottky barriers formed from InGaAs have a height that decreases with increasing indium mole fraction. The resulting lower turn-on voltage of these diodes suggests that they will require smaller LO voltages, and therefore power, for optimum performance. An added benefit of using InGaAs instead of GaAs is its superior mobility, which will lead to a lower series resistance, which in turn will reduce the conversion loss.

Of crucial importance to both the conversion loss and noise of the mixer is the diode I-V characteristic. We have previously reported on a Schottky diode current-voltage analysis that considers electron tunneling and image force lowering [2]. In diodes with epitaxial layers doped to greater than about 5.0×10^{16} cm^{-3}, electron tunneling significantly affects the diode ideality factor.

We present the results of conversion loss and mixer noise calculations using the I-V characteristics obtained from our diode model. A single diode equivalent circuit was used to model diode mixers in the sub-harmonically pumped, anti-parallel configuration. We have used a computer program by P. Seigel to perform the analysis [3], which we have modified to use the current-voltage model discussed in this paper, rather than the standard thermionic-emission model.

We also discuss fabrication technology currently being developed for a planar, anti-parallel InGaAs/InP diode.

II. Diode Model

A. Anti-Parallel Planar Diodes

An electron micrograph of a GaAs anti-parallel planar diode is shown in Figure 1 [1]. The $In_{0.5}Ga_{0.5}As$/InP anti-parallel planar diodes being designed in this study will have an identical geometry. A cross-section of such a diode is shown in Figure 2. A circuit model of a planar diode showing the major parasitics is shown in Figure 3. The junction capacitance, C_j, and the series resistance, R_s, are the dominant parasitics at high frequencies, and should be minimized for optimum conversion performance. The effects of the pad-to-pad capacitance, C_{pp}, and the finger inductance, L_s, are smaller, and have not been considered in the mixer calculations presented in this paper. Furthermore, the junction conductance itself may deviate from ideal exponential behavior, particularly at high forward or reverse bias, and this can also affect the conversion performance. This effect is considered in the Schottky I-V analysis presented in this paper.

The series resistance of a Schottky diode can be reduced by increasing the conductivity of the epitaxial layer and/or the substrate, or by reducing the thickness of the undepleted epitaxial layer. The epilayer conductivity can be increased by increasing its doping concentration, however, this involves a trade-off: the diode ideality is also decreased. The use of InGaAs, which has a greater electron mobility than GaAs, allows for a high conductivity epilayer, and avoids this trade-off, as we shall show later. In addition, the epilayer in InGaAs diodes can be made much thinner than in GaAs diodes. This is because the epilayer is generally made slightly thicker than the zero-biased depletion depth, which is proportional to the square root of the Schottky barrier height. Therefore, in equally doped material, the zero-biased depletion depth in $In_{0.53}Ga_{0.47}As$ is about half that in GaAs.

The zero-biased junction capacitance of InGaAs diodes is greater than that of comparable GaAs diodes because the junction capacitance is, to first order, inversely proportional to the depletion depth. However, at the current densities reached in normal operation, the typical junction capacitances of the diodes are expected to be comparable. This is because the depletion depth depends on the remaining barrier, that is, the Schottky barrier height minus the applied voltage, and the current density is roughly proportional to the exponential of the remaining barrier.

B. Schottky I-V Model

We shall briefly outline the quantum-mechanical transmission current-voltage model, which is described in greater detail elsewhere [4], and is largely based on the work of Chang, Crowell, and Sze [5,6].

The current density is calculated through a numerical evaluation of the equation

$$J(V) = \frac{RT}{k} \int_{E_{min}}^{\infty} dE_n \left[\tau(E_n, V) \left[F_s(E_n, V) - F_m(E_n) \right] \right] \quad (1)$$

where R is the Richardson constant in the semiconductor, T is the temperature, k is Boltzmann's constant, τ is the electron transmission coefficient, F_s and F_m are the semiconductor and metal distribution functions respectively, V is the applied bias, E_n is the component of the incident electron energy normal to the metal, and E_{min} is the minimum allowed electron energy. E_{min} corresponds to the conduction band minimum in the metal or the semiconductor, depending on the applied bias.

The electron transmission coefficient is obtained through a one dimensional solution of Schrodinger's equation covering the region of the Schottky barrier, including the effects of image force lowering. The transmission coefficient has been shown to vary sharply with the electron energy, and ranges from near zero for electrons with energies much below the barrier maximum, to near unity for electrons with energies a few kT greater than the barrier maximum [4].

We have used a drifted-Maxwellian to model the electron energy distribution, which is given by [7]

$$F = \frac{m^{*1/2}}{(2\pi kT)^{1/2}} \exp\left[\frac{-m^*(v_n - v_d)^2}{2kT} \right], \quad (2)$$

where v_n is the normal component of electron velocity, and v_d is the drift velocity, defined as

$$v_d = \frac{J}{qN_d^+}, \quad (3)$$

where N_d^+ is the concentration of the ionized donors in the epitaxial layer outside the depletion region. The current density and drift velocity are calculated iteratively using (1-3) until they

converge to the desired level of accuracy.

C. I-V Predictions

Figures 4 and 5a-b show the I-V characteristics of the metal-semiconductor junctions (denoted by V_j) of GaAs and $In_{0.5}Ga_{0.5}As$ diodes respectively, as predicted by the algorithm discussed in Section B. V_j. Table 1 shows the diode parameters used. The reverse current in a $In_{0.5}Ga_{0.5}As$ diode is predicted to be several orders of magnitude greater than in a GaAs diode. However, it is still nearly two orders of magnitude smaller than the maximum forward current. Thus, while the reverse current is not negligible, it is not expected to degrade mixer performance drastically, as we shall demonstrate in the next section of this paper. It is also noteworthy that the voltage-dependent ideality factors of the two diodes at a forward current density of 10^4 A/cm^2 (which corresponds to a current of 0.08 mA in a 1 μm diameter diode) are nearly identical.

Figures 5a-b also show the overall I-V characteristic of a whisker-contacted $In_{0.5}Ga_{0.5}As$/InP diode fabricated in our laboratory, and includes the effects of the series resistance. These whisker-contacted diodes are research devices only, and will be superseded by planar devices. The data agree well with our model, in which the only adjustable parameter is the Schottky barrier height.

III. Mixer Analysis

The conversion loss and noise calculations presented in this paper have used the multiple reflection algorithm developed by Held and Kerr [8]. A FORTRAN language computer program by P. Seigel, known as GISSMIX [3], (with a few modifications) was used to perform the

calculations. The modifications to the program include the use of the I-V model described above, instead of the thermionic emission model, as well as changes to permit the calculation of subharmonically pumped mixer performance using the single diode equivalent circuit.

A. Held and Kerr Mixer Analysis

The Held and Kerr mixer analysis is based on the assumption of a large signal LO source, upon which is superimposed a small signal RF. The time-dependent conductance of the diode is determined through a non-linear analysis. The diode waveform is then resolved into the small signal admittance, and is represented in the frequency domain through its Fourier coefficients. These coefficients are then used to calculate the noise and conversion performance of the diode mixer circuit. The analysis assumes a knowledge of the diode parameters as well as the embedding impedances at the mixing frequencies. The analysis is amply described elsewhere, and therefore we shall not outline the details of the analysis [8].

The mixer performance is in general affected by the embedding impedances presented to the diode by the mixer block at several sideband and LO harmonic frequencies. These parameters can be obtained through a characterization of the diode mount; however, our investigation has not yet progressed to that point. Due to the absence of information on the embedding impedances, we have chosen to simplify and standardize our analysis by representing all higher order mixing frequencies as short circuits. In general, the use of such an approximation will slightly underestimate the conversion loss and noise temperature. The embedding impedances we have assumed are given in Table 2.

The performance of sub-harmonically pumped, anti-parallel diodes was estimated through use of the single diode equivalent circuit [9]. In this circuit model, the odd-harmonic embedding impedance is equal to twice that presented to a single diode, and the even-harmonic embedding

impedances are set to zero.

B. Calculations

Figure 6 shows the predicted upper-sideband (USB) conversion loss of GaAs and $In_{0.5}Ga_{0.5}As$ single diode mixers at 505 GHz, as a function of the available LO power. Zero applied bias is assumed. The diode parameters used in the mixer analysis are given in Table 1. The $In_{0.5}Ga_{0.5}As$ diode will offer a minimum conversion loss of about 7 dB with P_{LO} equal to 0.2 mW, in comparison to the GaAs diode, which will offer about 8 dB conversion loss with P_{LO} equal to nearly 2 mW. The superior predicted conversion loss of the $In_{0.5}Ga_{0.5}As$ diode is due primarily to its lower series resistance, and its lower LO power requirement with zero bias is due to its lower barrier height.

Figures 7 and 8 show the predicted upper-sideband (USB) conversion loss and noise temperature respectively, of sub-harmonically pumped, anti-parallel GaAs and $In_{0.5}Ga_{0.5}As$ diodes, as a function of the available LO power per diode. The total LO power required by the diode pair is therefore twice the amount shown. An LO frequency of 250 GHz and a signal frequency of 505 GHz were assumed. The minimum conversion loss of the $In_{0.5}Ga_{0.5}As$ diode pair is predicted to be about 11 dB with 0.2 mW of total available LO power, compared to about 9 dB with about 2 mW of available LO power for the GaAs diode pair. The minimum USB noise temperatures of the $In_{0.5}Ga_{0.5}As$ and GaAs diode pairs are predicted to be about 2000 K and 1300 K respectively. Thus, $In_{0.5}Ga_{0.5}As$/InP diode anti-parallel mixers are expected to reduce the LO power requirement by at least an order of magnitude compared to that of similar GaAs diode mixers, while increasing the conversion loss and noise by no more than 2 dB and 50 percent respectively. The RF performance of $In_{0.5}Ga_{0.5}As$/InP diodes in an anti-parallel configuration is expected to be somewhat degraded from that of single diodes of the same

material and with similar parameters. We believe this is due to the relatively high reverse saturation current of these diodes. However, this drawback is small in comparison to their primary advantage: they will require LO sources at frequencies half of the signal frequency.

IV. Diode Fabrication

The objective of this facet of our work was to develop a device fabrication technology which will enable us to produce predictable planar, anti-parallel $In_{0.53}Ga_{0.47}As$ mixer diodes with reliable electrical characteristics. The fabrication procedure for planar, anti-parallel diodes on $In_{0.53}Ga_{0.47}As$ is very similar to that on GaAs. A highly abbreviated outline follows.

1. Active Layer Thinning: The active layer of $In_{0.53}Ga_{0.47}As$ was intentionally grown thicker than the theoretical zero-bias depletion thickness. This allowed us to adjust the actual epitaxial layer thickness by using an electrochemical thinning technique. The actual epilayer thickness was measured using a standard C(V) profiling technique but with a 10 MHz frequency to allow the component of current through the space-charge capacitance to be dominant. This provided us a way to optimize the I-V characteristic by changing the actual active layer thickness.

2. Oxide Deposition. A thin (6000 A) layer of SiO_2 was pyrolytically deposited on the active layer.

3. Ohmic Contact Formation. An ohmic contact was formed by electroplating Sn-Ni/Ni/Au on n^{++} $In_{0.53}Ga_{0.47}As$ and subsequently alloying at 400°C. The TLM pattern test has shown that the Sn-Ni/Ni/Au ohmic contact on $In_{0.53}Ga_{0.47}As$ is about $2–3 \times 10^{-6}$ Ωcm^2, which is one order of magnitude better than that on GaAs.

4. Anode Definition. Standard photolithography and reactive ion etching were employed to define anode windows in the SiO_2 layer. The anode metals (Pt and Au) were DC electroplated through these windows onto the underlying active $In_{0.53}Ga_{0.47}As$ layer to form the Schottky diodes.

5. Anode Contact Finger. Conductive thin films of chromium and gold were first deposited over the entire wafer through use of a sputtering system. Next, the fingers were electroplated over a photolithographically defined region. Both dry and wet etching were used to remove the thin chromium/gold film covering the wafer, leaving the contact fingers in place.

6. Surface Channel Etching. A final photolithography step defines the surface channel. Buffered hydrofluoric acid was first used to remove the SiO_2 in the surface channel. Then, the conducting $In_{0.53}Ga_{0.47}As$ between the pads was removed by using H_3PO_4 : H_2O_2 : H_2O, which provides the desired etch profile for different InGaAs crystal directions, thus allowing the finger to be undercut.

Early results of ohmic contact formation have shown a problem associated with alloying: the oxide near the anode region was damaged after alloying. This problem was solved by changing the plating parameters and the alloying temperature without changing the quality of the contact. The most crucial step in device fabrication is anode formation. Early attempts at anode formation on planar, anti-parallel $In_{0.53}Ga_{0.47}As$ resulted in a low breakdown voltage, as well as instability and nonuniformity of the I-V. These problems were overcome by optimization of the plating parameters. Profiles resulting from several chemical etchants have been investigated with respect to the desired profile in forming the surface channel, which undercuts the anode fingers and protects the anode region. The H_3PO_4 : H_2O_2 : H_2O family has been found to provide the desired results.

V. Conclusion

In this paper we have presented I-V calculations of $In_{0.5}Ga_{0.5}As$/InP Shottky barrier diodes. The model we have used considers electron tunneling, image force barrier lowering, and the effect of a drifted Maxwellian electron distribution. The model has been shown to agree well with experimental data on whisker-contacted $In_{0.5}Ga_{0.5}As$/InP and GaAs diodes fabricated in our laboratory. The I-V characteristics of $In_{0.5}Ga_{0.5}As$/InP diodes have been shown to be similar to those of GaAs diodes, but are displaced in voltage and have a higher reverse saturation current.

The I-V characteristics obtained from our model were used to predict the mixer performance of both single and sub-harmonically pumped, anti-parallel diodes. A modified form of Seigel and Kerr's analysis was used. The calculations show that in unbiased operation, $In_{0.5}Ga_{0.5}As$/InP single diode mixers will offer conversion performance equal to that of comparable GaAs diode mixers, and require only one-tenth the LO power. Furthermore, sub-harmonically pumped, anti-parallel $In_{0.5}Ga_{0.5}As$/InP diode mixers are expected to offer performance nearly as good as that of the best GaAs diode mixers, but will require one-tenth as much LO power to achieve their optimum performance.

The fabrication techniques for anti-parallel, $In_{0.5}Ga_{0.5}As$/InP planar diodes with surface channels have been extensively investigated. Difficulties in anode plating and ohmic contact formation have been resolved, and suitable chemical etchants necessary for the fabrication sequence have been found.

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Table 1. Diode parameters.

diode materials	GaAs	$In_{0.5}Ga_{0.5}As/InP$
anode diameter	0.5 μm	0.5 μm
ohmic contact width	50 μm	50 μm
ohmic contact length	50 μm	50 μm
chip thickness	125 μm	125 μm
active layer thickness	0.110 μm	0.065 μm
ϕ_B	0.950 eV	0.277 eV
active layer doping	1.5×10^{17} cm^{-3}	1.5×10^{17} cm^{-3}
buffer layer doping	2.0×10^{18} cm^{-3}	2.0×10^{18} cm^{-3}
C_{jo}	1.22 fF	2.10 fF
C_{jmax}	10.0 fF	10.0 fF
I_{sat}	7.85×10^{-17} A	8.25×10^{-7} A
I_{max}	5.0×10^{-3} A	5.0×10^{-3} A
η	1.12	1.09
R_s	15.0 Ω	9.0 Ω

Table 2. Mixer embedding impedances.

ω_{RF}	75 Ω
ω_{image}	75 Ω
ω_{LO}	50 Ω
ω_{IF}	matched

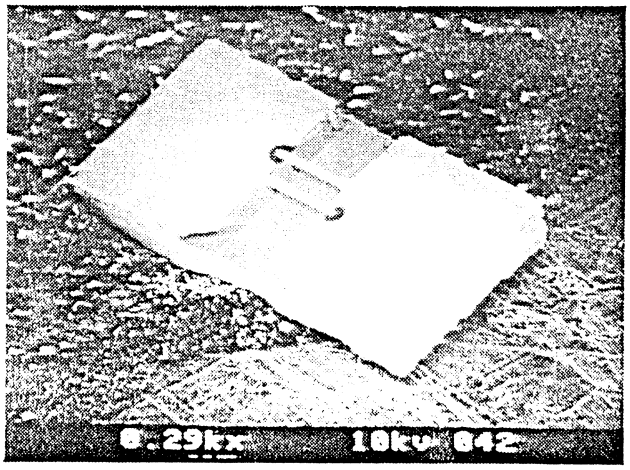

Figure 1. Electron micrograph of GaAs anti-parallel planar diode.

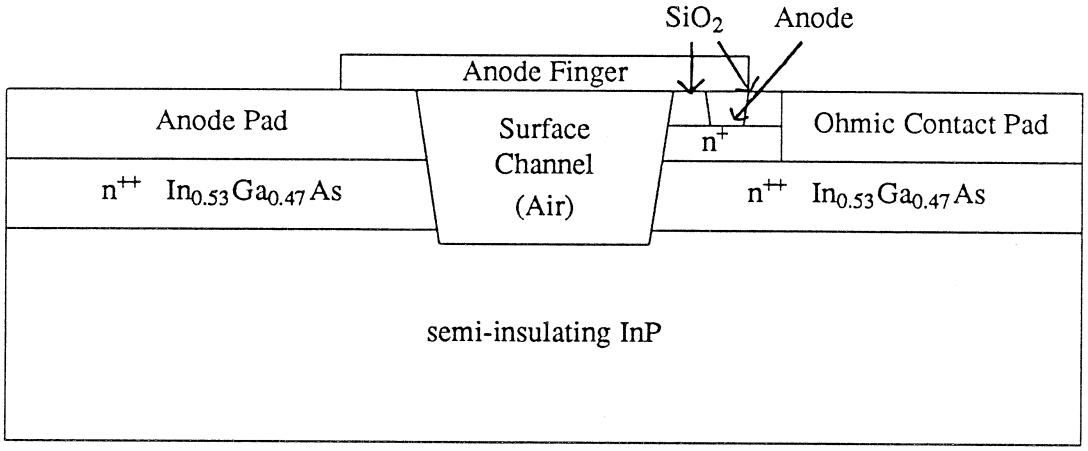

Figure 2. Cross-section of anti-parallel, planar InGaAs/InP diode (not to scale).

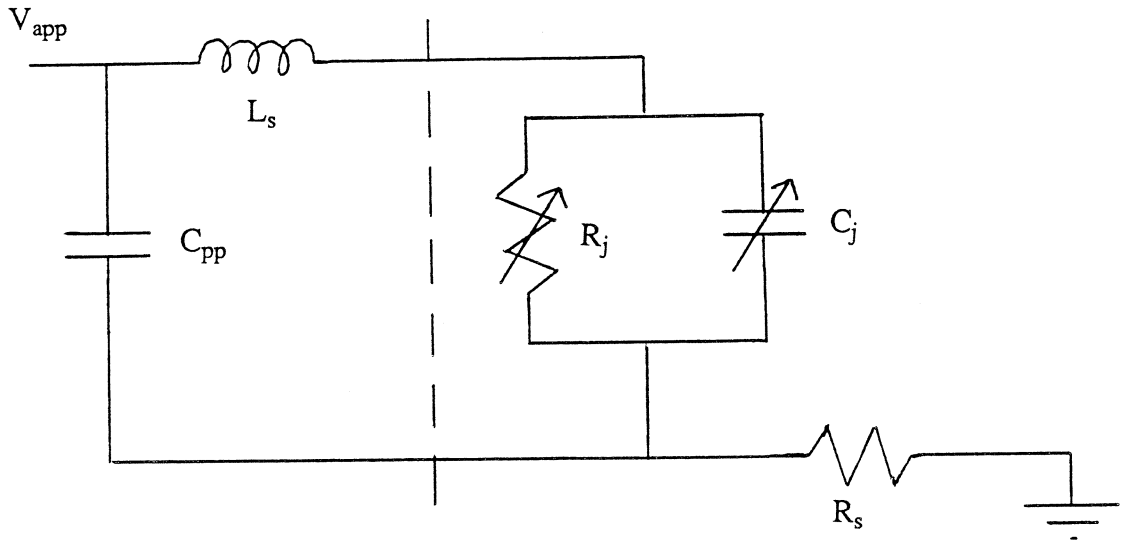

Figure 3. Circuit model of planar diode.

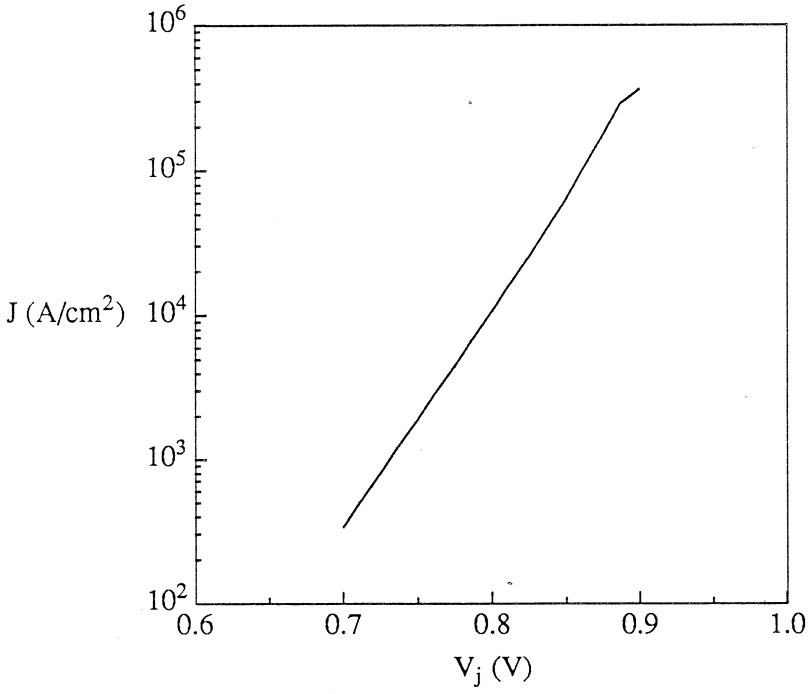

Figure 4. Forward current-voltage characteristic of GaAs Schottky diode.

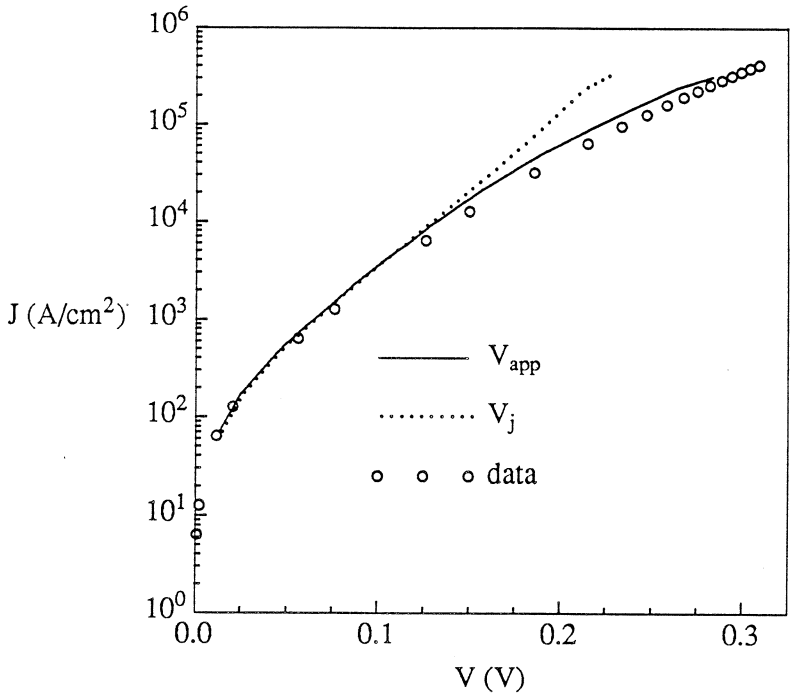

Figure 5a. Forward current-voltage characteristic of $In_{0.5}Ga_{0.5}As$/InP Schottky diode.

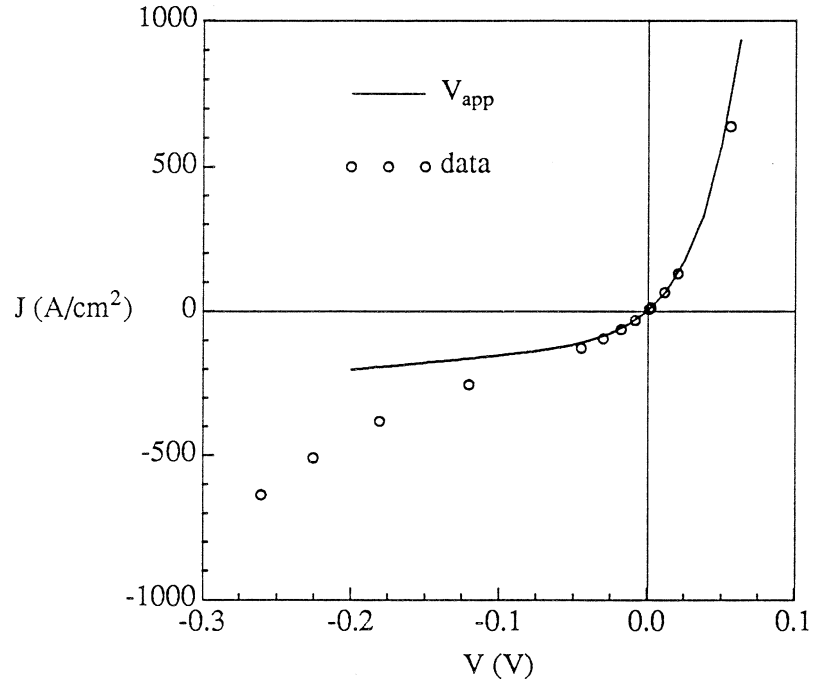

Figure 5b. Reverse current-voltage characteristic of $In_{0.5}Ga_{0.5}As$/InP Schottky diode.

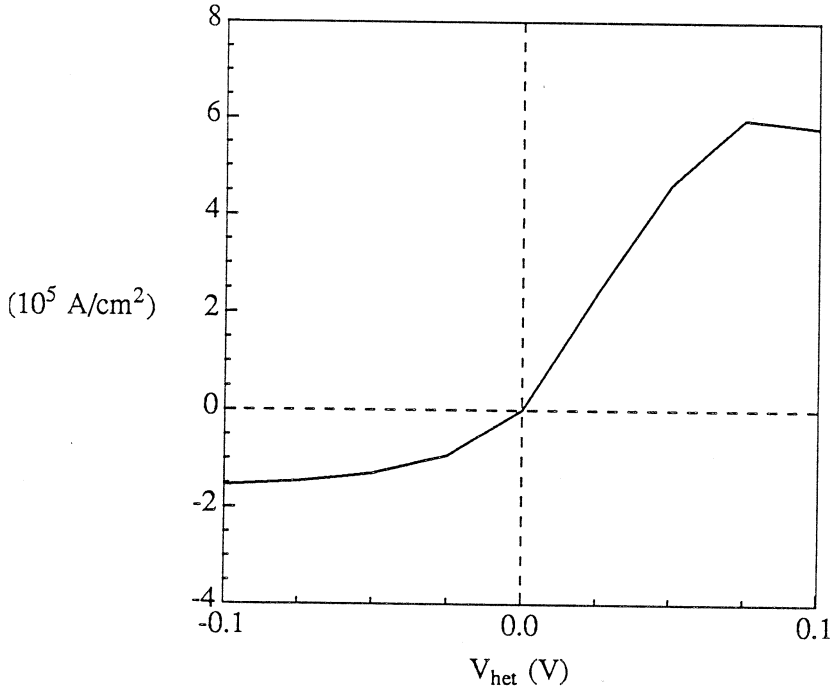

Figure 5c. Current-voltage characteristic of the heterojunction in an $In_{0.5}Ga_{0.5}As$/InP Schottky diode.

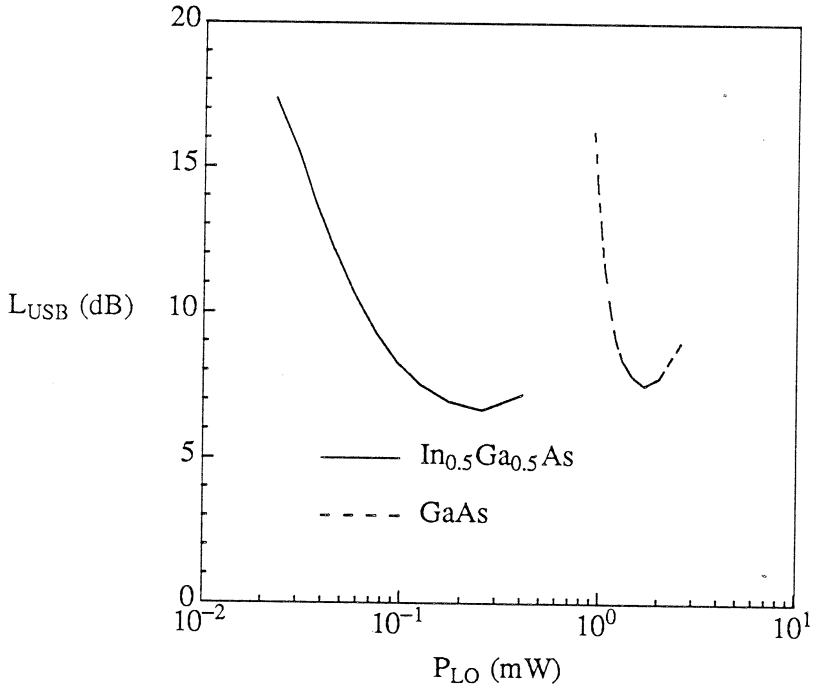

Figure 6. Conversion loss (USB) versus LO power of single Schottky diodes at 505 GHz.

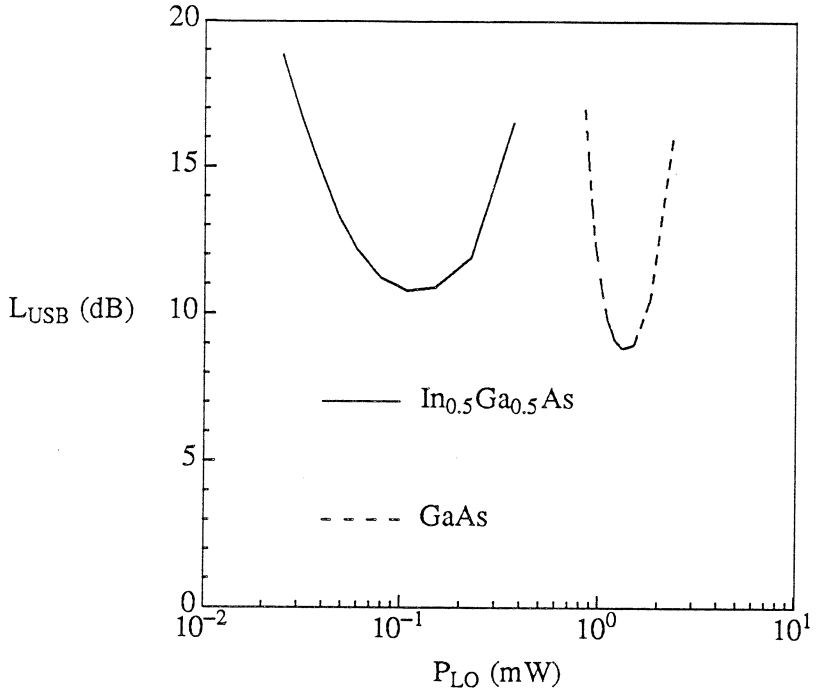

Figure 7. Conversion loss (USB) versus LO power per diode of sub-harmonically pumped, anti-parallel Schottky diodes at 505 GHz.

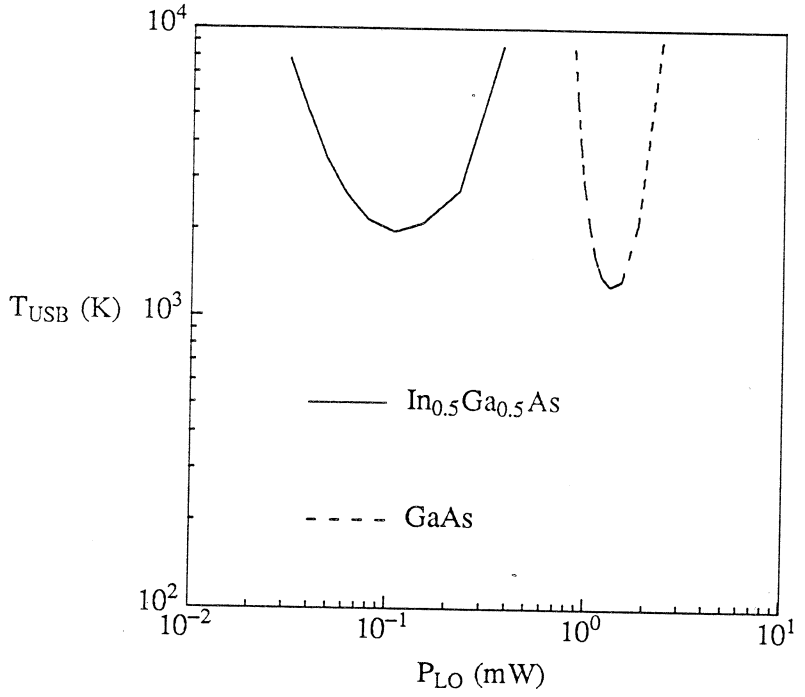

Figure 8. Noise temperature (USB) versus LO power per diode of sub-harmonically pumped, anti-parallel Schottky diodes at 505 GHz.