Implications of Area-Array I/O for Row-Based Placement Methodology

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Layout for Area-Array I/O

- Problem:

  Given a core portion of the chip which already contains the I/O buffers, place the … area-array pads on the top metal layer of the design ... and route these pads to the I/O ports of the chip. (Tan et al. 1997)

- New tool requirements
  - package/die co-simulation
  - clock/power distribution
  - new constraints for placement

Our Work

- Area-array *implications* for placement methodology
- Three-axis testbed
  - area-array vs. peripheral I/O regimes
  - alternating vs. simultaneous methodologies
  - hierarchical quadratic vs. min-cut + assignment engines
- Main observations
  - area-array I/O regime “more forgiving”...
  - … but wrong methodologies/engines entail substantial loss

Outline of Talk

- Previous work
  - area-array I/O layout
  - core and peripheral I/O placement
- Taxonomy of I/O and core placement
- Experimental questions and testbed
- Experimental results
- Conclusions and ongoing work

Area-Array I/O Layout

- Farbarik et al. 1997: CAD tool suite
  - area-pad floorplanner (assume fixed I/O-to-pad netlist)
  - gridless maze router
- Tan et al. 1997
  - search for pad locations (assume fixed core placement)
  - assignment of I/O ports to pad locations
- Kiamilev et al. 1997: three layout methodologies
  - #2: similar to Farbarik et al. w/ manual routing
  - #3: optimize core, I/O buffer placements on chip; place area pads above using *pad interface module*

Core and Peripheral I/O Placement

- Pedram et al. 1991
  - motivation: random I/O placement + alternation ineffective
  - linear assignment of I/Os based on circuit structure
  - context = quadratic placer (Ritual)
- Chen at al. 1992, Raj et al. 1997
  - improved I/O placement formulations + annealing
  - context = both quadratic, annealing placers
- Simultaneous I/O and core placement
  - e.g., augment top-down partitioner (Gao et al. 1993)

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I/O Pad Regimes

- Rectangular core layout region
- #I/O cells = #pad locations
  - uniformly spaced around core boundary (PG)
  - designer locations projected to core boundary (PU)
  - uniform array within core layout region (AA)
- Any I/O cell can be placed at any pad location
- No two I/O cells can occupy same location

I/O, Core Placement Methodologies

- (1) Fix core, place I/Os; (2) Fix I/Os, place core
- Alternating core-first
  - detach I/Os, place core cells, re-attach I/Os
  - start alternation with (1)
- Alternating I/O-first
  - start alternation with (2)
  - *random* or *user-defined* initial I/O placement
- Simultaneous

(Hierarchical) Placement Engines

- Quadratic (analytic) placers
  - continuous placement for min $(WL)^2$ or min WL
  - legalization by partitioning or transportation
  - many metaheuristics
- Pure min-cut placers
  - KL-FM iterative variants, min net cut objective
  - fidelity to min WL via terminal propagation, etc.
  - many metaheuristics

Motivating Observations

- “Not much” WL savings in AA regime (Maheshwari et al. 1995)
- Alternative I/O-first bad in PU regime (Pedram et al. 1991)
  - result may not converge
  - strongly dependent on initial I/O placement
- Quadratic placers require anchors (fixed I/Os)
- Hierarchical partitioning != assignment

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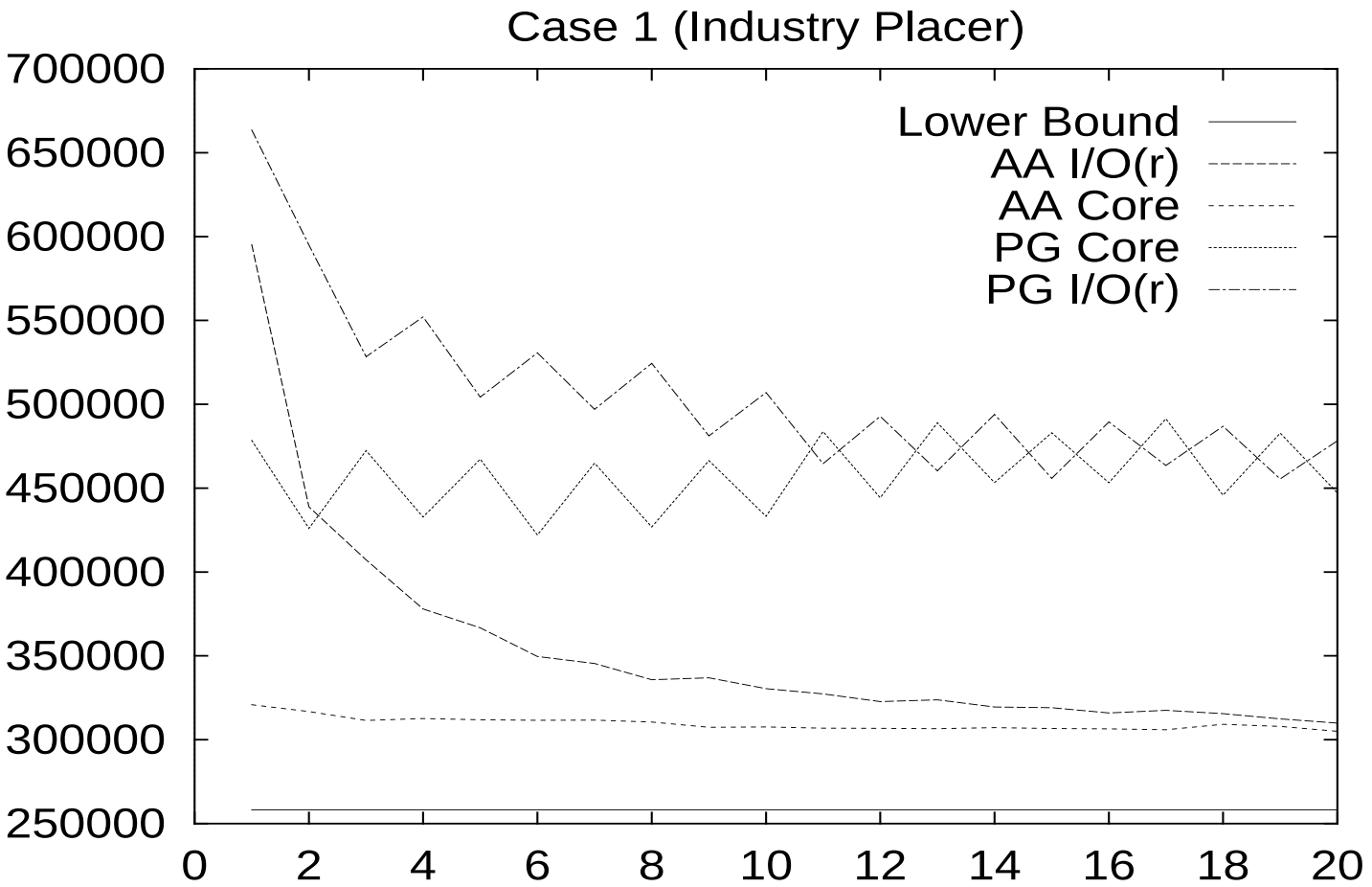
Experimental Questions

- Influence of I/O placement on final WL in AA regime?
- Alternating core-first vs. alternating I/O-first?
- Simultaneous vs. alternating?

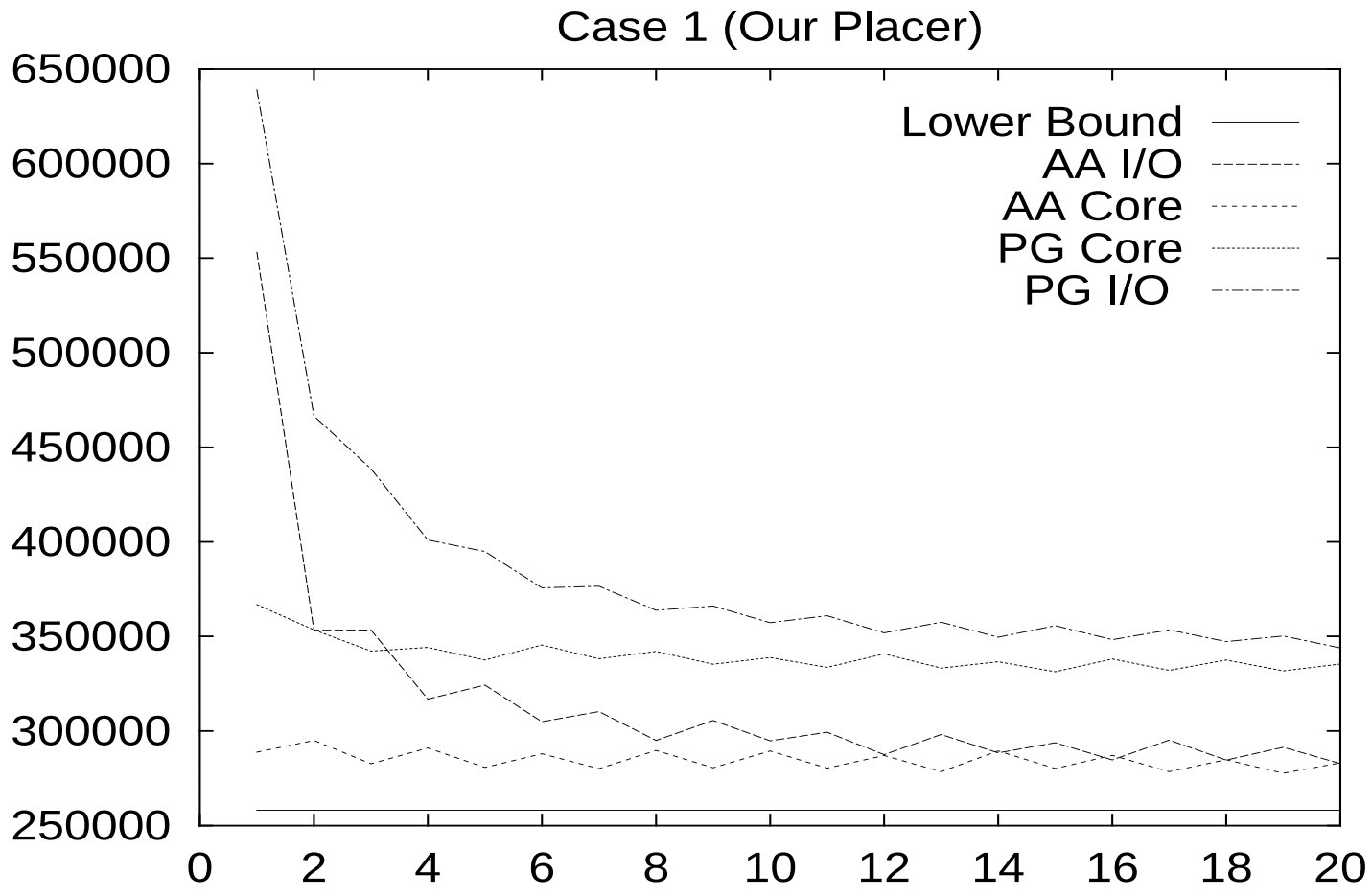
Experimental Testbed

- Four capabilities needed
  - 1. place core cells with I/Os detached
  - 2. place core cells with fixed I/Os
  - 3. place I/Os onto discrete locations with core fixed
  - 4. place I/Os, core simultaneously
- Industry placer w/coercion → 1,2,3
- Our placer (bipartition, assignment) → 1,2,3,4
- Two test cases (3286/12133 cells; 545/662 I/Os)

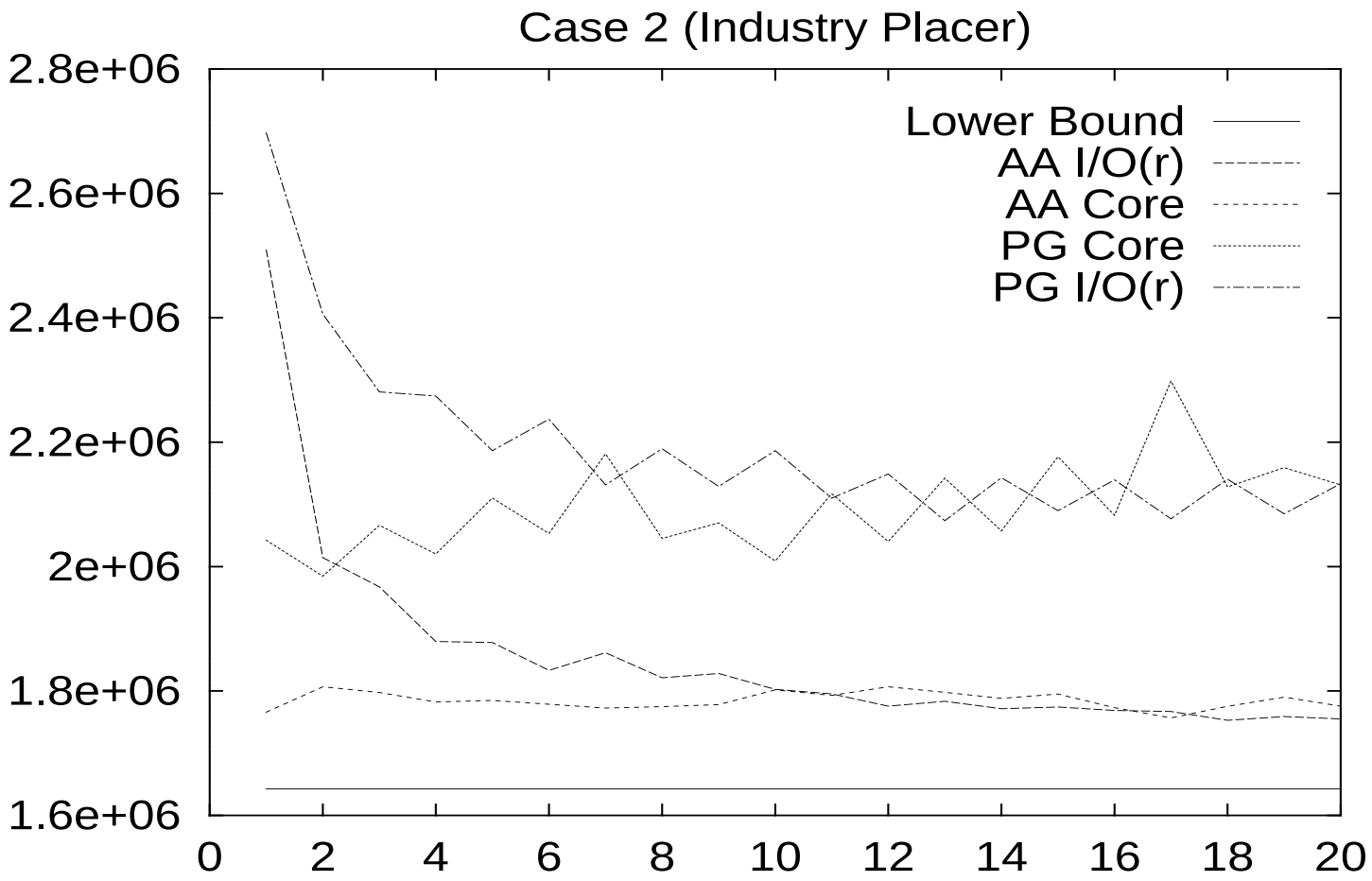
Experimental Results I



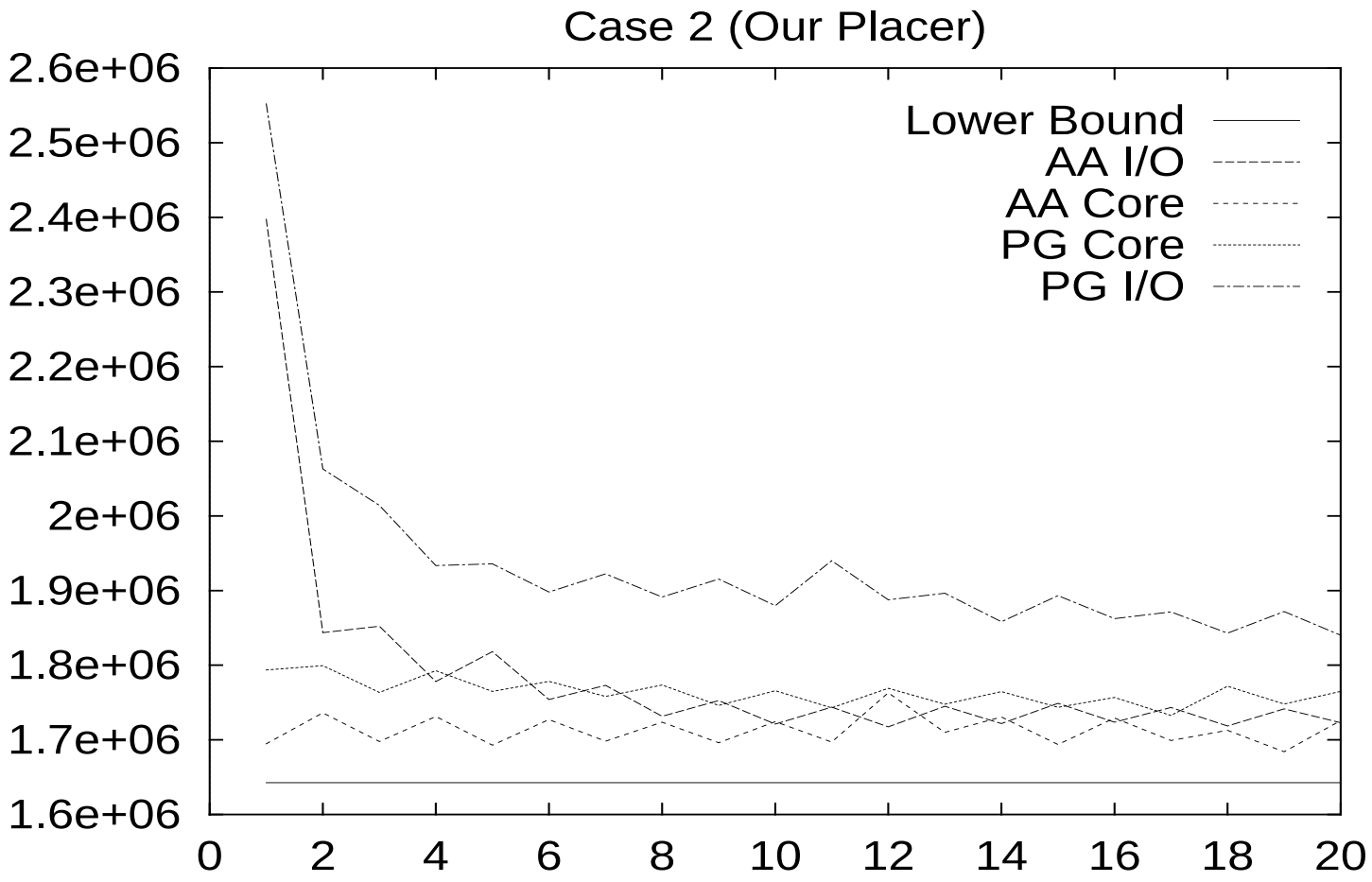
Experimental Results II



Experimental Results III



Experimental Results IV



Conclusions

- Effects of bad initial I/O placement confirmed
- Core-first variants much more successful
- Slow convergence of alternating methodology
- Substantial WL reductions in area-array regime
- Assignment framework for I/O placement
- “Jury still out” for simultaneous methodology

Ongoing Research

- Circuit structure vs. win from area-array I/O

Mutant 0	545, 1030, 1265, 352, 33, 6
Mutant 6	551, 1037, 1272, 345, 26
Mutant 19	564, 1072, 1358, 237
Mutant 110	655, 1459, 1117

- Direct comparison against industry placer
- Improved simultaneous methodology