GTX: The MARCO GSRC Technology Extrapolation System

A. Caldwell, Y. Cao, A. B. Kahng, F. Koushanfar,
H. Lu, I. Markov, M. Oliver,
D. Stroobandt and D. Sylvester

http://vlsicad.cs.ucla.edu/GSRC/GTX/

Supported by Cadence, Synopsys and the MARCO Gigascale Silicon Research Center

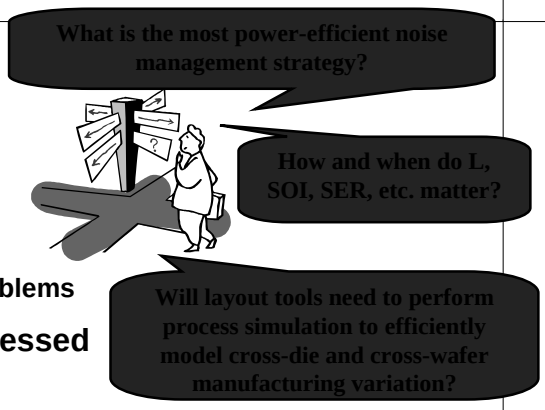
Outline

- **Introduction**
- **Previous efforts**
- **Goals for an "ideal" system**
- **GTX structure**
- **Fundamental features of GTX**
- **Example studies**
  - **Sensitivity analyses of cycle-time models**
  - **Evaluating new device models**
  - **Delay uncertainty study**

2

Introduction: Technology Extrapolation

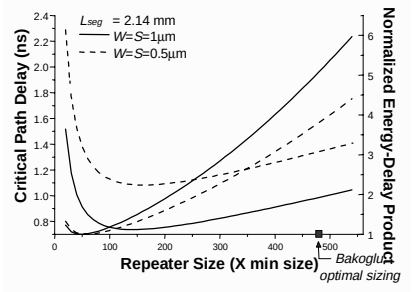
- Evaluates impact of
  - design technology
  - process technology
- Evaluates impact on
  - achievable design
  - associated design problems
- Questions to be addressed
- Sets new requirements for CAD tools and methodologies
- Roadmaps: familiar and influential example



3

Sample Study 1: Optimization

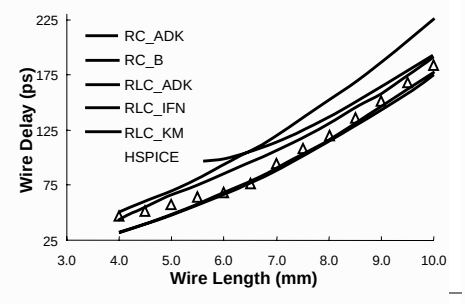
- Most commonly cited optimal buffer sizing expression (Bakoglu)
- New study:
  - Sweep repeater size for single stage in the chain
  - Examine both delay and energy-delay product

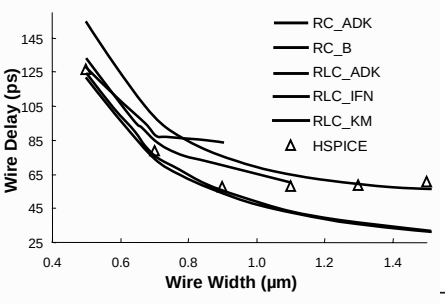


4

Sample Study 2: New Models

- Five different interconnect models
  - Bakoglu's model (RC)
  - [Alpert, Devgan and Kashyap, ISPD 2000] (RC)
  - [Ismail, Friedman and Neves, TCAD 19(1), 2000] (RLC)
  - [Kahng and Muddu, TCAD 1997] (RLC)
  - Extension of [Alpert, Devgan and Kashyap, ISPD 2000] (RLC)





What Do We Need?

- Reuse of existing models, effort
- Framework for adding new models to encompass new aspects of technology, new axes of achievable design
- Ability to evaluate models (sanity, consistency checks)
- Easy model substitution to compare between models
- Sweeping ability to assess the impact of modeling choices
- Constraints to allow elimination of infeasible solutions

6

What is Available?

- **Previous and ongoing efforts**
  - **ITRS Roadmaps**
  - **Tools: SUSPENS, GENESYS, RIPE, BACPAC, …**
  - **Numerous tools in industry**
- **Observations**
  - **Predict "same" parameters but different assumptions, inputs**
  - **Lack of documentation and visibility of internal calculations**
  - **Single inference chain for a given output (hard-coded)**
  - **Inflexible: user cannot define studies of related parameters**
  - **Near-total duplication of effort**
  - **Missing: models of CAD tools and optimizations (what is really "achievable"?)**
  - **Missing: scope, comprehensive coverage**

7

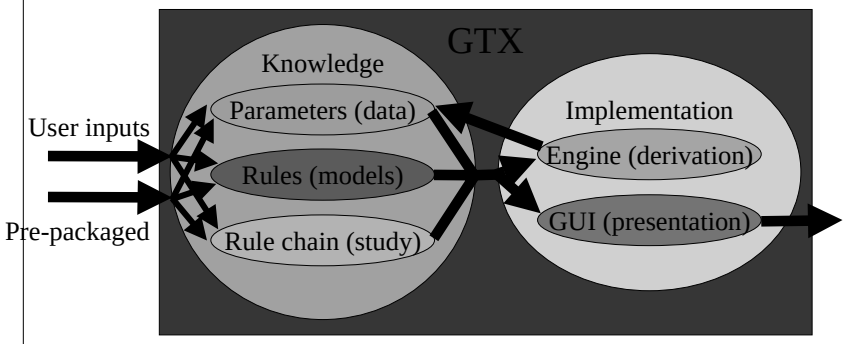
Goals of A New Technology Extrapolation System

- **Flexibility**
  - **Edit or define new parameters and relations between them**
  - **Perform specific studies (but different studies at different times)**
- **Quality**
  - **Continuous improvements**
  - **World-wide participation of experts**
- **Transparency**
  - **Open-source mechanism**
  - **Models are visible to the user**
- **Prevention of redundant effort**
  - **Permanent repository of first choice**
  - **Adoptability and maintainability**

8

GTX: GSRC Technology Extrapolation System

- **GTX is set up as a framework for technology extrapolation**



- **Openness in grammar, parameters and rules**
  - **Easy sharing of data in research environment**
  - **Contributions from other groups**

9

Knowledge Representation

- **Human-readable ASCII grammar**

```
#parameter dl_chip
#type double
#units {m}
#default
  1e-2
#description
  chip side length
#reference
#endparameter
```

```
#rule BACPAC_dl_chip
#description
#output
  double {m} dl_chip;
#inputs
  double {m^2} dA_chip;
#body sqrt(dA_chip)
#reference
#endrule
```

10

Knowledge Representation

- **Human-readable ASCII grammar**
- **Benefits:**
  - **Easy creation/sharing of parameters/rules by multiple users**
    - **D. Sylvester and Y. Cao: device and power, SOI modules that "drop in" to GTX**
    - **P.K. Nag: Yield modeling**
  - **Extensible to models of arbitrary complexity (specialized prediction methods, technology data sets, optimization engines)**
    - **Avant! Apollo or Cadence SE P&R tool: just another wirelength estimator**
  - **Applies to any domain of work in semiconductors, VLSI CAD**
    - **Transistor sizing, single wire optimizations, system-level wiring predictions,…**

11

Parameters

- **Description of technology, circuit and design attributes**
- **Importance of consistent naming cannot be overstated**
  - **Naming conventions for parameters**

[<preposition>] _ <principal> _ {[qualifier] _ <place>} _ {<qualifier>} _ [<adverbial>] _ [<index>] _ [<unit>]

  - **Example: `r_int_tot_lyr_pu_dl`**
  - **Requirements:**
    - **Relatively easy to understand parameter from its name**
    - **Distinguishable (no two parameters should have the same name)**
      - r_int (interconnect resistance) = r_int (interconnect resistivity) ?
    - **Unique (no two names for the same parameter)**
      - R_int = R_wire ?
    - **Sortable (important literals come first)**
  - **Software to automatically check parameter naming**

12

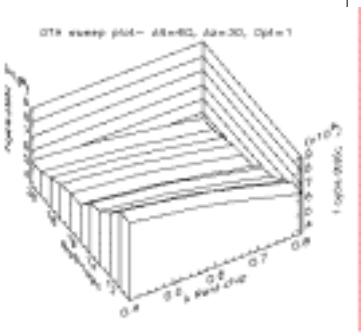
Rules

- Methods to derive unknown from known parameters
- ASCII rules
  - Laws of physics, models of electrical behavior, statistical models
  - Include closed-form expressions, vector operations, tables
  - Storing of calibration data (e.g., “technology files”) for known process and design points in lookup tables
  - Constraints, used to limit range during “sweeping”
- “External executable” rules
  - Assume a callable executable (e.g., PERL script)
  - Use command-line interface and transfer through files
  - Allow complex semantics of a rule
- “Code” rules
  - Implemented in C++ and linked into the inference engine

13

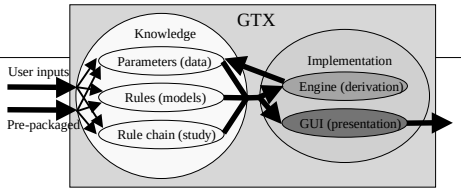
Rule Chains

- “Rule chains” guide inference
  - Acyclic set of rules
  - Interactive specification and comparison of alternative modeling choices
- Studies
  - Input values + rules that make a rule chain
  - User-controlled and savable
  - “Sweeping” of a rule chain
    - Evaluation of all combinations of multi-valued inputs
    - Example: clock frequency for different Rent exponents and varying logic depth



14

GTX Engine

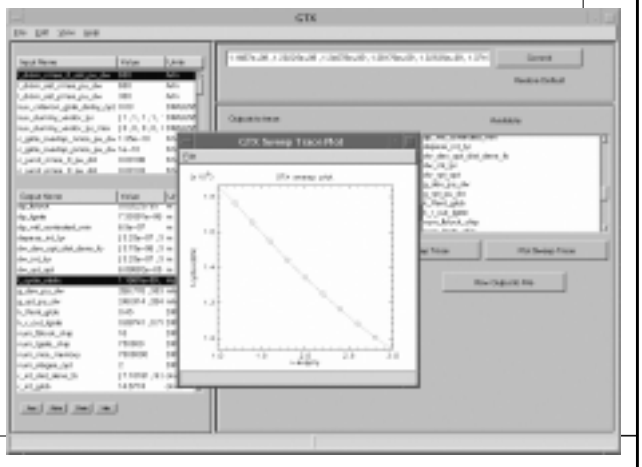


- Contains no domain-specific knowledge
- Evaluates rules in topological order
- Performs studies
- Multiple values through “sweeping”
- Runs on three platforms (Solaris, Windows and Linux)
- URL: http://vlsicad.cs.ucla.edu/GSRC/GTX/

15

Graphical User Interface (GUI)

- Provides user interaction
- Visualization (plotting, printing, saving to file)
- 4 views:
  - Parameters
  - Rules
  - Rule chain
  - Values in chain



GTX Current Status

- **Models implemented**
  - **Cycle-time models of SUSPENS (with extension by Takahashi), BACPAC (Sylvester, Berkeley), Fisher (ITRS)**
  - **Currently adding**
    - **GENESYS (with help from Georgia Inst. Tech.)**
    - **RIPE (with help from Rensselaer Univ.)**
  - **New device and power modules (Synopsys / Berkeley)**
  - **New SOI device model (Synopsys / Berkeley)**
  - **Inductance models (Silicon Graphics / Berkeley / Synopsys)**
  - **Yield model (CMU)**
- **Studies performed in GTX**
  - **Model analysis**
  - **Study of the impact of parameters**
  - **Design optimization studies**

17

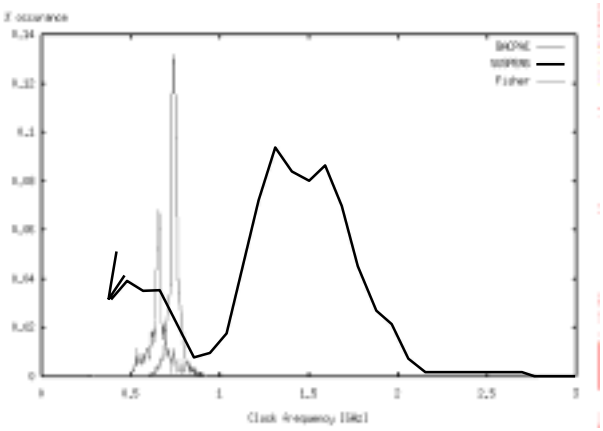
Outline

- **Introduction**
- **Previous efforts**
- **Goals for an "ideal" system**
- **GTX structure**
- **Fundamental features**
- **Example studies**
  - **Sensitivity analyses of cycle-time models**
  - **Evaluating new device models**
  - **Delay uncertainty study**

18

Sensitivity Analysis of Cycle-time Models: Parameter Sensitivity

- **Change parameter values and observe resulting difference in outputs**

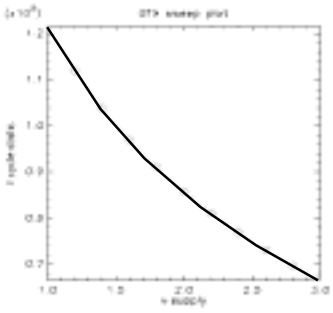


19

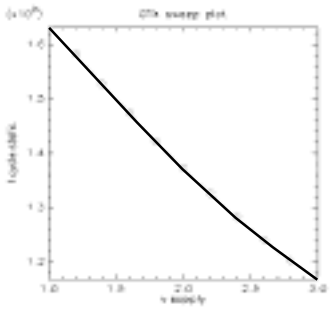
Sensitivity Analysis of Cycle-time Models: Model Sensitivity

- **Replace rule in a model's rule chain by another model's rule and observe the difference in outputs**

BACPAC



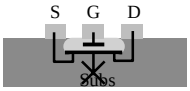
BACPAC with rule from Fisher

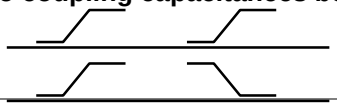


20

Bulk Si Versus SOI Device Models

- New device models for bulk Si and Silicon-on-Insulator (SOI) devices
  - Provided by D. Sylvester (Synopsys) and Y. Cao (UCB)
  - SOI model assumes partially-depleted SOI (PD-SOI) technology and is based on popular BSIM3SOI models
  - Both modules compared to BSIM3 HSPICE runs; results match within 10%
- General study
  - Floating body effect: changes in v_{th} and I_{dsat}
    - Calculate range of possible I_{dsat} values
    - Model ignores the impact of capacitive coupling on body voltage
  - Dynamic delay (due to coupling capacitances between same-layer interconnects)





21

Bulk Si Versus SOI Device Models (Cont.)

- Influence of device technology on clock frequency and power
  - Best case: largest I_{dsat} (realizable due to floating body effect, only for SOI) and no effective coupling capacitance: f from 1.03 GHz (bulk) to 1.31 GHz (SOI)
  - Worst case: smallest I_{dsat} and switching factor of 2: 867 MHz and 1.05 GHz
  - Power results

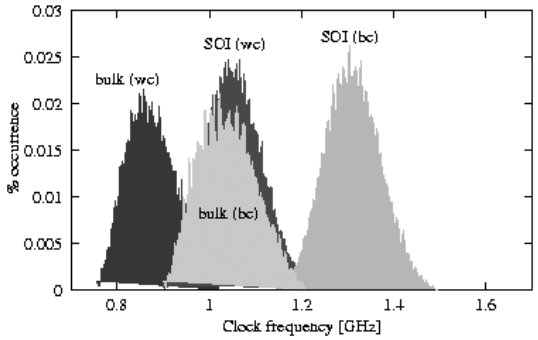
	Bulk Si		SOI	
	P (W)	%	*P* (W)	%
Logic + local wires	26.20	46.18	28.99	43.91
Global interconnects	2.20	3.88	2.60	3.93
I/O drivers + pads	11.71	20.65	13.35	20.22
Clock distribution	7.93	13.98	9.65	14.62
Memory	0.94	1.66	0.86	1.31
Short circuit	7.68	13.54	10.21	15.47
Leakage	0.07	0.12	0.36	0.54
Total power	56.74	100.00	66.03	100.00

    - SOI: 16% increase in power versus Bulk but 24% increase in frequency

22

Bulk Si Versus SOI Device Models (Cont.)

- **Parameter sensitivity of both models**
  - **Several technology related parameters are varied by +/- 10%**

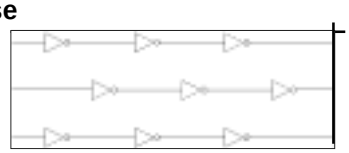


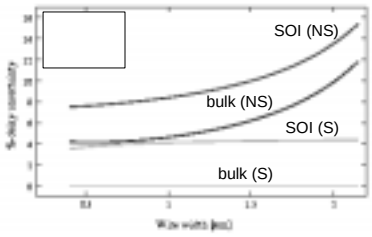
  - **SOI slightly less sensitive to input parameter changes**
  - **Process spread (between best-case and worst-case) larger for SOI**

23

Delay Uncertainty Study

- **Staggered repeaters**
  - **First introduced in [Kahng et al, VLSI Design 99] to reduce delay and noise**





24

Conclusion

- GTX: a new framework for technology extrapolation
- Flexible and extensible
- Enables easy reuse of models
- Provides a common parameter base between all models
- Provides user interaction
- Relies on open-source and contributions by expert users
- “Living Roadmap”
- Technology extrapolation becomes easier
- More principled understanding of requirements for CAD tools
- URL: http://vlsicad.cs.ucla.edu/GSRC/GTX/

25

GTX Project Information

- Design: A. Caldwell, A. B. Kahng, I. Markov, M. Oliver and D. Stroobandt
- Implementation: M. Oliver
- Knowledge gathering and study implementation: A. B. Kahng, F. Koushanfar, H. Lu and D. Stroobandt
- Model extensions and new studies: Y. Cao, X. Huang, S. Muddu, P.K. Nag and D. Sylvester
- Detailed information and downloading of latest version of GTX: http://vlsicad.cs.ucla.edu/GSRC/GTX/
- To contact the developers, ask questions, send comments, or to contribute models to GTX, please send E-mail to GTX@cs.ucla.edu

26