C u r r i c u l u m V i t a e

November 3, 2015

Personal

Name: **Igor L. Markov** E.mail address: imarkov@eecs.umich.edu
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Education

- Ph. D. in Computer Science, UCLA, 2001
- Master of Arts in Mathematics, UCLA, 1994.
- Diploma with Honors in Mathematics, Kiev University, 1994.

Work experience

Google, January 2014- Software Engineer.

Stanford Univ., EE Dept., November 2013- Visiting Professor.

Univ. of Michigan Ann Arbor, EECS Dept., 2012- Full Professor.

Moscow University, Dept. of Computational Mathematics and Cybernetics, May 2013 Visiting Professor.

Univ. of Michigan Ann Arbor, EECS Dept., 2006-2012 Associate Professor.

Synopsys, Inc., Sunnyvale, CA (NASDAQ: SNPS), May-August 2008 (via acquisition of Synplicity)

Synplicity, Inc., Sunnyvale, CA (NASDAQ: SYNP), January-May 2008 Principal engineer: ECAD algorithms and SW.

National Taiwan University, EE Dept., September-October 2007 Visiting Associate Professor.

Univ. of Michigan Ann Arbor, EECS Dept., 2000-2006 Assistant Professor.

UCLA, Computer Science Department, 1996-2000 Research in VLSI CAD. Research Assistant.

UCLA, Mathematics Department, 1994-96 Teaching Assist./Assoc.: College Mathematics and Computer Programming.

Parametric Technology Corp., Waltham, MA (NASDAQ: PMTC), 1995 SW engineer: solid-modeling CAD and computer graphics.

Professional societies: IEEE Fellow, ACM Distinguished Scientist

Honors, Awards and Selected Invited Lectures

- IBM University Partnership Award, **2001**.
- The *IEEE/ACM Design Automation Conference fellowship*, **2001**.
- Invited speaker at the IBM Annual All-site Meeting in Fishkill, NY **2001**.
- Invited papers/talks at *Int'l Symp. on Quality Electronic Design* **2003**, *Int'l Symp. on Physical Design* **2003** and *Int'l Workshop on Logic Synthesis* **2003**.
- Distinguished Lecture in Quantum Information Processing, *National Institute of Standards and Technology* (NIST), Radiation Physics Division, January **2004**.
- The **2004** *IEEE Circuits and Systems (CaS) Society Donald O. Pederson Award* (presented at DAC 2004) for the paper, "Synthesis of Reversible Logic Circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 6, pp. 710-722, June 2003 (with V.V. Shende, A.K. Prasad, and J.P. Hayes).
- Three-lecture tutorial at a summer school on symmetries in AI at the Univ. St. Andrews, Scotland, June **2004**.
- Invited speaker at the Intel research symposium in Haifa, Israel, June **2004**.
- The 2004 ACM *Special Interest Group on Design Automation (SIGDA) Outstanding New Faculty Award* (presented at ICCAD in November **2004**).

- *Best-paper award at DATE* **2005**, for the paper "Accurate Reliablity Evaluation and Enhancement via Probabilistic Transfer Matrices" by S. Krishnaswamy, G. F. Viamontes, I. L. Markov and J. P. Hayes.
- *NSF CAREER Award* **2005**.
- ACM Recognition of Service Award **2005**.
- Synplicity Inc. Faculty Award **2005**.
- ACM SIGDA *Technical Leadership Award* (presented at ICCAD in November **2005**).
- IEEE *Senior Member*, November **2005**.
- First place at the ISPD **2007** global routing contest.
- Invited talks at EDPS **2007**, **2008**, **2010**.
- ACM SIGDA, Advisory Board **2005-2006** and Executive Board **2007-2009**, Communications chair **2009-2012**.
- Invited attendee at the Google Faculty Research Summit in Mountain View, CA, July **2007**.
- ACM *Senior Member* **2007**, ACM Distinguished Scientist **2011**.
- A series of 8 invited lectures at Taiwan Universities in September-October **2007**: National Taiwan Univ. (EE/EDA, EE/CS and CSIE), National Cheng-Kung Univ. (EE and CS), Sun Yat-sen Univ. (CS), National Chiao Tung Univ. and Tsing-Hua Univ.
- Invited presentation at the meeting of the IEEE Kansai chapter in Kyoto, Japan, October **2007**.
- Invited talk at SASIMI 2007 in Sapporo, Japan, October **2007**.
- Communications of ACM (CACM) member of editorial board, January **2008**.
- EECS Outstanding Achievement Award from the Univ. of Michigan, January **2008**.
- Microsoft *A. Richard Newton* Breakthrough Research Award, March **2008**.
- Best-paper award at Int'l Symposium on Physical Design (ISPD), Portland, OR, April **2008** (with Steve Plaza and Prof. Valeria Bertacco).
- Invited talk at VTS 2008 in San Diego, CA, April **2008**.
- Invited mini-course on Physical Design of Integrated Circuits in Bento Gonçalves, Brazil, May **2008**.
- Invited speaker at the Intel research symposium in Haifa, Israel, June **2008**.
- Invited attendee at the Microsoft Faculty Research Summit in Redmond, WA, July **2008**.
- First place at the ISPD **2009** clock-network synthesis contest.
- ACM SIGDA Service Award **2009**.
- Presenter at the National Science Foundation workshop on the Future of Electronic Design Automation; Arlington, VA, July **2009**.
- IEEE CEDA Early Career Award **2009** for outstanding contributions to algorithms, methodologies and software for the physical design of integrated circuits, presented at ICCAD **2009**.
- First place at the ISPD **2010** clock-network synthesis contest.
- *Best-paper award* at the Int'l Conf. on Computer-Aided Design (ICCAD) **2010**, San Jose, CA.
- Panelist, session chair, panel organizer and invited workshop speaker at DAC **2011**.
- Invited tutorial presenter at ICCAD **2011** and **2012**.
- GSRC A. Richard Newton impact award **2012**.
- Best paper award at *the Turing Centenary Conference*, Manchester, UK, **2012**.
- First pace at the ICCAD **2012** place-and-route contest.
- IEEE *Fellow*, November **2012**.

- First and second places at the ISPD **2013** gate-sizing contest (in two categories resp.)
- A mini-course at Moscow State University, May **2013**.
- DAC *Prolific Author Award*, June **2013**.
- *Top Writer*, Quora, **2013**.
- Best-paper award nominations at DAC **1997**, ASPDAC **1999**, ASPDAC **2000**, DAC **2003**, DAC **2004**, DATE **2005**, ISPD **2006**, ISPD **2008**, ICCAD **2010**, ISPD **2011**, ICCAD **2011**, DATE **2012**, ISPD **2012**.

Honors and Awards Won by Students

- Arathi Ramani and Saurabh Adya: *Design Automation Conf. (DAC) fellowship*, **2001**
- DoRon Motter: *Motorola fellowship*, **2001**
- DoRon Motter: 1^{st} place at *ICCAD CADathlon* **2002**
- Vivek Shende and Aditya Prasad: *IEEE CaS Donald O. Pederson paper-of-the-year award* (IEEE Trans. on Computer-Aided Design), **2003**
- George Viamontes: *US Dept. of Energy High-performance Computing Fellowship*, **2003**
- Matt Hardy: 1^{st} place at the *student design contest at the Design Automation Conf.* (DAC) **2004**
- Saurabh Adya: *graduate mentorship award from the University of Michigan*, **2004**
- Hayward Chan: honorable mention from the *Computing Research Association* (CRA) for work on block-packing with symmetries, **2004**
- Gabe Black and Jarrod Roy: 1^{st} place at *ICCAD CADathlon* **2004** (shared with MIT)
- Smita Krishnaswamy and George Viamontes: best paper award at the *Design Automation and Test in Europe Conf.* (DATE) **2005**
- Jarrod Roy: 1^{st} place at *ICCAD CADathlon* **2005**
- Jarrod Roy: *Rackham Graduate fellowship*, **2006**
- Aaron Ng: Nominated for the best paper award at the *Int'l Symp. on Physical Design* (ISPD) **2006**
- Kai-Hui Chang and David Papa: 1^{st} place at the *IWLS* **2006** *Implementation Challenge*
- Jin Hu: *Rackham Graduate fellowship*, **2006**
- Kai-Hui Chang and George Viamontes: 2^{nd} place at *ICCAD CADathlon* **2006**
- Jarrod Roy: winner of the *ISPD* **2007** *routing contest* (1^{st} place in the 2D category, 3^{rd} place in the 3D category)
- Michael Moffitt: winner of the *ISPD* **2007** *routing contest* (1^{st} place in the 3D category, 2^{nd} place in the 2D category)
- Michael Moffitt: winner of the *IBM Joseph Raviv postdoctoral fellowship*, **2007**
- Smita Krishnaswamy and Steve Plaza: 2^{nd} place at the *IWLS* **2007** *Implementation Challenge*
- Héctor Garcia: *Rackham Graduate fellowship*, **2007**
- Kai-hui Chang: *EDAA Outstanding Ph.D. Dissertation Award*, presented at DATE **2008** in Munich, Germany.
- Steve Plaza: *best paper award* at the Int'l Symposium on Physical Design (ISPD) **2008**, Portland, OR.
- Dongjin Lee: 1^{st} place at the *ISPD* **2009** *clock-network synthesis contest* in San Diego, CA.
- Kai-hui Chang: *ACM SIGDA Outstanding Ph.D. Dissertation Award*, presented at DAC **2009**, San Francisco, CA.
- Hector Garcia: 1^{st} Place in Technical Paper Competition at *SHPE* **2009** in Washington, DC.
- Smita Krishnaswamy: *EDAA Outstanding Ph.D. Dissertation Award*, presented at DATE **2010** in Dresden, Germany.
- Dong-Jin Lee and Myung-Chul Kim: 1^{st} place at the *ISPD* **2010** *clock-network synthesis contest*, San Francisco, CA.

- Dong-Jin Lee and Myung-Chul Kim: *best paper award* at the Int'l Conf. on Computer-Aided Design (ICCAD) **2010**, San Jose, CA.
- Dong-Jin Lee and Myung-Chul Kim: 2^{nd} place at the ICCAD **2010** CADathlon contest, San Jose, CA.
- David Papa: *EDAA Outstanding Ph.D. Dissertation Award*, presented at DATE **2011** in Grenoble, France.
- Jin Hu: *Outstanding Graduate Student Instructor Award*, **2011**
- Héctor Garcia: *Rackham Centennial fellowship*, **2012**
- Myung-Chul Kim, Jin Hu and Dong-Jin Lee: 1^{st} place at the *ICCAD* **2012** *place-and-route contest* organized by IBM Research
- Pankit Thapar and Benjamin vander Sloot: 1^{st} and 2^{nd} places at the *ISPD* **2013** *gate-sizing contest* organized by Intel Labs
- Daniel MacLennan, Peter Xie and Andrew Segavac: 3^{rd} place at the *ICCAD* **2013** *logic-synthesis contest* organized by Cadence Design Systems

Research interests

- Machines that make machines
- Algorithms, tools and methodologies for Electronic Design Automation, including 3D integrated circuits
- Intellectual property protection and IC security
- Algorithms for search and combinatorial optimization
- Quantum information and computation

Teaching interests

Undergraduate	Graduate
Algorithms and Data Structures, Digital Electronics	Analysis and Design of Algorithms
Object-oriented programming, Graph Algorithms	CAD for VLSI, Combinatorial Optimization
Discrete Mathematics, Mathematical Programming	Quantum Information Processing

- Guided graduate student seminars on (i) quantum computing,
  (ii) physical synthesis, verification and test of integrated circuits
- Taught large undergraduate courses on logic circuits, algorithms and data structures, and algorithm analysis

Professional Service

SERVICE AT THE UNIVERSITY OF MICHIGAN

- Member of the Fulbright Committee, 2001
- Undergraduate student advisor at the Department of EECS, 2001-2003
- Member of the Computing Infrastructure committee at the Department of, EECS 2003-2005
- Member of the Graduate Committee at the CSE Division, 2005-2006
- Internal referee for four faculty/lecturer reviews, 2005-2008
- Member/chair of major review committees at the CSE Division, 2006, 2008, 2009
- Member of a major review committee at the ECE Division, 2011
- Chair of the undergraduate program in Computer Engineering, 2006-2013
- Member of the Research Strategy Committee at the College of Engineering, 2007
- Member of the committee reviewing graduate programs in Computer Science and Engineering, 2011
- Member of the committee reviewing the Computer Science/LSA program, 2011

- Director of the Sun Microsystems *Center of Excellence* at the University of Micigan, 2007-2009
- College of Engineering Representative for several faculty candidates
- Member of several dozen Ph.D. committees at the EECS, IOE and Mechanical Engineering Departments
- Member of qualifying examination committees (every semester)
- Also see **Work with Graduate and Undergraduate Students** below

MEMBERSHIP IN OFF-CAMPUS DISSERTATION AND THESIS COMMITTEES

- Universidade Federal do Rio Grande do Sul (UFGRS), Porto Alegre, Brazil
  Doctoral Committee for *Renato Hentschke* — June 2007
- University of Michigan Dearborn; Master's Thesis Committee for *Héctor Garcia* — August 2007
- University of Waterloo, Canada, Doctoral Committee for *Kristofer Vorwerk* — July 2009
- University of Toronto, Canada, Doctoral Committee for *Marcel Gort* — March 2014

EDITORIAL ASSIGNMENTS

- Member of the Editorial Board of *ACM Journal on Emerging Technologies in Computing*, 2010-current.
- Member of the Editorial Board of *IEEE Design & Test*, 2009-current.
- Member of the Editorial Board of *Communications of ACM*, 2008-curent.
- Member of the Editorial Board of *IEEE Transactions on Computer-Aided Design*, 2008-current.
- Member of the Editorial Board of *IEEE Transactions on Computers*, 2007-2011.
- Associate Editor of *ACM Transactions on Design Automation of Electronic Systems* (TODAES), 2007-2011
- Guest Editor, *Integration: the VLSI Journal*, 2005-2006
- Editor of the *ACM SIGDA newsletter* (over 2,700 subscribers), 2005-2007;
  Associate Editor, 2002-2005. Contributed the article "*What is Post-Silicon Debug?*" (May 2008)
- Editor of the online *GSRC Bookshelf for CAD Algorithms* `http://vlsicad.eecs.umich.edu/BK`, 2000-2007.

OTHER BOARD & TASK FORCE MEMBERSHIPS

- *IEEE committee for selecting IEEE Fellows*, 2014
- *ACM committee on Ethics an Plagiarism*, 2014-
- *ACM Computing Classification System* Committee, chair of the Hardware track, 2011
- *ACM Special Interest Group on Design Automation* (SIGDA) advisory board, 2005-2006,
  Executive Board, 2007-current (re-elected in 2009)
- Chair of the SIGDA Technical Committee on Emerging Technologies in Computing, 2010-2011
- *NSF workshop on the Future of Electronic Design Automation*, Arlington, VA, 2009
- *ACM Task Force on revitalizing the Communications of the ACM*
  (organized by ACM Pres. David Patterson, chaired by Prof. Moshe Vardi), 2007
- SIGDA liaision to the CADathlon programming contest at ICCAD, 2006
- *Digital Logic* advisory board with McGraw Hill Corp.,
  focusing on undergraduate courses in Digital Logic, 2005-2006
- *ACM Student Research Competition* at DAC 2010 (judge)

ORGANIZATIONAL ACTIVITIES AND PROGRAM COMMITTEE CHAIRMANSHIPS

- Moderator for *Emerging Technologies*, Computing Research Repository CoRR (http://arxiv.org/corr) (2011-)
- Topic chair for IC Physical Design at *ACM/IEEE Design Automation and Test in Europe Conf.* (DATE) 2009-11
- Topic chair for New, Emerging, Specialized Design Technologies *ACM/IEEE Design Autom. Conf.* (DAC), 2009-2010
- Topic chair for VLSI Floorplanning and Placement *ACM/IEEE Int'l Conf. on Computer-Aided Design* (ICCAD) 2010

- Track chair for Post-CMOS VLSI, *ACM Great Lakes Symposium on VLSI* (GLSVLSI), 2009-2011
- *ACM Int'l Workshop on Logic and Synthesis* (IWLS): publications chair (2008), special sessions chair (2009), general chair (2010), technical program committee co-chair (2011)
- Vice-chair for Tools and Methodologies at *IEEE Intl. Conf. on Computer Design* (ICCD), 2005
- Co-founder of the *ACM/IEEE Intl. Workshop On System-Level Interconnect Prediction* (SLIP), served as publicity chair, publication chair, special sessions chair (2000-2003) program committee chair (2004) and general chair (2005)
- Organizer of special sessions at the *ACM/IEEE Design Automation Conference* 2003, 2006, 2009 and 2010
- Session chair/moderator: DATE 2003-04,2008; SLIP 2000-05,2007; ISPD 2002-03,2005,2008-11; ISCAS 2002-03; ICCAD 2003-05, 2007; ASPDAC 2007; ICCAD 2007; ISPD 2010, DAC 2011

MEMBERSHIP IN PROGRAM COMMITTEES

- *ICCAD* tutorial selection committee, 2011
- *ACM TODAES* best-paper selection committee, 2008, 2010 (chair)
- *NanoArch* best-paper selection committee, 2009
- *ACM/IEEE Design Autom. Conf.* (DAC), 2004-05 (Placement and Floorplanning), 2006,2009-10 (Emerging Tech.)
- *ACM/IEEE Design Automation and Test in Europe* (DATE) Conf., 2003-2005 (Physical Design), 2007 (Circuit Test), 2008-2011 (Physical Design), 2014 (Physical Design and Logic Synthesis)
- *ACM/IEEE Asia and South Pacific Design Autom. Conf.* (ASPDAC), 2008,09 (Verification)
- *IEEE Symp. on Defect and Fault Tolerance in VLSI Systems* (DFT), 2008,09
- *ACM/IEEE Intl. Conf. on Computer-Aided Design of Integrated Circuits* (ICCAD), 2003-2005, 2009-2010
- *ACM/IEEE Intl. Symposium on Physical Design* (ISPD), 2002-2005, 2008-2011
- *The Satisfiability Symposium* (SAT), 2010-11
- *IEEE/ACM Symposium on Nanoscale Architecture* (NanoArch), 2007-2010
- *Intl. Symmetry Conference* 2007
- *ACM International Conference on Computing Frontiers* 2007
- *ACM/IEEE Great Lakes Symposium on VLSI* (GLSVLSI), 2002-04,2009-11
- *AAAI Workshop on Symmetry in Constraint-Satisfaction Problems* (SymCon), since 2003-2009
- *ACM/IEEE Intl. Workshop on Logic and Synthesis* (IWLS), since 2002
- *ACM/IEEE Intl. Workshop On System-Level Interconnect* (SLIP), since 1999
- *Workshop on Theory of Quantum Computation, Communication and Cryptography* (TQC), 2008.
- *IEEE DATC Electronic Design Processes Workshop* (EDP) 2008-
- *IEEE Workshop on Design and Test of Nano Devices, Circuits and Systems* (NDCS), 2008
- *Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms* (ERDIAP), 2011

REVIEWING, REVIEW PANELS, REFERENCES

- Book reviews for MIT Press, Cambridge Univ. Press, Oxford Univ. Press
- Proposal reviewer/panelist at the US National Science Foundation (NSF) and the US Dept. of Defense (DoD), Proposal reviewer for Nat'l Sciences and Engneering Research Council Canada (NSERC), Proposal reviewer for the Research Competitiveness Service (RCS) of American Association for the Advancement of Science (AAAS)
- IEEE senior member review panelist

- Reviewer for journals and Magazines: *ACM Transactions on Design Automation, ACM Transactions on Reconfigurable Systems, ACM Journal of Emerging Technologies in Computing, AIMS Advances in Mathematics and Communications, Nature, Nature Physics, APS Physical Review A, Journal of Statistical Physics, IOP Journal of Physics A: Mathematical and Theoretical, New Journal of Physics, IEEE Transactions on Computers, IEEE Transactions on CAD, IEEE Transactions on VLSI, IEEE Transactions on Circuits and Systems I, IEEE Transactions on Circuits and Systems II, IEEE Transactions on Information Forensics and Security, IEEE Transactions on Nanotechnology, IEEE Transactions on Nanobioscience, IEEE Design and Test, Nature Photonics, Quantum Information and Computation, Quantum Information Processing, Theoretical Computer Science, Discrete and Applied Mathematics, Constraints, Annals of Operations Research, IEE Proceedings: Computers and Digital Techniques, IEE Proceedings: Circuits, Devices and Systems, IEE Electronic Letters, Journal of Electronic Testing, Journal of Universal Computer Science, IOP Journal of Physics A: Mathematical and Theoretical, Journal of Multiple-Valued Logic and Soft Computing, Journal of Formal Methods in System Design, Journal of Parallel and Distributed Computing, Integration: the VLSI Journal, Microelectronics Journal, International Journal of Electronics, The Computer Journal*
- Reviewer for conferences: *ACM/IEEE Design Automation Conf. (DAC), ACM/IEEE Intl. Conf. on Computer-Aided Design (ICCAD), IEEE/ACM Design Automation & Test in Europe (DATE), IEEE/ACM Intl. Symposium on Circuits and Systems (ISCAS), ACM Intl. Symposium on Computer Architecture (ISCA), ACM Architectural Support for Programming Languages and Operating Systems (ASPLOS), AAAI Intl. Joint Conf. on Artificial Intelligence (IJCAI), Uncertainty in Artificial Intelligence (UAI), International Test Conference (ITC)*
- Reference for internal promotions at IBM, 2007, 2008
- Reference for univ'ty appointments and tenure promotions at top universities in the US, Canada, Australia, China, Israel.

MISCELANEOUS SERVICE

- Co-developed (with Dr. Lou Scheffer from Cadence) a software system for DUplicate text DEtection (DUDE) that has been used by all major ACM SIGDA conferences and IEEE Transactions on Computer-Aided Design to filter submitted manuscripts. For more details, see `http://sigda.eecs.umich.edu/DUDE/`

Research Funding

- Int'l Business Machines Corp. (IBM), **2000-2003**.
- Defense Advanced Projects Agency (DARPA), *Quantum Information Science and Technology*, **2001-2005**.
- Semiconductor Industry Association (SIA/MARCO) and DARPA via *the Gigascale Silicon Research Center* (GSRC), **2001-2006**.
- National Science Foundation (NSF) *Information Technology Research* (ITR), **2002-2006**.
- National Science Foundation (NSF) *Computer Architecture* (CA), **2002-2005**.
- Synplicity, Inc., **2003-2008**.
- National Science Foundation (NSF) *Design Automation* (DA/SGER), **2003-2004**.
- National Science Foundation (NSF) *CAREER*, **2005-2010**.
- Univ. of Michigan, Division of Computer Science and Engineering, *High-visibility Projects in CSE*, **2004-2005**.
- AirForce Research Laboratory (AFRL), **2006-2013**.
- University of Michigan, Undergraduate Research Opportunity (UROP) **2006-2007**.
- IEEE Council on EDA via *MP Associates*, **2007**.
- Microsoft Corp., **2008**.
- Sun Microsystems, **2008, 2009**.
- eASIC, **2009**.
- Texas Instruments, **2009**.
- National Science Foundation (NSF), *EAGER* **2009-2011**.
- National Science Foundation (NSF), **2012-2015**.
- Semiconductor Research Corp. (SRC), **2012-2015**.
- Mentor Graphics, **2012-2013**.
- Equipment donations from IBM (**2002**), Intel (**2004, 2008**), Altera (**2005**), AMD (**2006**) and Sun (**2007-2008**).

Work with Graduate Students

- Graduated eleven Ph.D. students – Dr. Arathi Ramani (Microsoft), Dr. Saurabh Adya (Synopsys), Dr. George Viamontes (Lockheed Martin), Dr. Kai-hui Chang (Avery Design Systems), Dr. Steve Plaza (Synopsys Advanced Technology Group), Dr. Smita Krishnaswamy (IBM Research / T.J. Watson Lab), Dr. Jarrod Roy (IBM Austin), Dr. David Papa (IBM Research / ARL), Dr. Dongjin Lee (Samsung Group), Dr. Myung-Chul Kim (IBM Research / ARL), Dr. Jin Hu (IBM Corp)
- Of the current and past graduate students, three are minorities and four are women. Most of my students have published and presented their work at national and international conferences and symposia. They have successfully interned at IBM Research, Cadence Labs, Mentor Graphics, Synopsys, Calypto Design Systems, Texas Instruments.

Work with Undergraduate Students

- Organized research projects for six freshmen and sophomores under the Undergraduate Research Opportunity Program (UROP) at the University of Michigan in AY 2006/2007.
- Organized directed studies projects (EECS 499) and summer research projects (SURE) for 20+ talented undergraduate students. Some of them are now employed at Amazon.com, Google.com, Microsoft, Dept. of Defense, Toyota Research, and some went to graduate school at Stanford, Princeton, UT Austin, and Univ. of Michigan.
- Shared the 2004 Donald O. Pederson "paper-of-the-year" award (presented at DAC) with two undergraduates Vivek Shende and Aditya Prasad (now at Princeton/Math and Amazon.com resp.)
- Together with undergraduate co-authors, published three peer-reviewed workshop papers (IWLS 2002-03, 2014 and SymCon 2003), conference papers (ICCAD 2002, DATE 2004, DATE 2013, SPIE QIC 2004, GLSVLSI 2004, ICCAD 2014), and journal papers (IEEE Trans. on CAD, Quantum Information and Computation, APS Physical Review A).
- Undergraduate student Hayward H. Chan received an honorable mention from CRA in Fall 2004 for his work on block packing with symmetries.
- Provided reference letters to a number of undergraduate students applying to graduate school, as well as for various awards and scholarships.

Patents and Patent Applications:

- I. L. Markov and K. S. McElvain, US Patent 8141024, "Temporally Assisted Sharing in Electronic Systems", issued Mar 20, 2012.
- K.-H. Chang, I. Wagner, I. L. Markov, and V. Bertacco, U.S. Patent 8365110, "Automatic Error Diagnosis and Correction for RTL Designs," issued Jan 29, 2013.
- I. L. Markov and K. S. McElvain, US Patent 8,453,084, "Approximate Functional Matching in Electronic Systems" issued May 28, 2013.
- J. A. Roy, I. L. Markov, F. Koushanfar US Patent 8,732,468, "Protecting Bus-based Hardware IP by Secret Sharing," issued May 20, 2014.
- J. A. Roy, I. L. Markov, F. Koushanfar U.S. Patent Application No. 12/127,523, "Methods for Protecting Against Piracy of Integrated Circuits," March 2009.

Publications:[1]

Electronic versions are at `http://www.eecs.umich.edu/~imarkov/pubs/`

Books and Book Chapters (dissertations not included)

B13. (with S. Krishnaswamy and J. P. Hayes), "Design, Analysis and Test of Logic Circuits Under Uncertainty," 134 pages, Springer **2013**, (ISBN 978-9048196432).

B12. (with D. A. Papa), "Multi-Objective Optimization in Physical Synthesis of Integrated Circuits," 164 pages, Springer **2013**, (ISBN 978-1461413554).

[1] Two publications unrelated to main research interests (in *IEEE Computer* and *Proc. Kiev Math. Inst.*) not listed.

B11. (with H. Katebi), "Large-scale Boolean Matching" in *Advanced Techniques in Logic Synthesis, Optimizations and Applications*, S. Khatri and K. Gulati, eds; Springer, **2011**.

B10. (with A. B. Kahng, J. Lienig and J. Hu), *VLSI Physical Design: from Graph Partitioning to Timing Closure*, 312 pages, Springer **2011** (ISBN 978-90-481-9590-9).

B9. (with G. F. Viamontes and J. P. Hayes), *Quantum Circuit Simulation*, Springer **2009** (ISBN: 978-9048130641).

B8. (with K.-H. Chang and V. Bertacco), *Functional Design Errors in Digital Circuits: Diagnosis, Correction and Layout Repair*, Springer **2008** (ISBN: 978-1-4020-9364-7).

B7. (with A. A. Kennings), "Circuit Placement," in *Encyclopedia of Algorithms*, M.-Y. Kao, ed.; pp. 143-146, Springer, **2008**.

B6. (with J. A. Roy), "Partitioning-driven Techniques for VLSI Placement," in *Handbook of Algorithms for VLSI Physical Design Automation*, C. Alpert, D. Mehta and S. Sapatnekar, eds; CRC Press, **2008**.

B5. (with J. A. Roy and D. A. Papa), "Capo: Congestion-aware Placement for Standard-cell and RTL Netlists with Incremental Capability," in *Modern Circuit Placement: Best Practices and Results*, G.-J. Nam and J. Cong, eds; Springer, **2007**.

B4. (with D. A. Papa), "Hypergraph Partitioning and Clustering," in *Approximation Algorithms and Metaheuristics*, T. Gonzalez, ed.; pages 61-1 through 61-19, CRC Press, **2007**.

B3. (with A. Ramani), "Automatically Exploiting Symmetries in Constraint Programming," in *Lecture Notes in Computer Science, vol. 3419*, B. Faltings, A. Petcu, F. Fages and F. Rossi, eds; pp. 98-112, Springer, **2005**.

B2. (with D. B. Motter), "A Compressed Breadth-first Search For Satisfiability," in *Lecture Notes in Computer Science, vol. 2409*, D. M. Mount and Cl. Stein, eds; Springer, pp. 29-42, **2002**.

B1. (with A. E. Caldwell and A. B. Kahng), "Design and Implementation of the Fiduccia-Mattheyses Heuristic for VLSI Netlist Partitioning," in *Lecture Notes in Comp. Science, vol. 1619*, M. T. Goodrich, C. C. McGeoch, eds; pp. 177-193, Springer, **1999**.

Papers in journals and magazines

J88. (with J. Hu and M.-C. Kim), "Progress and Challenges in VLSI Placement Research," *Proceedings of IEEE* 103(11), pp. 1985-2003, **2015**.

J87. (with S. M. Plaza), "Solving the Third-Shift Problem in IC Piracy With Test-Aware Logic Locking," *IEEE Trans. on CAD of Integrated Circuits and Systems* 34(6), pp. 961-971, **2015**.

J86. (with H. J. Garcia), "Simulation of Quantum Circuits via Stabilizer Frames," *IEEE Trans. on Computers*, October **2014**.

J85. Igor L. Markov, "Limits to Fundamental Limits on Computation", *Nature* 512, pp. 147-154, August **2014**.

J84. (with H. J. Garcia and A. W. Cross), "On the Geometry of Stabilizer States," *Quantum Information and Computation*, vol. 14, no. 7-8, pp. 683-720, **2014**.

J83. (with R. R. Nadakuditi), "On Bottleneck Analysis in Stochastic Stream Processing," *ACM Trans. on Design Automation of Electronic Sys.* (TODAES), vol. 18, no. 3, article #34, July **2013**.

J82. (with M.-C. Kim and D.-J. Lee), "SimPL: An Algorithm for Placing VLSI Circuits," *Communications of the ACM*, vol. 56 no. 6, pp. 105-113, June **2013**.

J81. (with M. Saeedi), "Synthesis and Optimization of Reversible Circuits - A Survey," *ACM Computing Surveys* vol. 45, no. 2, February **2013**.

J80. I. L. Markov, "Know Your Limits: A Review of 'Limits to Parallel Computation: P-Completeness Theory'," *IEEE Design and Test*, vol. 30, no. 1, pp. 78-83, January **2013**.

J79. (with M. Saeedi), "Faster Quantum Number Factoring via Circuit Synthesis," *Physical Review A* 87, 012310, **2013**.

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