David A. Papa

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Vital Statistics

Date of Birth: February 03, 1981
Place of Birth: Royal Oak, Michigan, United States
Citizenship: United States

Education

University of Michigan Ann Arbor **Grad Date:** Sept 2010
Degree: Ph.D. to be conferred in December 2010 **GPA:** 7.13/9.0
Degree: Masters of Computer Science and Engineering **GPA:** 7.25/9.0
Degree: Bachelor of Computer Engineering **GPA:** 3.6/4.0
Magna Cum Laude

- **VLSICAD**
- Logic Design, Synth., and Verif.
- Adv. Compiler Construction
- Operating Systems
- Adv. Computer Architecture
- Linear Algebra
- Adv. Electrical Engineering
- Theory of Calculus
- Data Structures and Algorithms
- Adv. OO Programming Concepts
- Software Engineering
- Adv. Algorithm Analysis
- Embedded System Design
- Artificial Intelligence
- Electromagnetics
- Combinatorics & Graph Theory

Computer Skills

Languages: C/C++, Tcl and Perl (familiarity with several others).
Libraries: Standard C++ Library, Qt, OpenGL, and OpenAccess.
Environments: Linux, Windows, AIX, Solaris.
Applications: g++, svn, cvs, MS Devel. Studio, gdb, gprof, valgrind.

Experience

Broadway Technology Austin, TX
Senior Developer Jan 2011-Present
- Design and implement automated financial trading system

IBM Austin, TX
Research Coop May 2006-December 2010
- IBM Austin Research Lab (ARL)
- Focus on improvements to **Placement Driven Synthesis (PDS)**
- Improved speed of physical synthesis by four times in two years
- Large software system and team

University of Michigan Ann Arbor, MI
Graduate Student Research Assistant September 2002-May 2006
- Advanced Computer Architecture Lab
- Primary focus on EDA Tools for VLSICAD
- Strong experience with Capo, a leading academic placement tool
- Practical experience collaborating on large software system

Cadence Berkeley Labs Berkeley, CA
Research Scientist June 2004-September 2004
- Developer of open-source software for Open Access 2.2
- Designer of programmer's tool-kit OAGear including placer and GUI.

University of Michigan Ann Arbor, MI
Software Engineer/Research Scientist May 2001 - September 2001
- Research in the field of VLSICAD.
- Programmer of new algorithms relevant to the field.

Honors

EDAA Outstanding Dissertation Award	2010
Outstanding Technical Accomplishment	2009
Early Tenure Inventor – IBM	2008
First Plateau Invention Achievement Award – IBM	2007
Best Contribution Award – IWLS Programming Competition http://www.eetimes.com/news/latest/showArticle.jhtml?articleID=188702906	2006
Eta Kappa Nu engineering honor society	2001
Class Honors	2000
University Honors	2000
University of Michigan Dean's List	1999, 2000, 2001
Cranbrook Kingswood Prize Program Award	1996, 1997, 1998, 1999

Patents

Issued
- C. J. Alpert, Z. Li, M. D. Moffitt and D. A. Papa "Method for Incremental, Timing-driven, Physical-synthesis using Discrete Optimization," November 2007
- C. J. Alpert, Z. Li, T. Luo, D. A. Papa and C. N. Sze, "Improved Method for Incremental, Timing-driven, Physical-synthesis Optimization Under a Linear Delay Model," November 2007

Filed
- C. J. Alpert, A. K. Karandikar, Z. Li, G.-J. Nam, D. A. Papa and C. N. Sze, "Method for Incremental, Timing-driven, Physical-synthesis Optimization," September 2007
- C. J. Alpert, Z. Li, D. A. Papa and C. N. Sze, "Methods for Optimal Timing-driven Cloning under a Linear Delay Model," November 2007
- M. D. Moffitt and D. A. Papa, "Method for Bounded Transactional Timing Analysis," June 2008
- C. J. Alpert, Z. Li, G.-J. Nam, D. A. Papa, C. N. Cze and N. Viswanathan, "A Method for Clock Optimization with Local Clock Buffer Control Optimization," November 2010
- C. J. Alpert, Z. Li, G.-J. Nam, D. A. Papa, C. N. Cze and N. Viswanathan, "Latch Clustering with Proximity Constraints to the Latch Drivers," November 2010

Pending
- J. Hopkins, D. A. Papa and S. I. Ward, "Decoupling Capacitor Insertion using Hypergraph Connectivity Analysis," (to be filed)
- W. R. El-Essawy, D. A. Papa and J. A. Roy, "A Method to Minimize the Required Maximum Link Capacity for Three-Dimensional Compute Node Interconnect Routing," (to be filed)
- W. R. El-Essawy, D. A. Papa and J. A. Roy, "A method to Automatically Route Supercompute Interconnect," (to be filed)
- C. J. Alpert, Z. Li, G.-J. Nam, D. A. Papa, C. N. Sze, N. Viswanathan and B. C. Wilson, "Improved Accuracy Pin-Slew Mode for Gate Delay Calculation," (to be filed)

Publications

In Books
- D. A. Papa and I. L. Markov, "Hypergraph Partitioning and Clustering," in Approximation Algorithms and Metaheuristics, T. Gonzalez, ed.; CRC Press, 2007, in print.
- J. A. Roy, D. A. Papa and I. L. Markov, "Capo: Congestion-aware Placement for Standard-cell and RTL Netlists with Incremental Capability," in Modern Circuit Placement: Best Practices and Results, G.-J. Nam and J. Cong, eds; Springer, 2007.

In Journals
- D. A. Papa, M. D. Moffitt, C. J. Alpert and I. L. Markov, "Speeding Up Physical Synthesis with Transactional Timing Analysis," *IEEE Design and Test of Computers*, September 2010.

- K.-H. Chang, D. A. Papa, I. L. Markov, V. Bertacco, "Invers: An Incremental Verification System with Circuit Similarity Metrics and Error Visualization," *IEEE Design and Test of Computers*, vol. 26, no. 2, pp. 34-43, March 2009.
- D. A. Papa, T. Luo, M. D. Moffitt, C. N. Sze, Z. Li, G.-J. Nam, C. J. Alpert and I. L. Markov, "RUMBLE: An Incremental, Timing-driven, Physical-synthesis Optimization Algorithm," *IEEE Trans. on Computer-Aided Design*, vol. 27, no.12, pp. 2156-2168, December 2008.
- J. A. Roy, D. A. Papa, I. L. Markov, "Fine Control of Local Whitespace in Placement," *VLSI Design*, vol. 2008, article 517919, 10 pp. DOI:10.1155/2008/517919.
- J. A. Roy, S. N. Adya, D. A. Papa and I. L. Markov, "Min-cut Floorplacement," *IEEE Trans. on Computer-Aided Design*, vol.25, no.7, pp. 1313-1326, July 2006.

Publications

In Conferences

- S. I. Ward, D. A. Papa, Z. Li, C. N. Sze, C. J. Alpert and E. Swartzlander, "Quantifying Academic Placer Performance on Custom Designs" *Intl. Symposium on Physical Design (ISPD)* 2010.
- D. A. Papa, S. Krishnaswamy and I. L. Markov, "SPIRE: A Retiming-based Physical-Synthesis Transformation System," *Intl. Conference on Computer Aided Design (ICCAD)* 2010, pp. 373 - 380.
- Z. Li, D. A. Papa, C. J. Alpert, S. Hu, W. Shi, C. N. Sze and Y. Zhou "Ultra-Fast Interconnect Driven Cell Cloning for Minimizing Critical Path Delay," *Intl. Symposium on Physical Design (ISPD)* 2010, pp. 75-82.
- T. Luo, D. A. Papa, Z. Li, C. N. Sze, C. J. Alpert and D. Z. Pan, "Pyramids: An Efficient Computational Geometry-based Approach for Timing-driven Placement," *Intl. Conference on Computer Aided Design (ICCAD)* 2008, pp. 204-211. (best paper award finalist)
- M. D. Moffitt, D. A. Papa, Z. Li and C. J. Alpert "Path Smoothing via Discrete Optimization," *Design Automation Conference (DAC)* 2008, pp. 724-727.
- D. A. Papa, T. Luo, M. D. Moffitt, C. N. Sze, Z. Li, G.-J. Nam, C. J. Alpert and I. L. Markov, "RUMBLE: An Incremental, Timing-driven, Physical-synthesis Optimization Algorithm," *Intl. Symposium on Physical Design (ISPD)* 2008, pp. 2-9.
- K.-H. Chang, D. A. Papa, I. L. Markov and V. Bertacco, "InVerS: An Incremental Verification System with Circuit Similarity Metrics and Error Visualization," *Proc. Intl. Symposium on Quality Electronic Design (ISQED)* 2007, pp. 487-492.
- J. A. Roy, D. A. Papa, A. N. Ng, I. L Markov, "Satisfying Whitespace Requirements in Top-down Placement," *Proc. Int'l Symp. on Physical Design (ISPD)* 2006, pp. 206-208.
- J. A. Roy, D. A. Papa, S. N. Adya, H. H. Chan, J. F. Lu, A. N. Ng, I. L. Markov, "Capo: Robust and Scalable Open-Source Min-cut Floorplacer," *Intl. Symposium on Physical Design (ISPD)* 2005, pp. 224-227.
- D. A. Papa, I. L. Markov and P. Chong, "Utility of OpenAccess in Academic Research," *Proc. Asia and South Pacific Design Automation Conference (ASPDAC)* 2006, pp. 440-441.
- Z. Xiu, D. Papa, P. Chong, A. Kuehlmann, R. Rutenbar, I. Markov, "Early Research Experience with OpenAccess Gear: An Open Source Development Environment for Physical Design," *Intl. Symposium on Physical Design (ISPD)* 2005, pp. 94-100.
- S. N. Adya, S. Chaturvedi, J. A. Roy, D. A. Papa and I. L. Markov, "Unification of Partitioning, Floorplanning and Placement," *Intl. Conf. Computer-Aided Design (ICCAD)* 2004, pp. 550-557
- D. A. Papa, S. N. Adya and I. L. Markov, "Constructive Benchmarking for Placement," *Great Lakes Symp. on VLSI (GLSVLSI)* 2004, pp. 113-118.

Invited Talks

- D. A. Papa and I. L. Markov, "Fast Simulation and Equivalence Checking Using OpenAccess," *the Open Access conference (OA)*, November 2006.
- D. A. Papa, I. L. Markov and P. Chong, "Utility of OpenAccess in Academic Research," Proc. *Asia and South Pacific Design Automation Conference (ASPDAC)* 2006, pp. 440-441.
- J. A. Roy, D. A. Papa, J. F. Lu, A. N. Ng, I. L. Markov, "Tool Development For Multi-Million Gate Designs," *workshop on Electronic Design Processes (EDP)*, 2005.

In Workshops

- D. A. Papa, M. D. Moffitt, C. J. Alpert and I. L. Markov, “Bounded Transactional Timing Analysis,” *TAU* 2010.
- K.-H. Chang, D. A. Papa, I. L. Markov and V. Bertacco, “Fast Simulation and Equivalence Checking Using OAGear,” *Intl. Workshop on Logic Synthesis (IWLS)* 2006, pp. 270-271.

Reviews

Journals

- IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD).