

# Gaurav Chadha

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## RESEARCH INTERESTS

My research interests lie in the design of runtime systems, architecture and compiler level solutions for the performance improvement of multi-threaded applications and dynamically typed languages. Designing multi-threaded applications that can efficiently utilize the underlying hardware resources for high performance is a non-trivial task. My work focuses on finding innovative hardware and software solutions for controlling the concurrency of multi-threaded applications.

Currently, I am working on performance improvement of dynamically typed languages that have become the language of choice for web applications. This work looks at software changes and hardware modifications that can benefit both the interpreted and JIT compiled parts of javascript engines.

## EDUCATION

**University of Michigan, Ann Arbor** Sep 2009 - present  
Ph.D. in Computer Science and Engineering  
Advisors: Prof. Satish Narayanasamy, Prof. Scott Mahlke

**University of Michigan, Ann Arbor** Sep 2009 - May 2011  
M.S. in Computer Science and Engineering  
GPA: 7.862 / 9.00 (A = 8.0)

**Indian Institute of Technology Guwahati** Aug 2005 - May 2009  
B.Tech in Computer Science and Engineering  
GPA: 8.89 / 10.00

## RESEARCH EXPERIENCE

**University of Michigan, Ann Arbor** Jan 2010 - Sep 2011  
**Mentors:** Prof. Satish Narayanasamy, Prof. Scott Mahlke  
**Work:** This project involves controlling the number of threads of a multi-threaded program at runtime to improve performance. The optimal number of threads to run in a multi-threaded program varies not only for different inputs but also at runtime, as the program goes through different “phases” during execution exhibiting different characteristics or due to a change in available system resources, which motivates this project. Considerable configurability of the machine and system setup is required in this project for which I use a full system timing simulator FeS2 (<http://fes2.cs.uiuc.edu/>) that uses Simics for functional correctness. I use the most recent version of the memory model Ruby from Wisconsin GEMS instead of the one shipped with FeS2 which lacks support for modelling CMPs. This work is under submission at SPAA 2012.

**University of Michigan, Ann Arbor** Aug 2009 - Aug 2010  
**Mentors:** Prof. Satish Narayanasamy, Prof. Scott Mahlke, Prof. Jeffrey Fessler  
**Work:** Performance optimization (SIMDization, etc.) of medical imaging applications (CT image reconstruction) for Intel Larrabee using its very wide SIMD units. We also studied the effects of prefetching and influencing cache line eviction on streaming programs on Intel Larrabee and optimized programs using these. Support for generating code compatible for compilation on Intel Larrabee was implemented in the StreamIt compiler.

- INTERNSHIP**      **High Performance Computing lab, Georgia Tech**      May 2008 - Jul 2008  
**Mentor:** Prof. Richard Vuduc, Prof. David Bader  
**Work:** Improved performance of financial services applications of R (<http://www.r-project.org>), an open source software environment for statistical computing and graphics, for IBM Cell B.E. which involved parallelization, SIMDization, optimizing DMA accesses, eliminating branches and efficient division of work among Cell's heterogeneous cores. I also worked on optimization of Sparse Matrix Vector Multiplication (SpMV) on the Cell B.E.
- UNDERGRADUATE THESIS**      **Indian Institute of Technology Guwahati**      Aug 2008 - April 2009  
**Mentor:** Prof. Sajith Gopalan  
**Work:** I worked on performance optimization of applications for the Cell B.E. and Nvidia GPUs, thus providing a comparison on the different sets of optimization strategies that need to be employed on the two different architectures. Applications included SpMV (hard to optimize because of sparsity of data), Discrete Wavelet Transform and Dense Matrix Multiplication (easiest to optimize).
- HONORS AND AWARDS**
- Riethmiller Fellowship Award, 2010, 2011 and 2012.
  - DAAD (German Academic Exchange Service) scholarship for a research internship in Germany, 2008.
  - Selected for the CRUISE program in Georgia Tech, 2008.
  - Placed among the top 10% students in the centre in the National Standard Examination in Physics 2004-2005 conducted by the Indian Association of Physics Teachers.
  - Certificate of Merit in the Invitational World Youth Math Intercity Competition (IWYMIC) 2002.
- TECHNICAL SKILLS**      **Compilers:** LLVM, StreamIt
- Architectural Simulators:** Simics, FeS2
- Programming Languages:** C, C++, Java, Verilog, Bash, Python
- Other Tools:** PIN, Latex
- RELEVANT GRADUATE COURSEWORK**
- University of Michigan, Ann Arbor**
- EECS 470: Advanced Computer Architecture (A)
  - EECS 583: Advanced Compilers (A)
  - EECS 570: Parallel Computer Architecture (A+)
  - EECS 573: Microarchitecture (A-)
  - EECS 598: Ubiquitous Parallelism (A+)
- Indian Institute of Technology Guwahati**
- CS 523: Advanced Computer Architecture (A)
  - CS 526: CAD for VLSI (A+)
- EXPERIENCE**
- Reviewed paper submissions for several architecture and compiler conferences: MICRO, ASPLOS, HPCA, ISCA, PACT, CASES, ICCD, CGO, PLDI.
  - Graduate Student Instructor for EECS 370 - Introduction to Computer Organization.