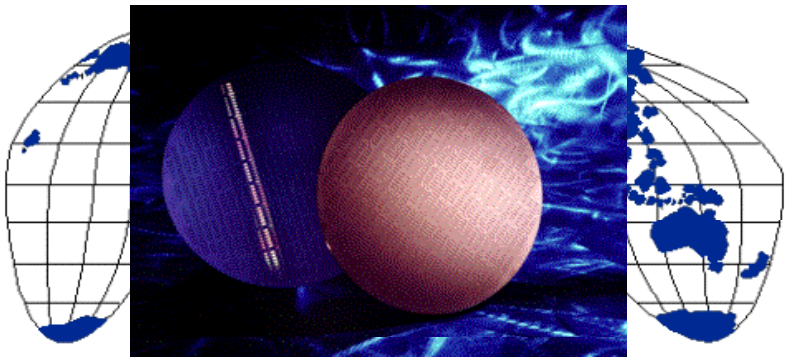
Paradigm Shift in Semiconductor Business and Manufacturing



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Sony Corporation

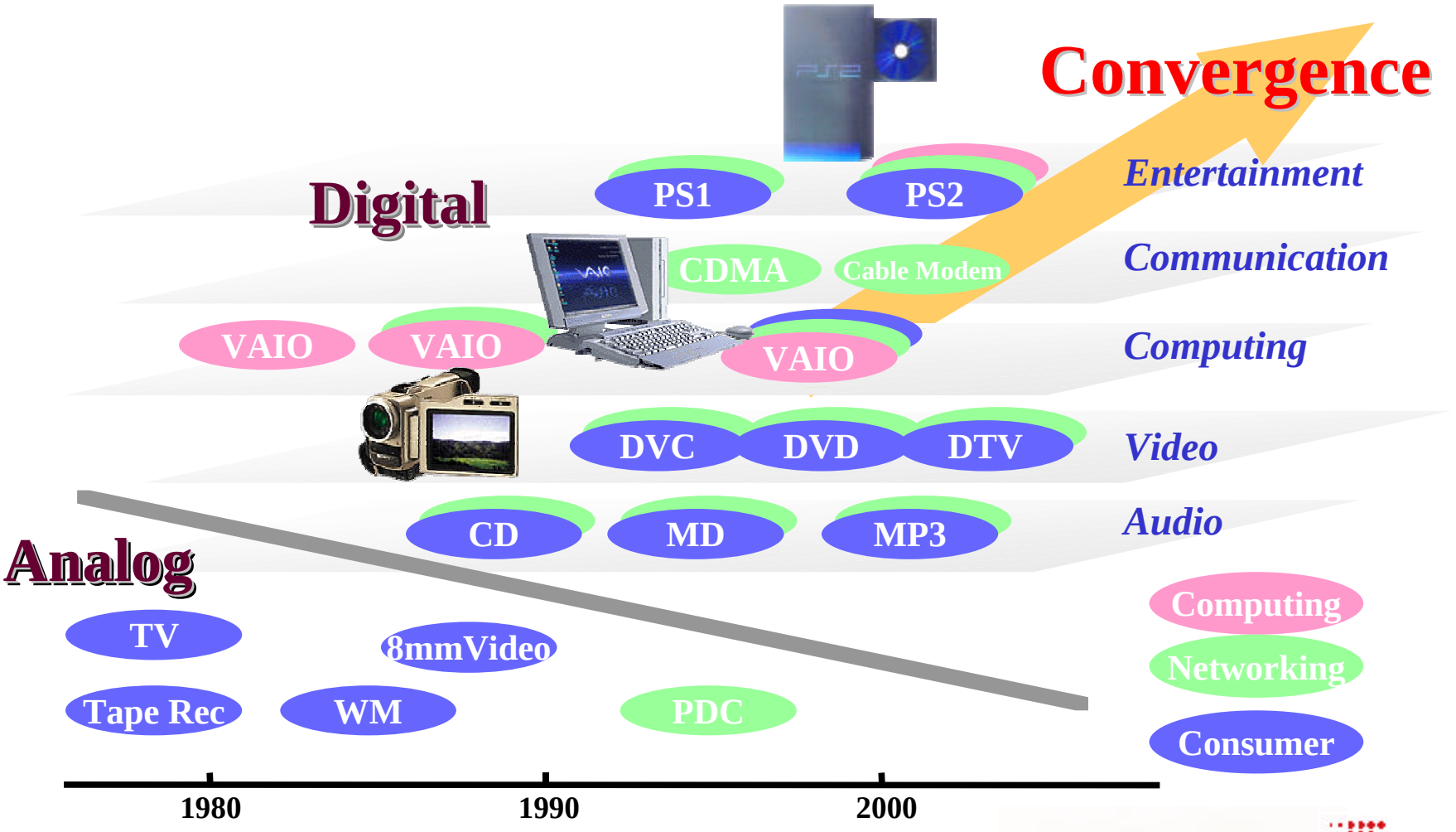
SONY

Contents

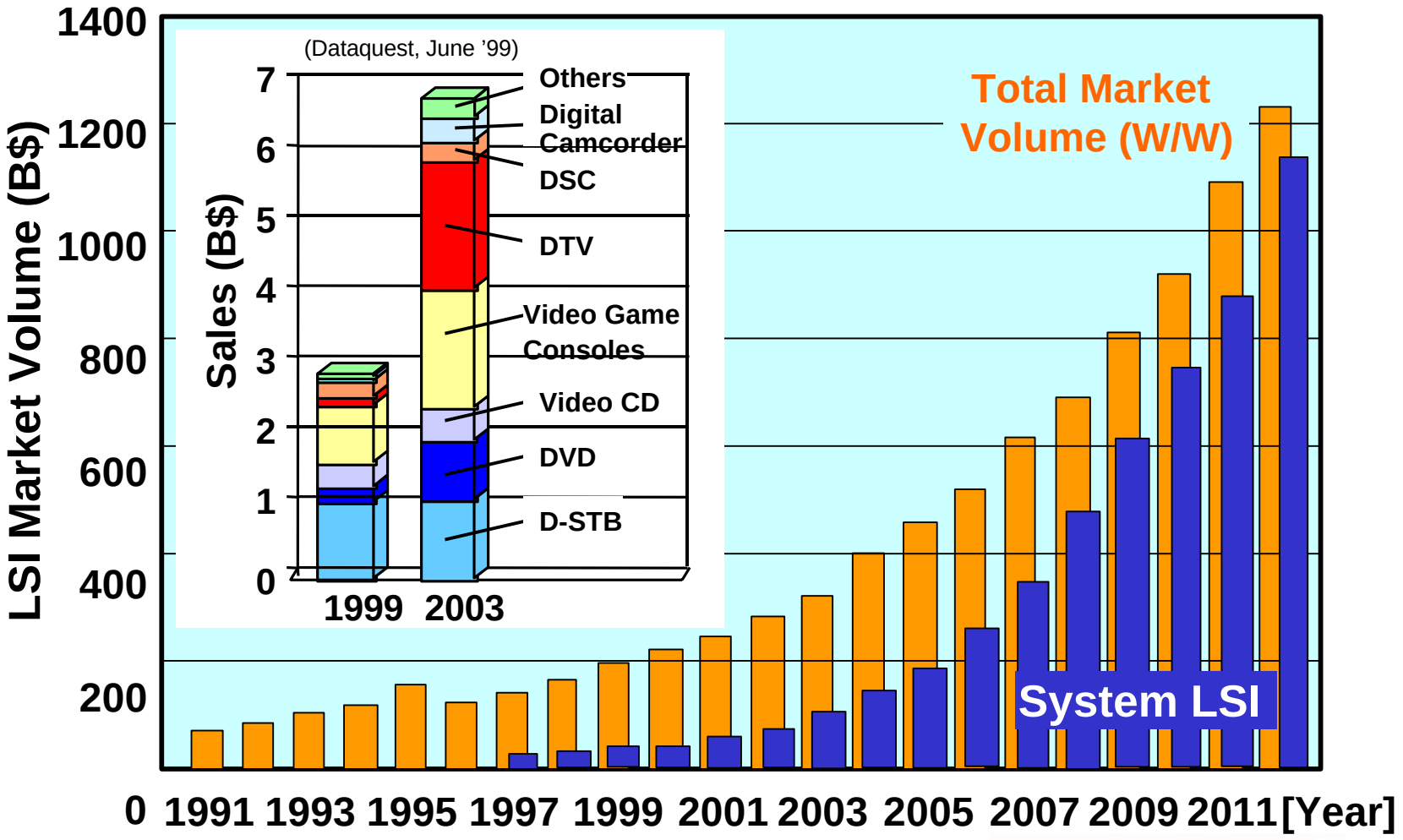
- Paradigm Shift in Semiconductor Business
- Sony's Lithography Roadmap
- Flexible Manufacturing Line
- Conclusion

Paradigm Shift through Digitalization

Digitalization creates a new market combining Consumer, Network and PC applications.



Paradigm Shift in Semiconductor Products



Ref. Nikkei Microelectronics (1999)

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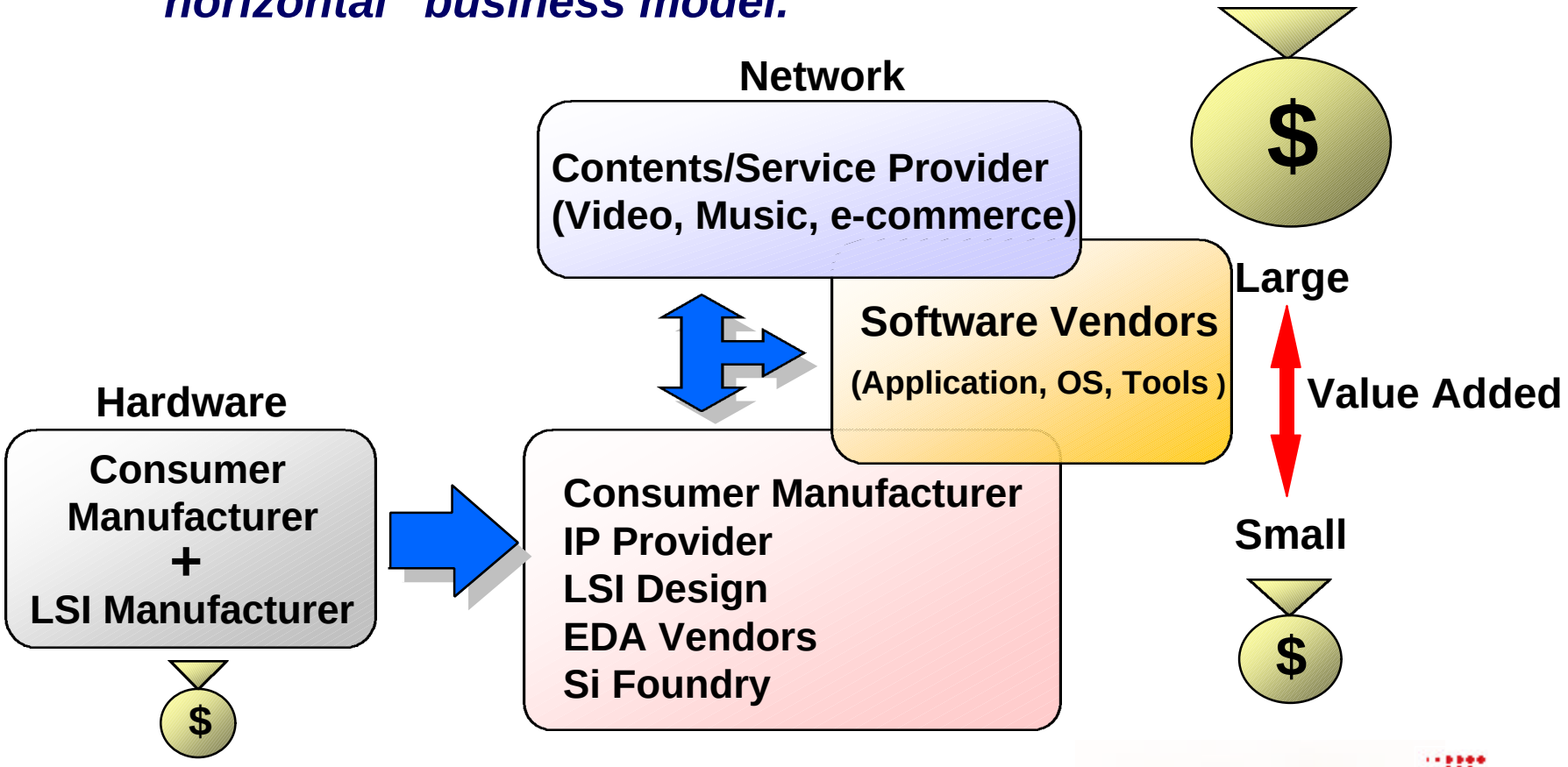
Impact of Digitalization on LSI

- Large scale system LSI (SOC) with embedded DRAM
- Flash memory becomes major storage media
- Consumer products are merging with network and PC
- Software and security play more important role

Shift in Values in Electronics

- Network oriented business lowers the status of hardware.
- High specialization and standardization result in "horizontal" business model.



PlayStation 2

Fusion of Graphics, Audio/Video and PC

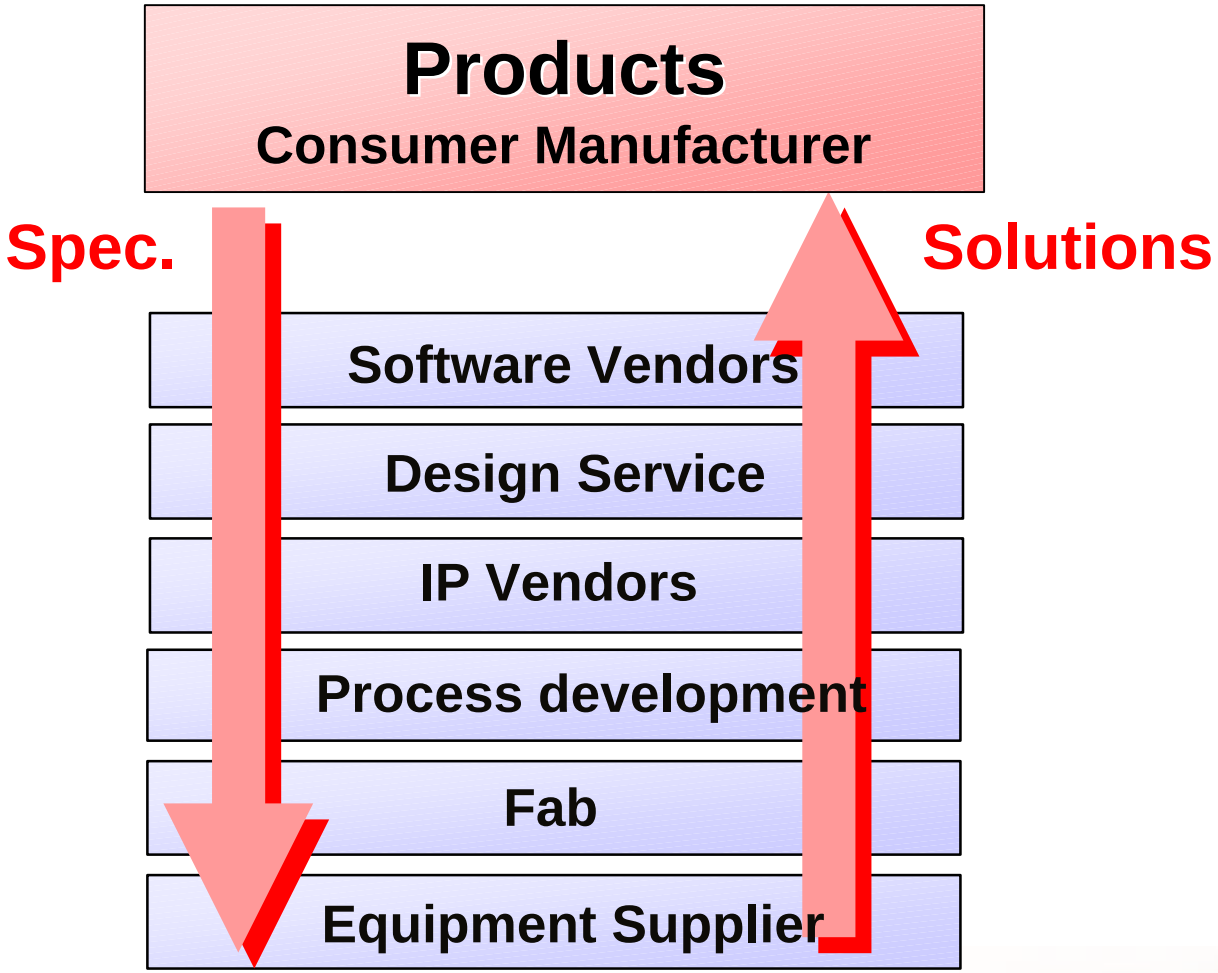
128bit CPU: “Emotion Engine”
Clock 300MHz
Main Memory 32MB(Direct RDRAM)

Graphics : “Graphic Synthesizer”
Clock 150MHz
Embedded Cache VRAM 4MB

SPU
I/O Processor
CD-ROM Drive: X24
DVD-ROM Drive: X4

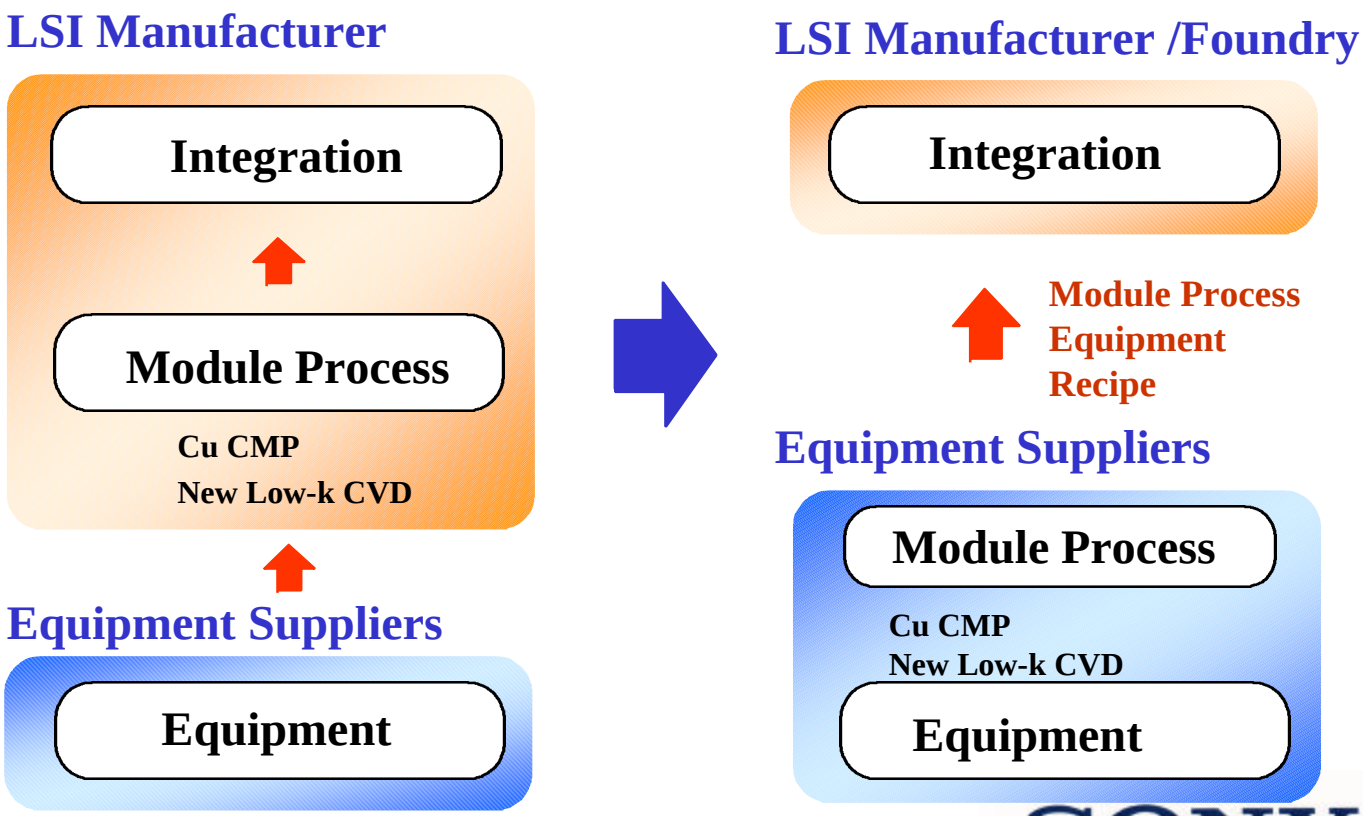
New Vertical Integration

Products demand new vertical integration with horizontal business model.



Module Processes by Equipment Suppliers

Saves cost/time/risk of process development by introduction of module processes optimized by equipment suppliers.



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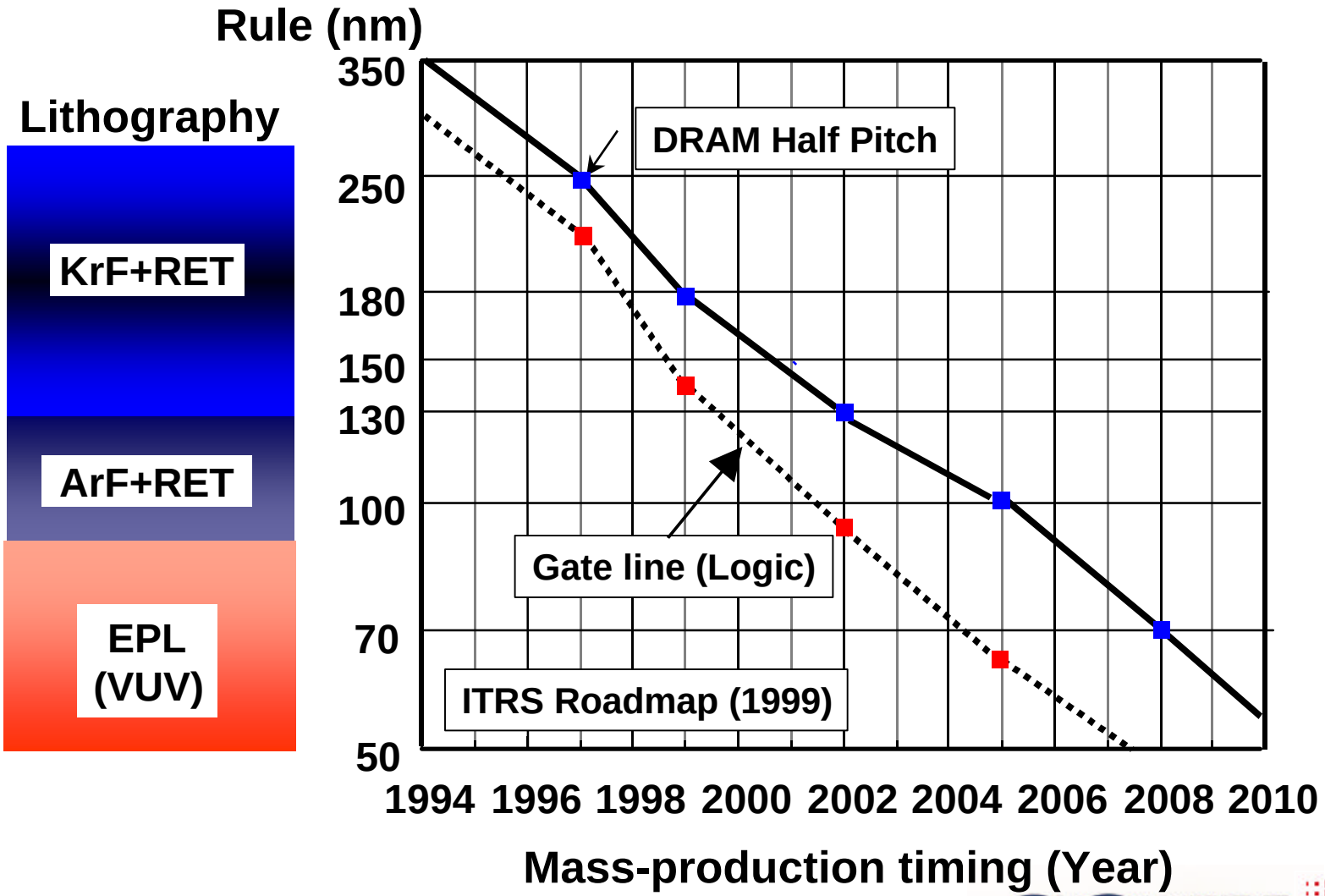
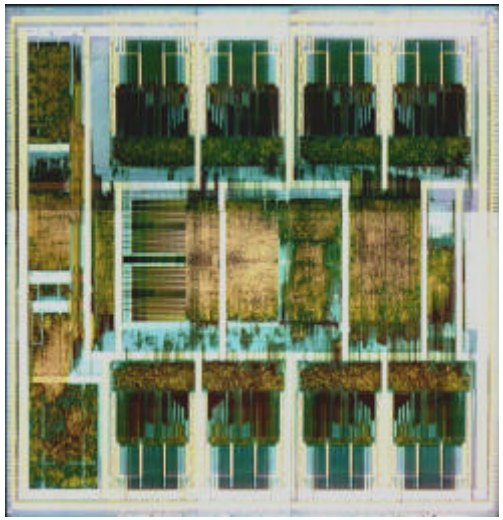
Sony's Lithography Strategy



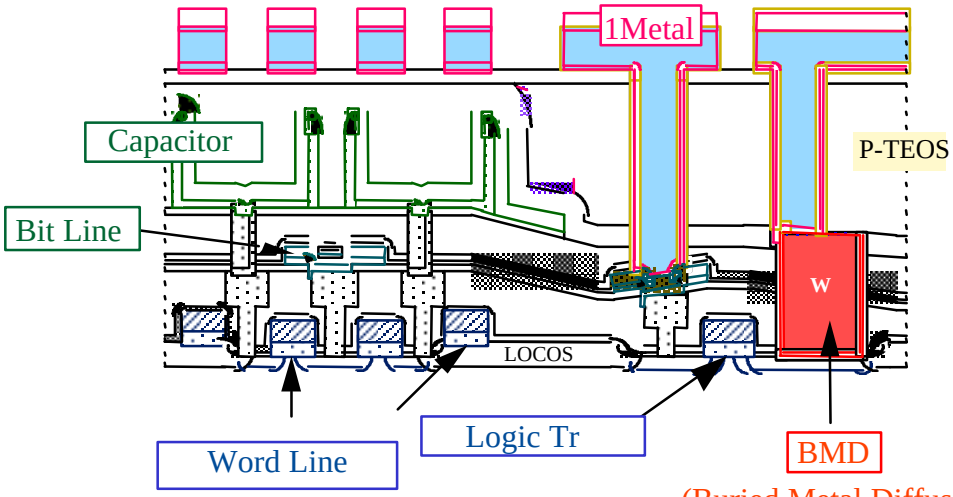
“Graphic Synthesizer”

The Most Advanced Embedded DRAM LSI



0.25um CMOS
4MB Embedded DRAM
42.7M Transistors
Clock150MHz
Band Width 48GBps
75M Polygon/sec
384 pin BGA

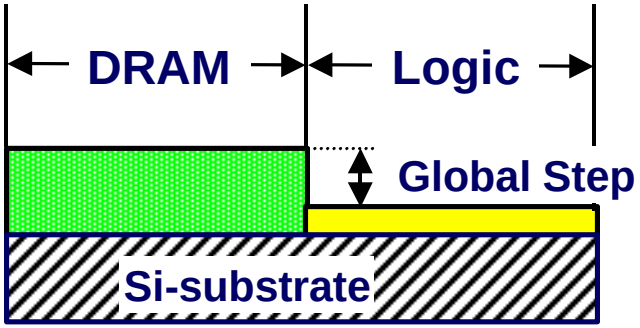
Cross sectional View



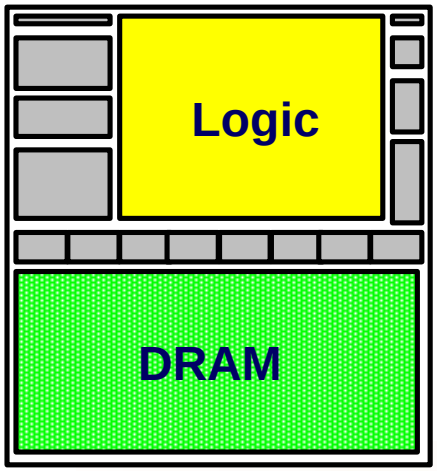
The Feature and Critical Issues of 130nm Emb-DRAM LSI Process

- The most advanced design rule to achieve high performance Tr
  -> Enhance resolution, and refine OPC system (speed, accuracy)
- Large variation in duty cycles
  -> Reduce iso – dense bias
- High global step
  -> Enlarge D.O.F
- High aspect hole process
  -> Enhance etching durability

<Side view>



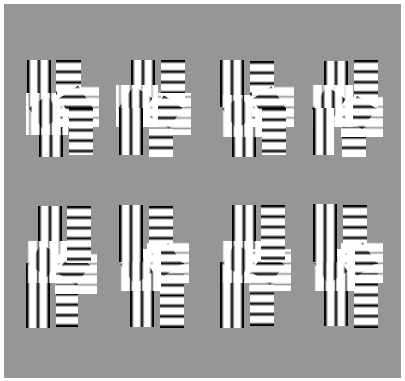
<Top view>



Resolution Enhancement Tech. to Sub-100nm

Double Exposure Levenson-PSM

Levenson (1-st exp.)

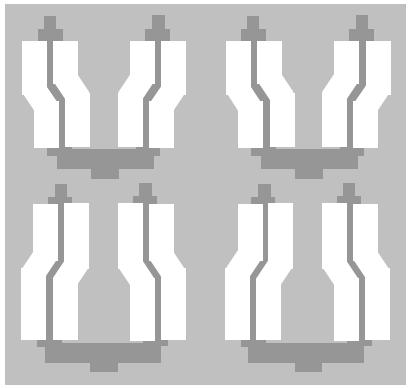


Cr

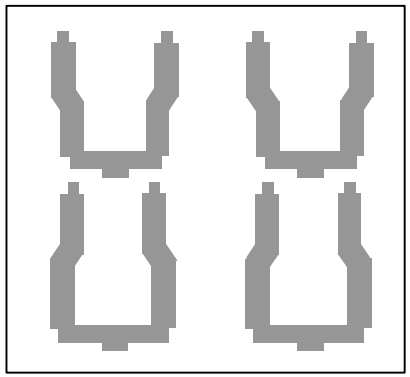
T-0deg

T-180deg

Levenson+Binary



Binary (2-nd exp.)

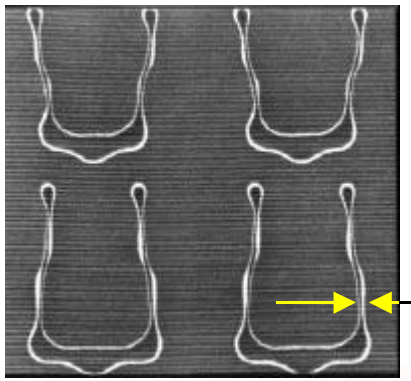


λ: 248nm

NA: 0.68

Illu: 1/2 Ann.

After Lithography



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Requirements for ArF Litho. to Below 100nm

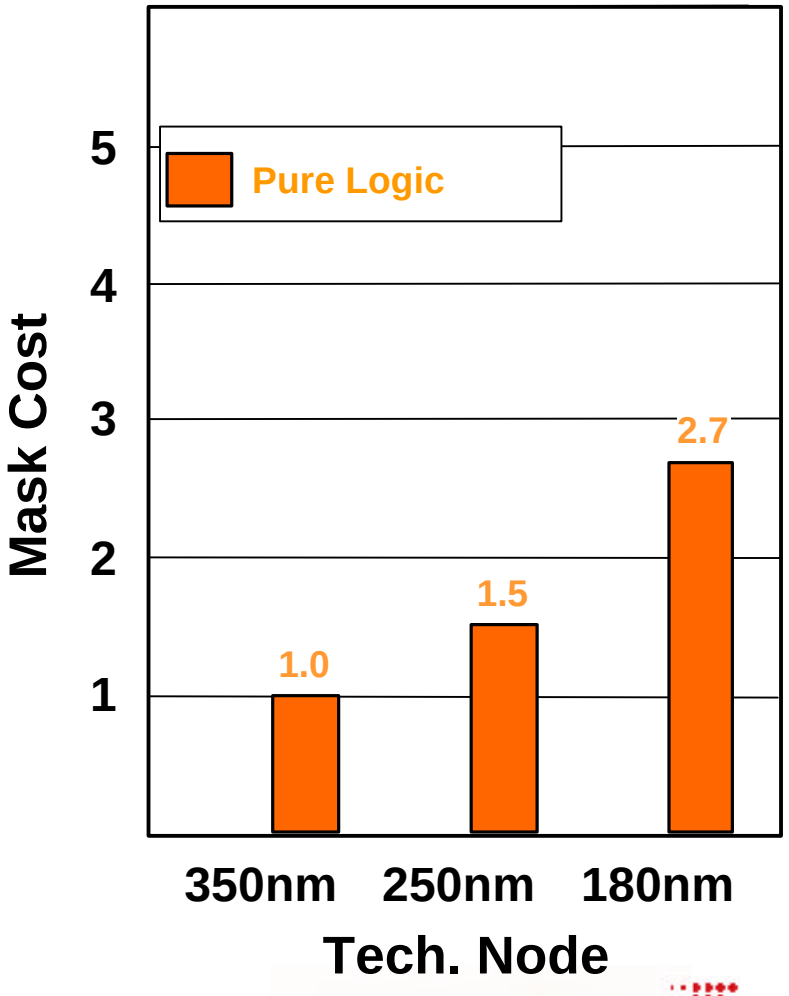
- **ArF exposure system**
  - **- High NA (>0.70), - Small Aberration, - Same performance in each machine,**
  - **- Reduce initial and running cost, - Stability including ArF laser,**
- **ArF resist**
  - **- Resolution**
    - **- Gate: 100nm logic gate (iso, semi-iso), DRAM(gate 130nm)**
    - **- Contact: 150nm**
    - **- Edge roughness: <1nm**
  - **- Etching durability: aspect ratio>10 in contact process**
  - **- Defect density: none**
- **Mask**
  - **- High CD uniformity to get MEF 1.6 – 1.7**
  - **- Defect density: same as NTRS**
  - **- Grid size change: 5nm ->2nm**
  - **- High durability in transmittance and phase for ArF laser light and chemical damage**
  - **- High accuracy phase control**
  - **- Price and T.A.T**

Key Issues for Mask Cost Reduction

- **Critical issues**
  - Mask writer: throughput / price
  - Inspection tool: throughput / price
- **How to foster suppliers?**

  For 130nm era:
  - Cooperative work between supplier, consortium, and users.

  For below 100nm era:
  - World wide strong cooperation.



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Characteristics of System LSI Market

Needs new process development and production strategy optimized for system LSI market characteristics.

	MPU	DRAM	System LSI
Requirement	High Speed	Cost, Speed	Cost, Low Power, Functionality
Device	Logic	DRAM	Customized (Analog, Emb. DRAM)
Market Size	Large	Large	Medium
Production	Few Products/ High Volume	Few Products/ High Volume	Many Products/ Low Volume
KFS	**Early Introduction of Advanced Process**	Scale Merit	Q-TAT, Flexibility, IP

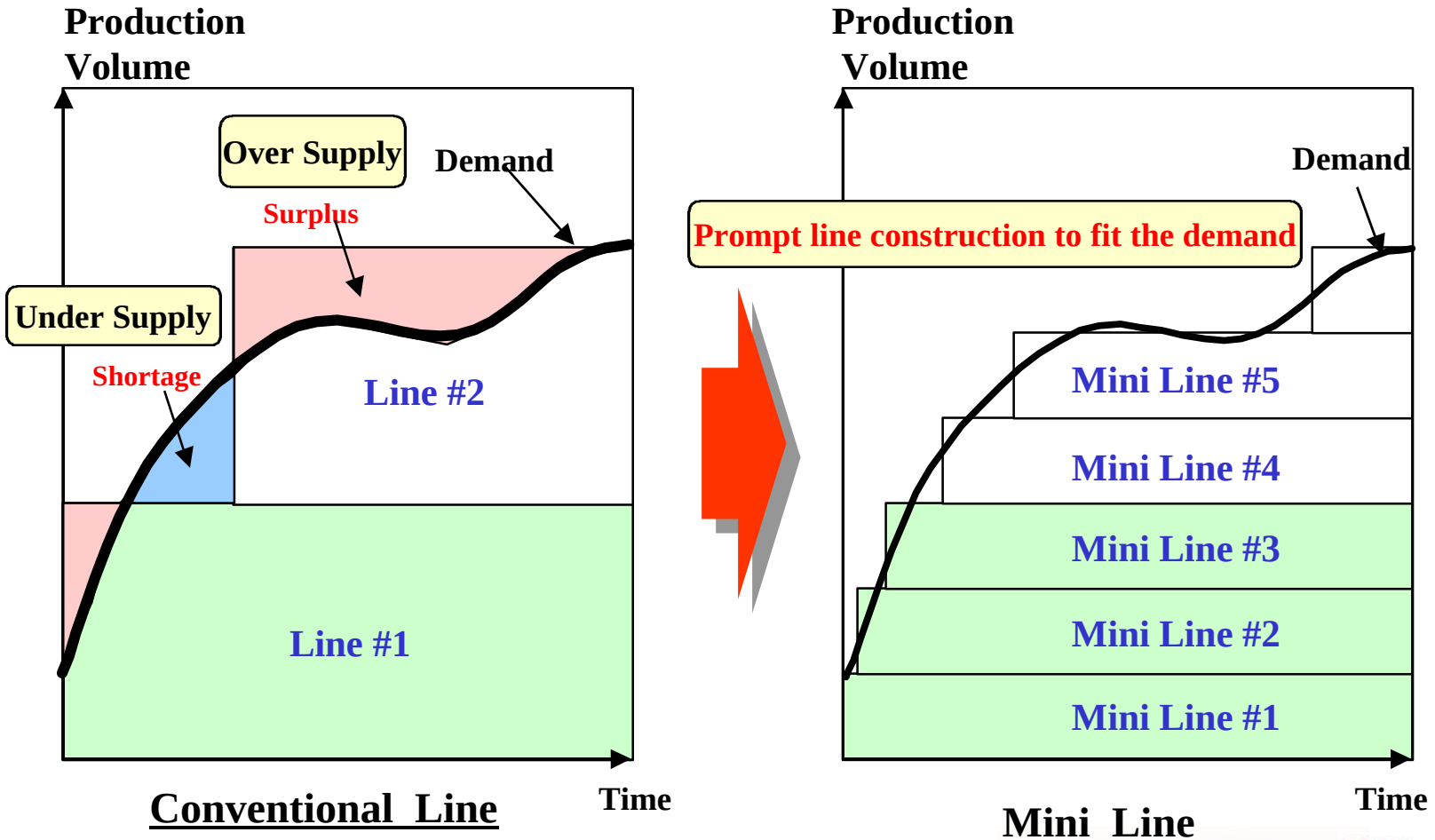
Products and Production Lines

Mini Lines (Scalable Lines) enable both flexibility and efficiency of capital investment.

Volume/Products	Low/Many Medium/Few High/Few
Memory, MPU	Large Line (Scale Merit)
System LSI	Multiple Mini Lines; Mini Line

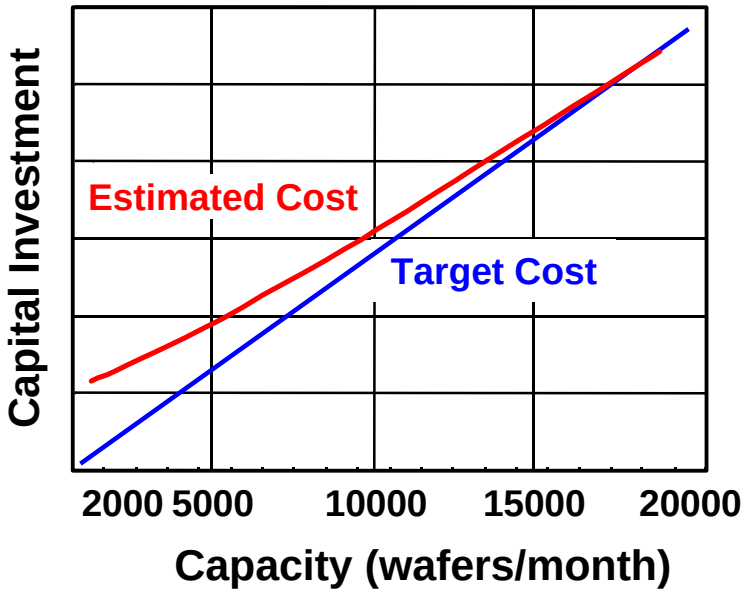
Mini Line: Concept

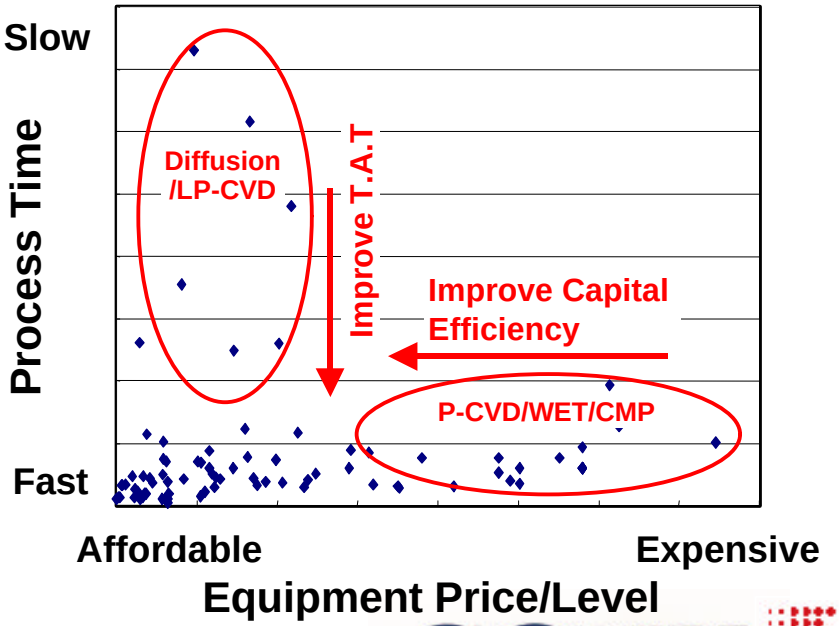
Well balanced wafer supply to market with multiple mini lines



To Realize Mini-line Concept…

- **Target**
  - Wafer Capacity: 1/3 - Capital Investment: 1/3 - TAT: A.S.A.P
- **Critical issues**
  - Efficiency in Capital Investment - T. A. T
- **Strategy**
  - Cooperation with Suppliers
  - Utilization The Small Number of Wafers per Lot





Conclusions

- The structure in electronics industry is changing….
- New business model for system LSI is needed.
  - Partnership through target product
- Development item in chip company itself should be focused.
  - Which item is common or specific?
  - Common module process solution by equipment suppliers and consortium
- Flexible mini line is needed.

Digital consumer with net working drive
New Technology and Business Scheme.