MOS Capacitor

EECS 320

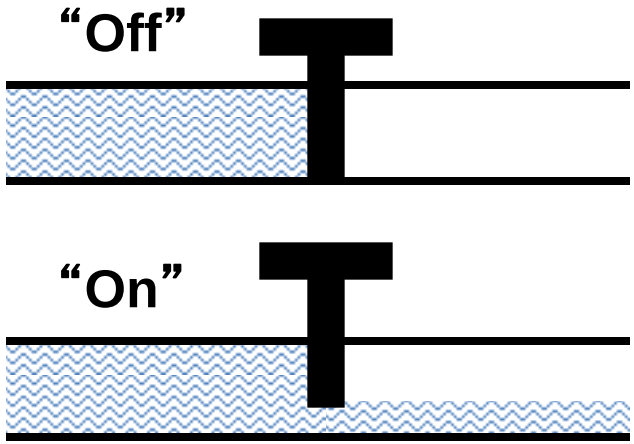
Introduction to Semiconductor Devices

Transistor

Goal: Control output with small input

Analogy: Valve controls water flow

Valve Controls Flow

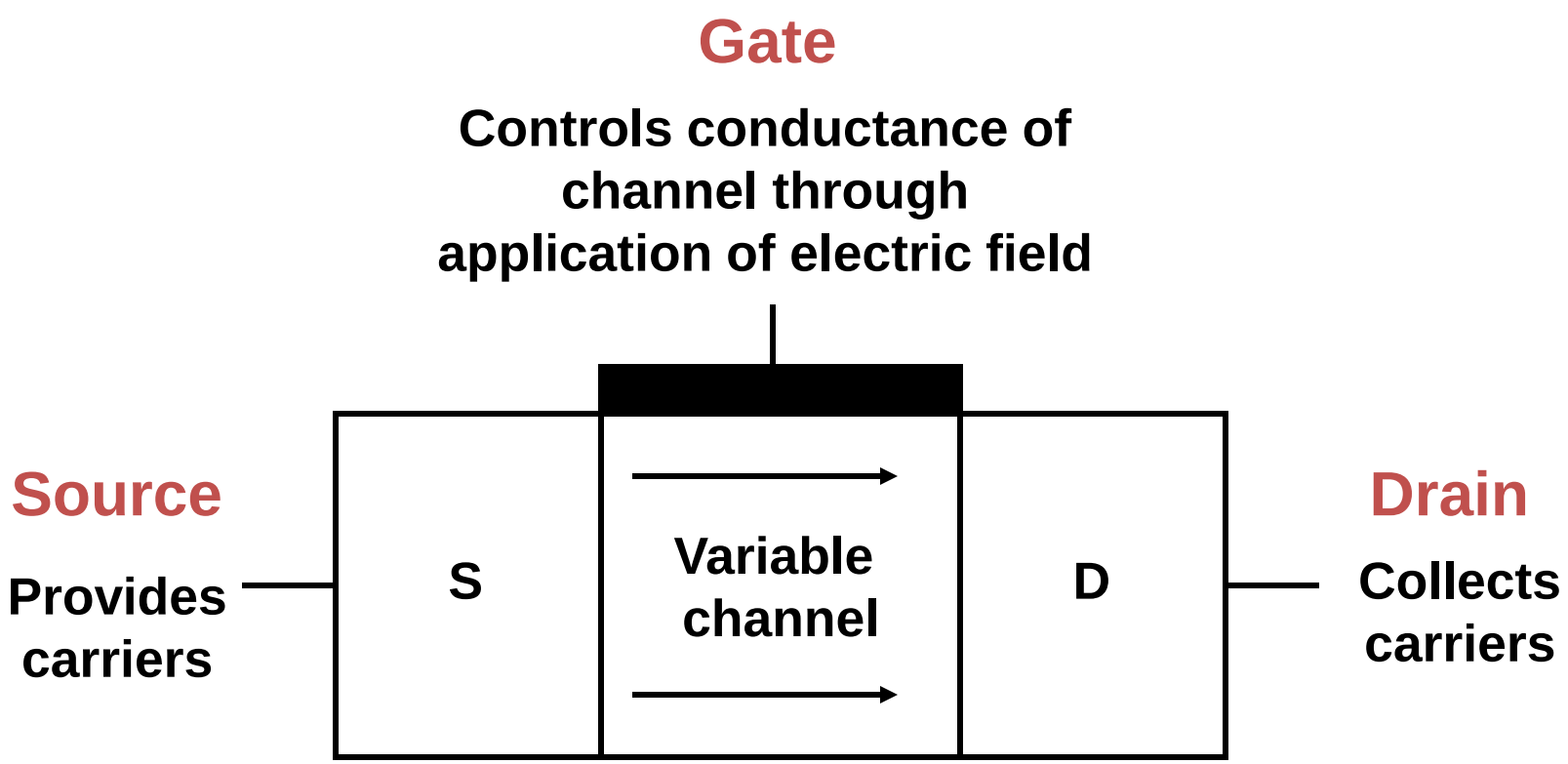


- Input controls aperature
- Output = water flow

Electronics analogy

- **Water flow = electron or hole current**
- **Valve = channel conductance controlled by electric field**

Field Effect Transistor Terminals

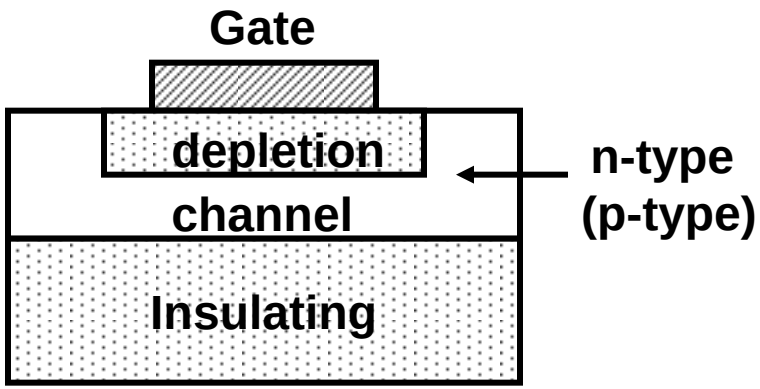


Control source to drain current with gate voltage

Gates For FETs

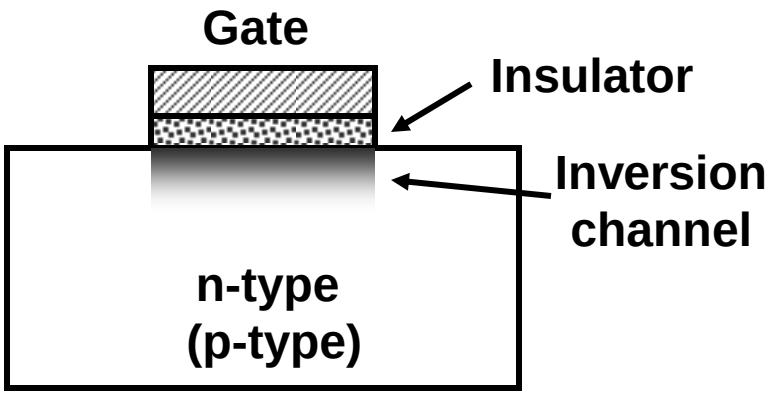
How do we control conductance of a channel?

Depletion



- Field controls depletion width, channel depth
- Reverse-bias p-n (JFET)
- Reverse-bias Schottky (MESFET)

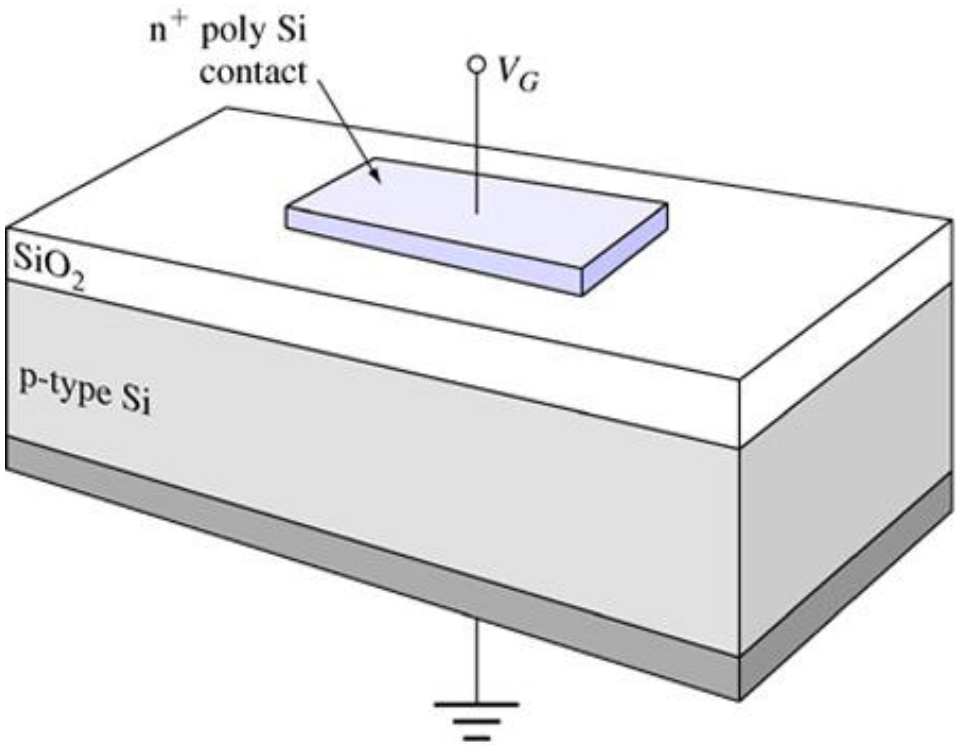
Inversion

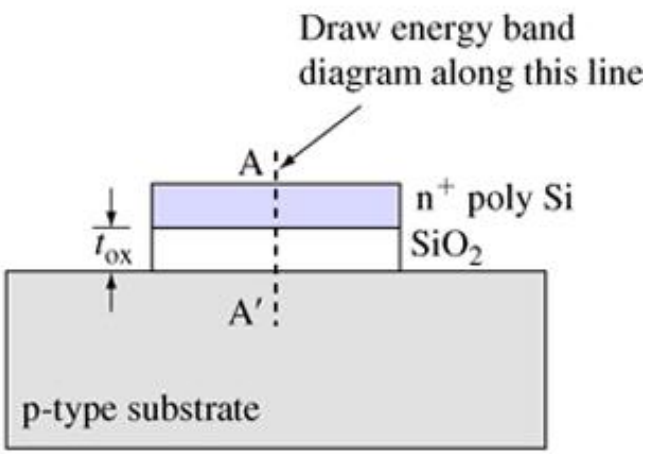


- Field inverts surface, controls surface charge density
- Metal-Insulator-Semiconductor (MISFET, MOSFET)

MOS Structure

Basis for controlling channel charge





SiO_2/Si – "Nature's Choice"

- Need: insulator with excellent interface to semiconductor
- Isolation between gate and semiconductor: voltage control over current flow through inversion layer

SiO_2 : **E_G = 9 V**, **$\varepsilon = 3.9\ \varepsilon_0$**

Si/SiO_2 interfaces may be achieved with interface state densities of $N=10^{11}\ cm^{-2}eV^{-1}$ (extremely small!)

http://www.ibm.com

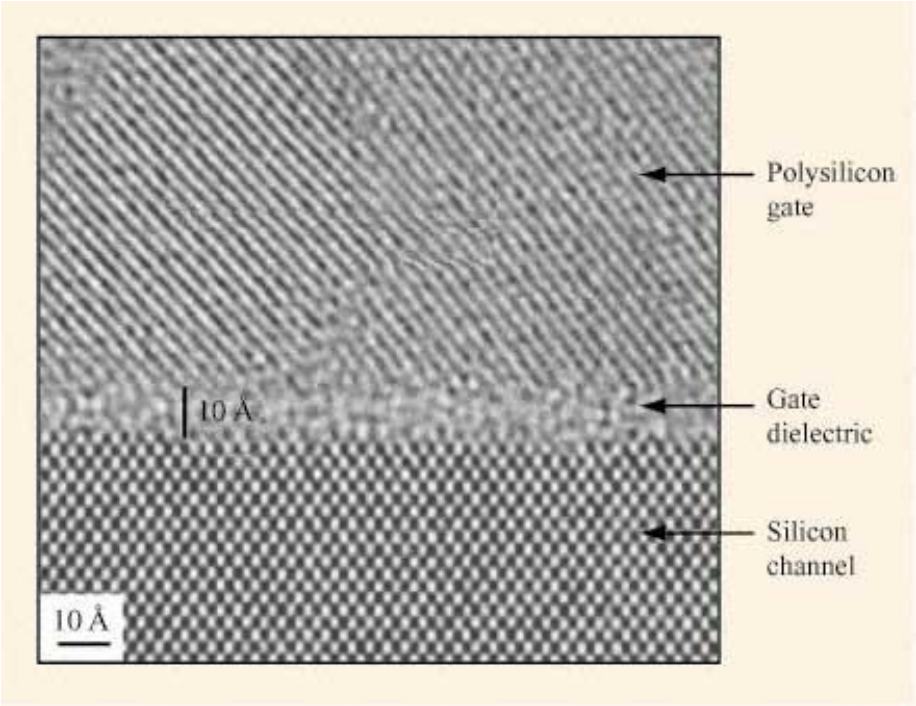


Figure 2

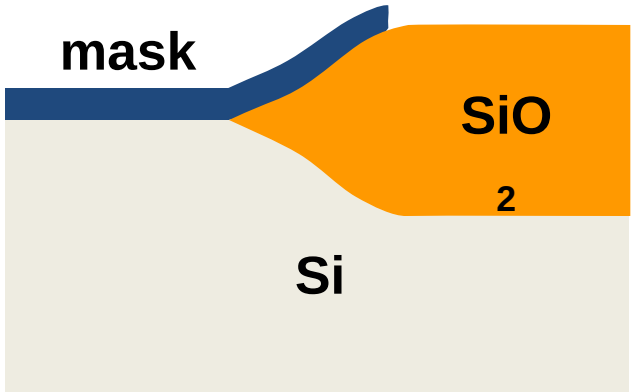
XTEM lattice image of the Si substrate, gate dielectric, and polysilicon for a 90-nm-technology-node device under development.

Thermal Oxidation

- Oxidation of silicon is controllable down to atomic layers
- "Wet" or "dry" thermal oxidation
- Selective oxidation useful for device integration
- Resulting oxide terminates ~48% of total thickness below original interface, ~52% above original interface

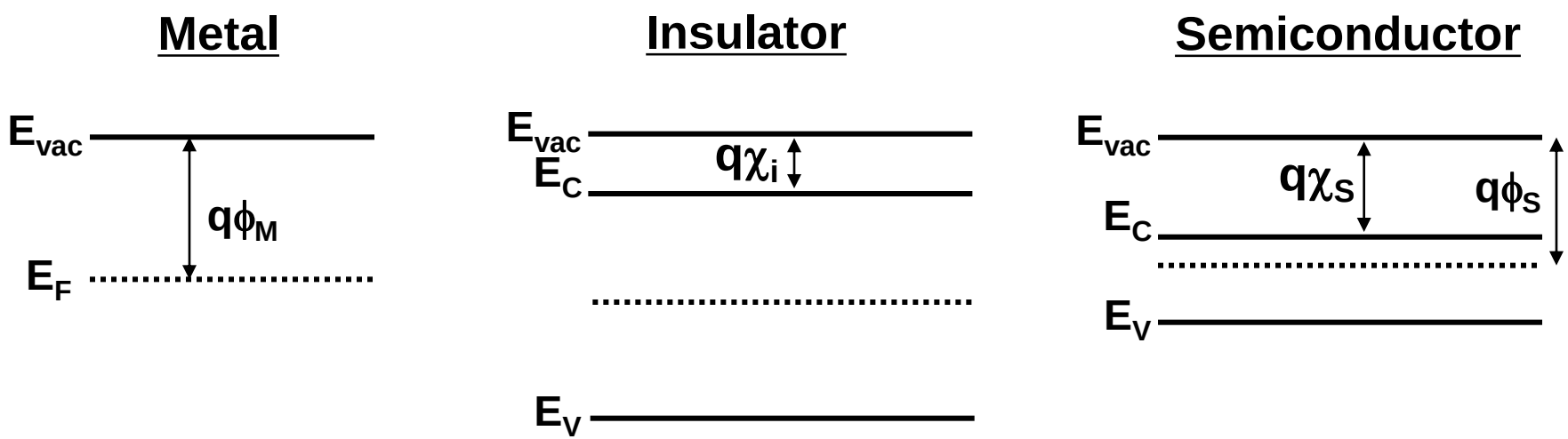
$$Si + O_2 \rightarrow SiO_2$$

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$



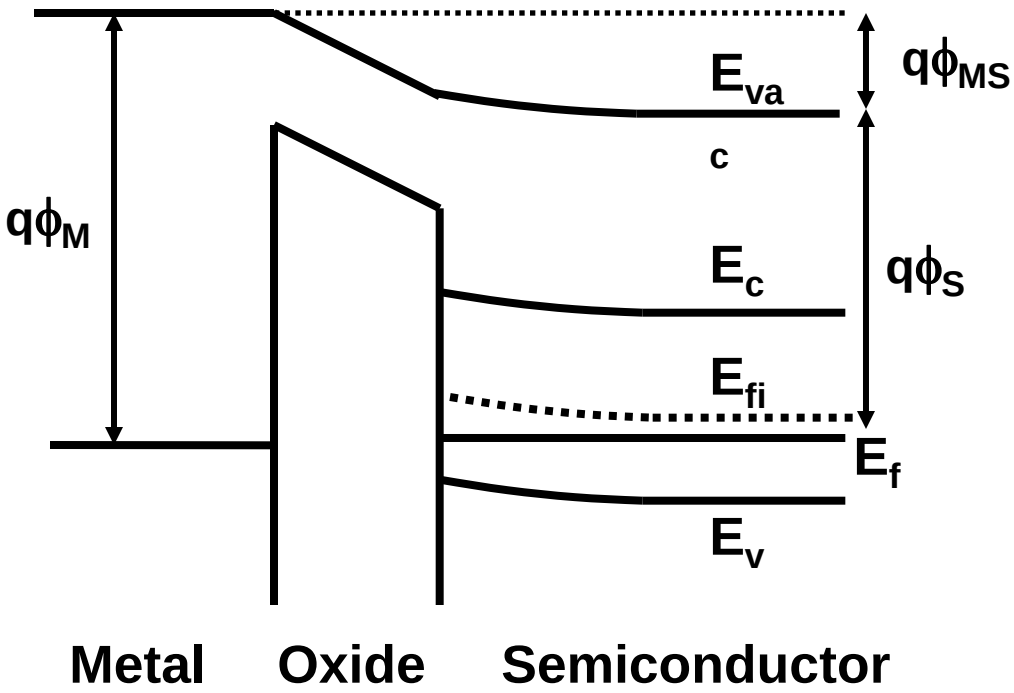
Insulator Band Diagram

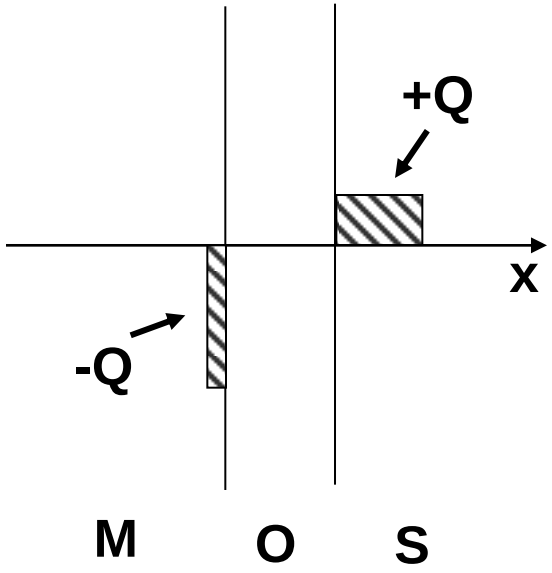
What does the energy band diagram look like for an insulator?



M-O-S Equilibrium Energy Band Diagram

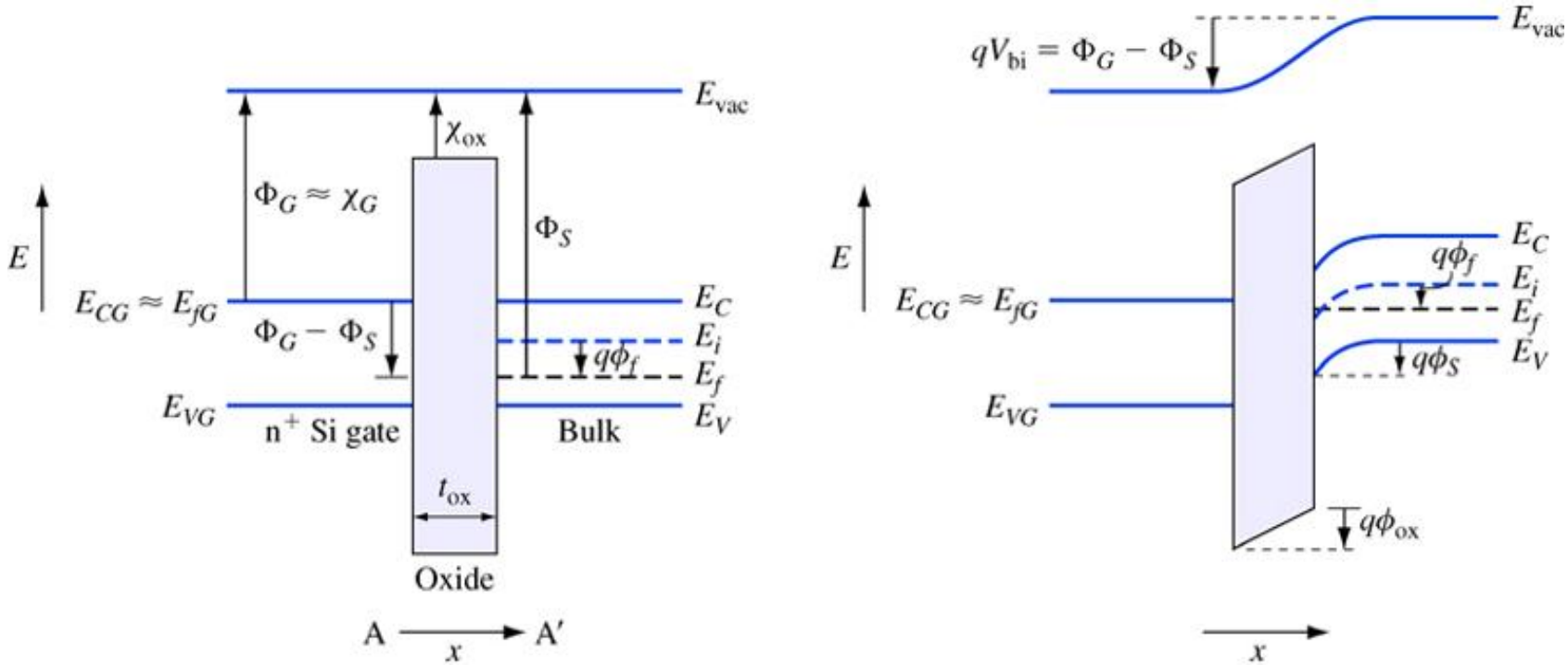
Equilibrium configuration depends on metal and semiconductor work function





Energy Band Diagram

Flat band and under bias



$$V_{bi} = -\frac{1}{q}\left|\Phi_G - \Phi_S\right| = \phi_{ox} + \phi_S$$

M-O-S / M-S Comparison

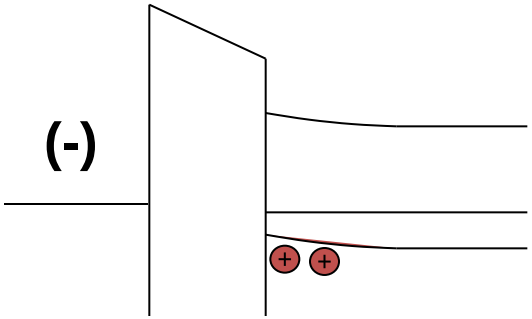
How does the M-O-S structure compare to the M-S structure?

Qualitatively, how do you expect the I-V characteristics to behave?

Band Diagram Change With Gate Bias

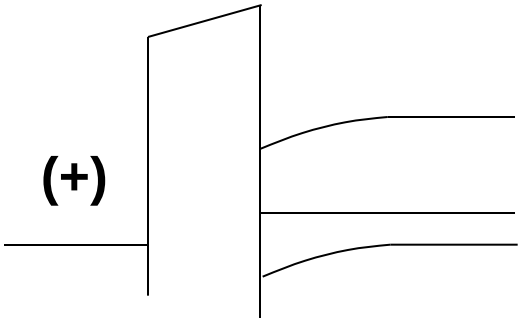
Charge at oxide-semiconductor interface changed by V_G (p-type substrate, NMOS)

Accumulation



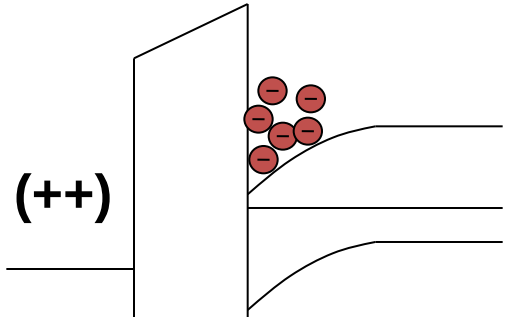
Accumulate holes at O-S interface

Depletion



Push holes away from O-S interface

Inversion



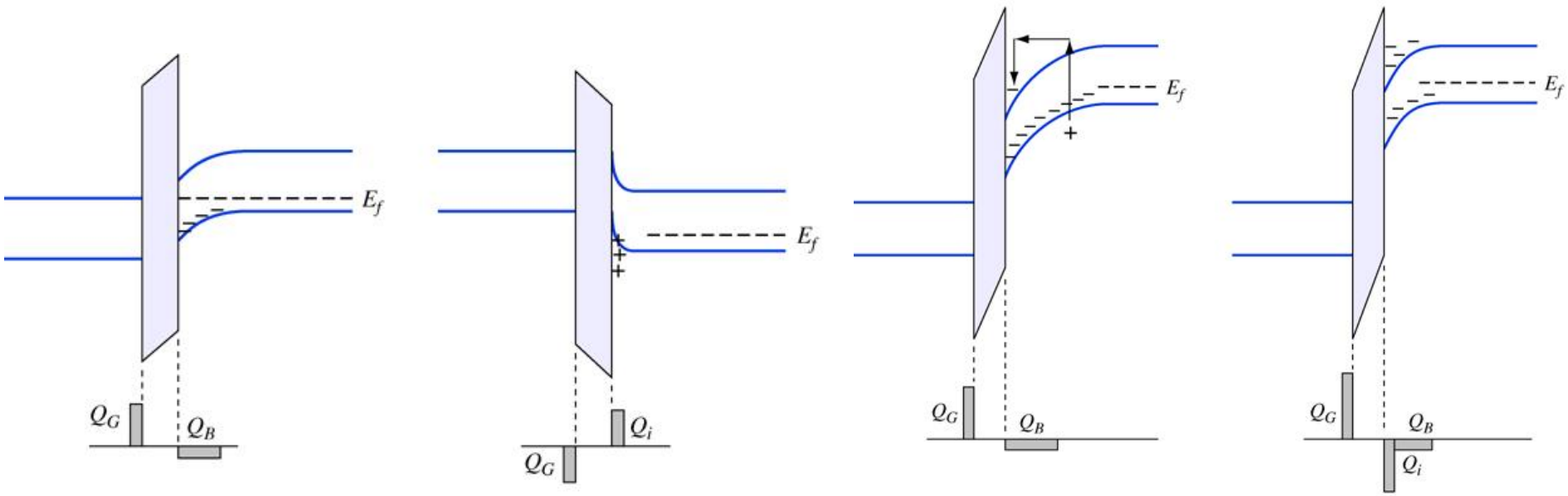
Invert surface, create electron channel

Increasing V_G

Now draw the diagrams for n-type substrate, PMOS

MOS Capacitor Under Varying Gate Bias

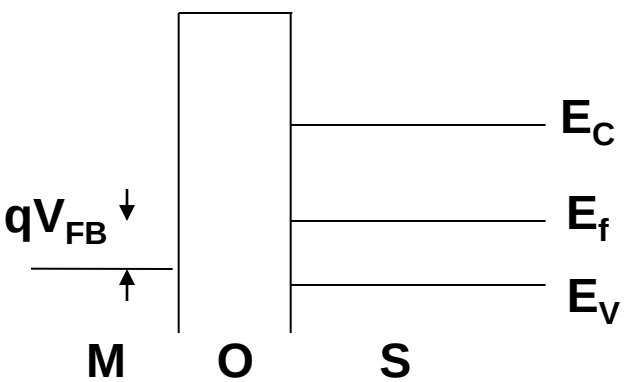
Same concept, different figures



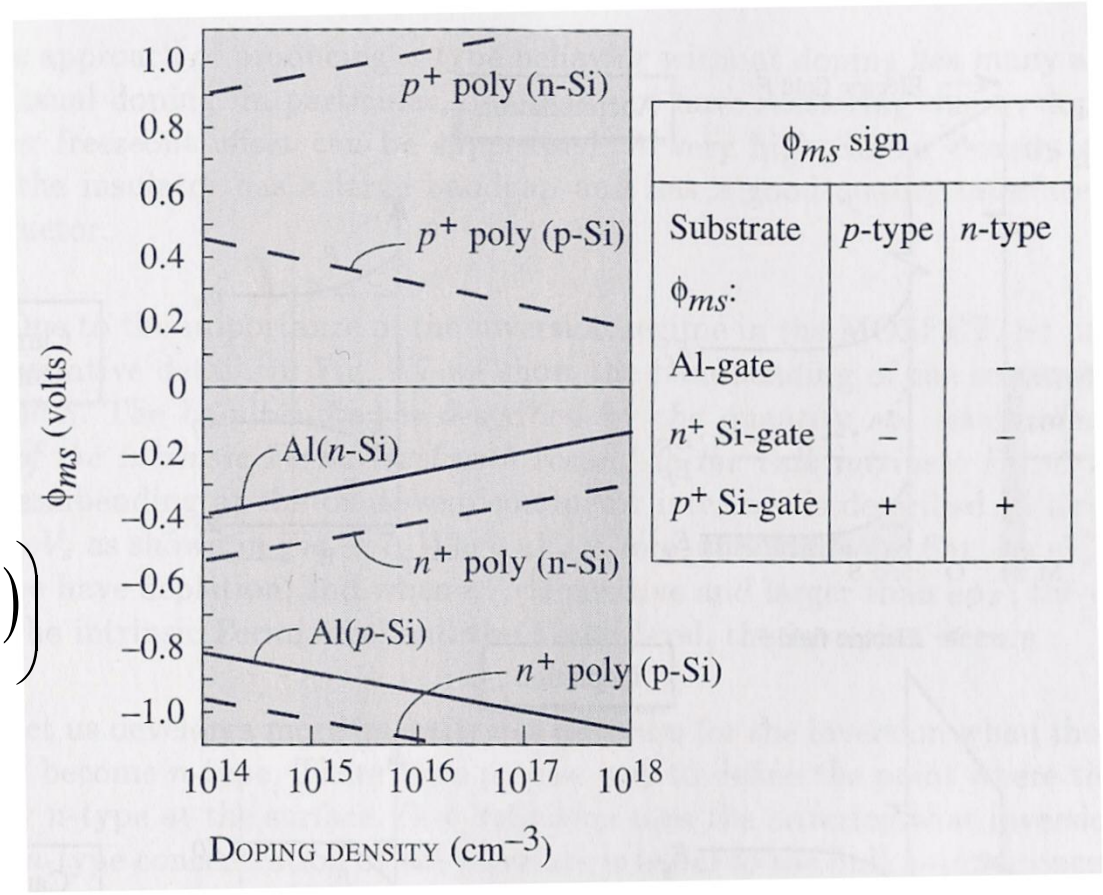
(*a*) Equilibrium (*b*) Accumulation (*c*) Immediately after positive voltage applied on gate (*d*) Steady state with positive voltage applied to gate

Flat Band Condition

Voltage needed for flat energy bands (analagous to V_{bi})



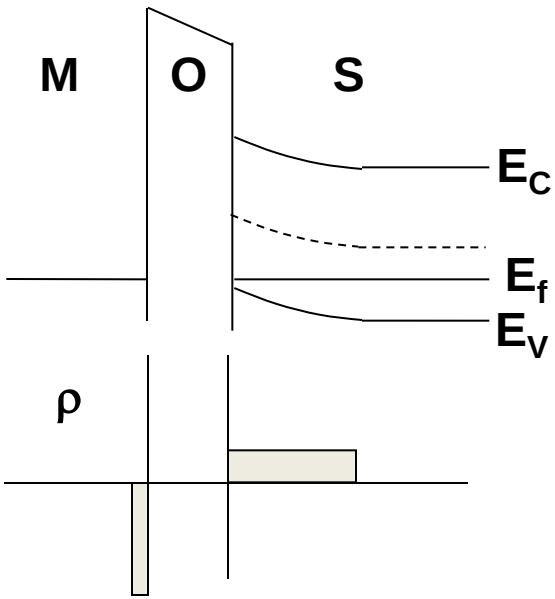
$$V_{FB} = \phi_{MS} = \phi_M - \left(\chi_S + \frac{1}{q}\left(E_C - E_f\right) \right)$$

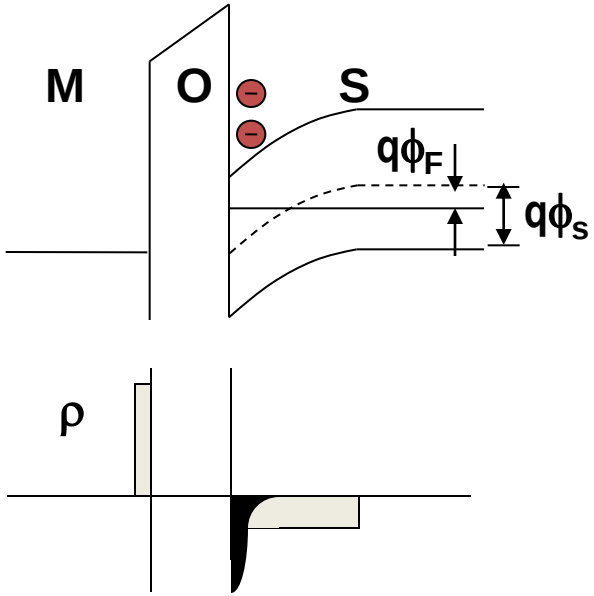


ϕ_{ms} sign		
Substrate	p-type	n-type
ϕ_{ms}:		
Al-gate	–	–
n^+ Si-gate	–	–
p^+ Si-gate	+	+

J. Singh, Semiconductor Devices: Basic Principles

New Terminology





$$\phi_S = \frac{1}{q}\left[E_i(bulk) - E_i(surface)\right]$$

Surface potential NOT semiconductor workfunction

$$\phi_F = \frac{1}{q}\left[E_i(bulk) - E_F\right]$$

Potential related to doping

What is the Inversion Condition?

What is ϕ_F for a given doping level?

p-type Semiconductor

$$\phi_F = \frac{kT}{q}\ln\left(N_A / n_i\right)$$

n-type Semiconductor

$$\phi_F = -\frac{kT}{q}\ln\left(N_D / n_i\right)$$

Define inversion where carrier concentration at O-S interface equal to doping level in the bulk

$$\boxed{\phi_S = 2\phi_F}$$

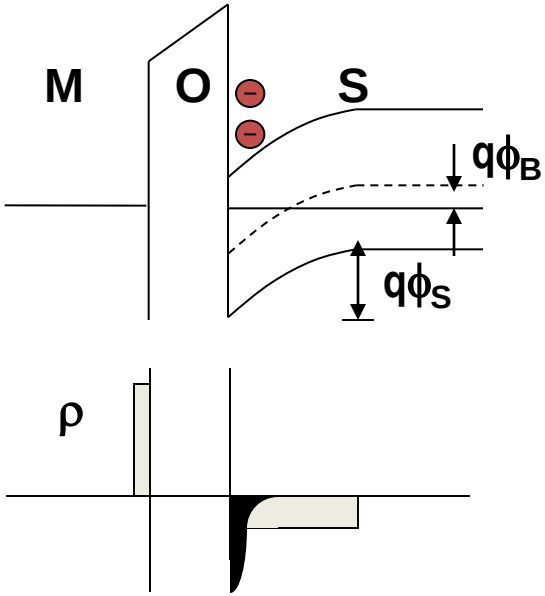
Maximum Depletion Width

Depletion width changes slowly beyond inversion,
Assume depletion width constant = W_T

$$W = \sqrt{\frac{2\varepsilon\phi_S}{qN}}$$

At inversion transition

$$\boxed{W_T = \sqrt{\frac{4\varepsilon|\phi_F|}{qN}}}$$



How will the width depend on doping?

Gate Voltage Relation

We have determined surface potential required for inversion, but what is the gate voltage required? (note there is a voltage drop across oxide)

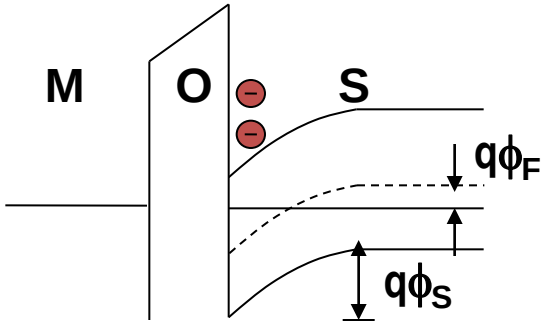
Apply electrostatic boundary conditions

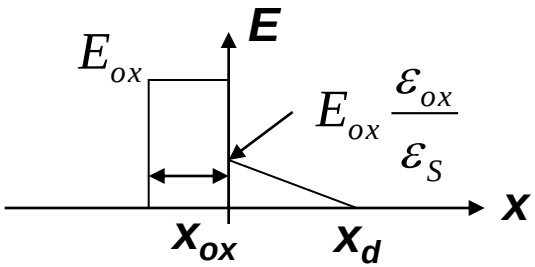
$$V_G = \phi_S + \frac{\varepsilon_S}{\varepsilon_{ox}} x_{ox} E_S$$

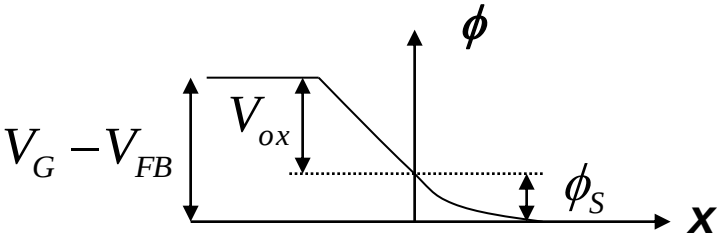
$$E_S = \sqrt{\frac{2qN}{\varepsilon_S}|\phi_S|}$$

$$V_G = \phi_S + \frac{x_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_S N|\phi_S|}$$

$$V_G = \phi_S + \frac{\sqrt{2q\varepsilon_S N|\phi_S|}}{C_{ox}} = \phi_S + \frac{Q_{ox}}{C_{ox}}$$

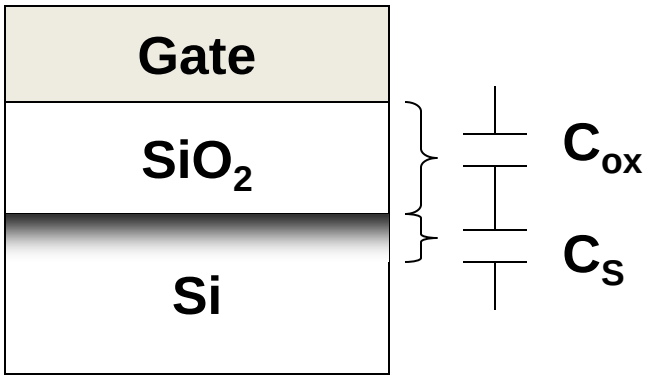






C-V Characteristics

MOS: 2 capacitors in series

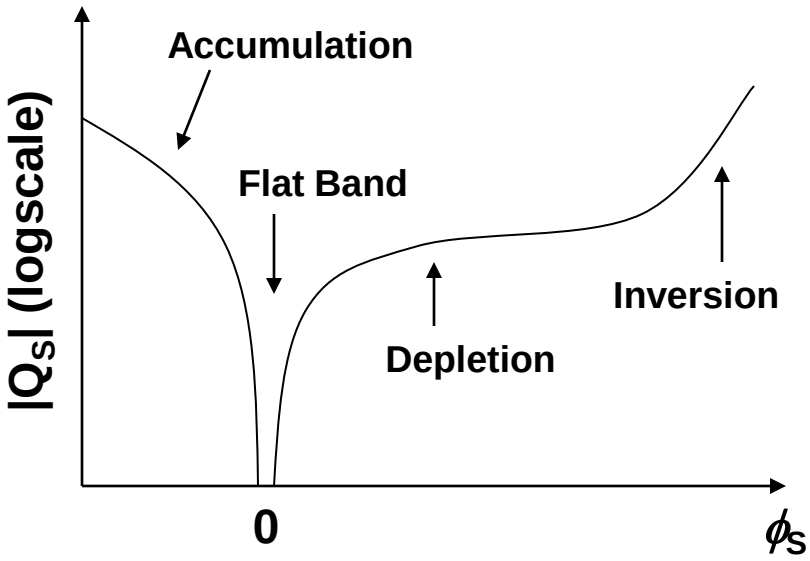


$$C_{dif} = \frac{C_{ox}C_S}{C_{ox}+C_S} = \left(\frac{1}{C_{ox}} + \frac{1}{C_S}\right)^{-1}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{x_{ox}}$$

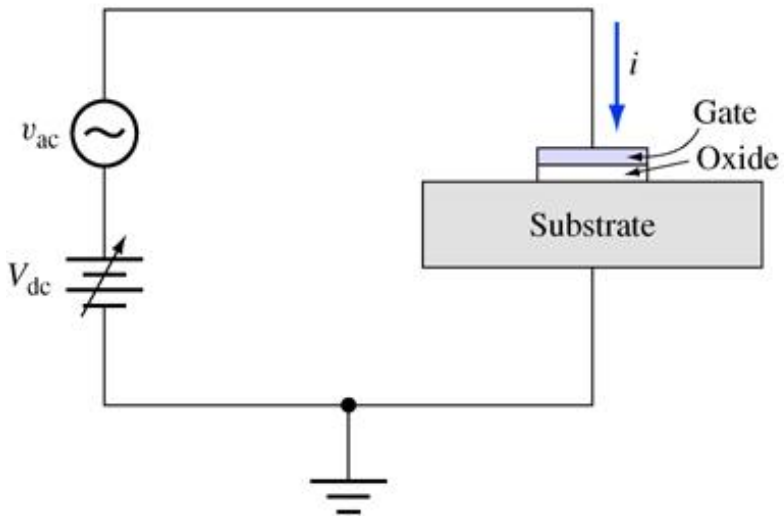
$$C_S = \left|\frac{dQ_S}{d\phi_S}\right|$$

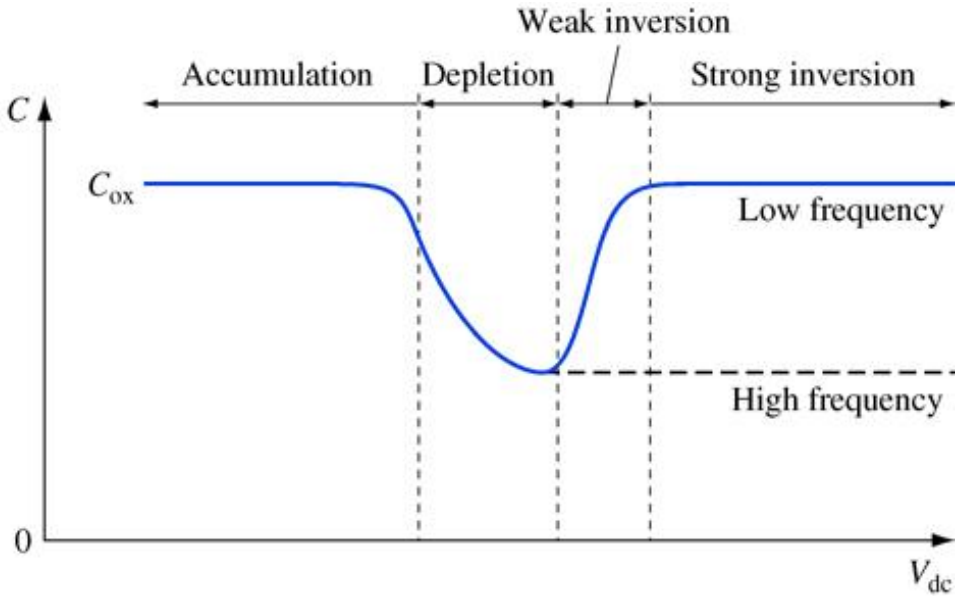
C_S depends on bias, charge density



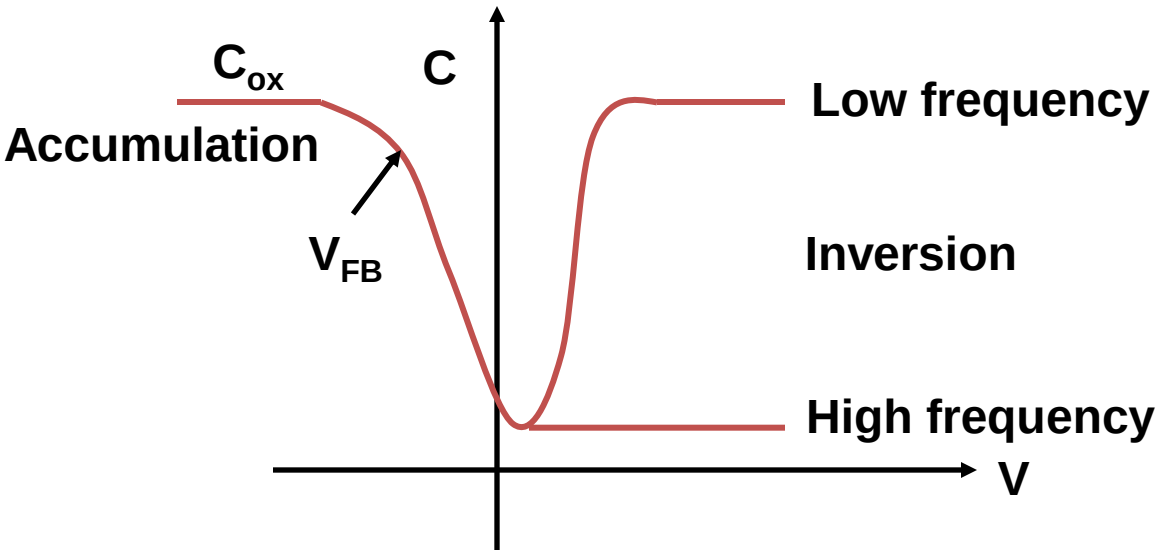
Capacitance-Voltage Characteristics

Capacitance varies with C_S

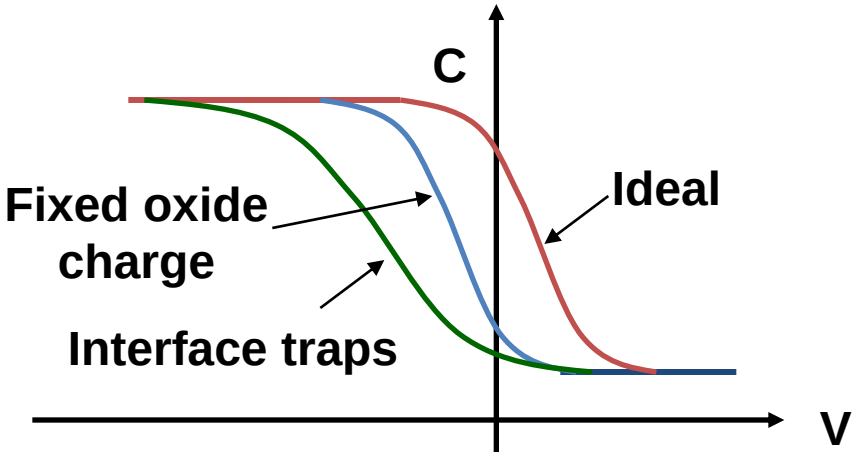




C-V Characteristics



At high frequency, inversion layer cannot form



Charge trapped in oxide or at oxide/semiconductor interface distort C-V characteristics