Call for Papers for a Special Section of IEEE Transactions on VLSI Systems on System Level Interconnect Prediction (SLIP)

Complex wiring systems that consist of signal, power, and clock interconnections will place significant limits on performance, power dissipation, design complexity, and cost of billion transistor systems. Sophisticated system-level statistical models for wire demand, noise, and delay are needed to predict and optimize computer architectures, physical designs, and implementation technologies. Primary applications of SLIP theory include early architectural planning, advanced interconnect timing analysis, FPGA architecture design, synthetic benchmark circuit generation, advanced placement and routing congestion metrics, a priori multilevel wire sizing and repeater insertion estimation, enhanced technology roadmap planning (e.g. low k-dielectrics, 3-D integration, integrated photonics, etc.), and early yield analysis. Over the years, system simulators such as SUSPENS (Stanford), RIPE (RPI), BACPACK (Berkeley), GENESYS (Georgia Tech), and GTX (MARCO GSRC) have incorporated SLIP models to estimate clock frequency, IPC, dynamic and static power dissipation, die size, number of required metal levels, and yield for future VLSI systems.

Scope

Submissions that focus on theory and application of system level interconnect prediction to computer architectures, physical design, and interconnect technology are invited for this special section of T-VLSI. Specific topics of interest are:

1. Statistical properties of complex interconnect systems
2. Techniques and calibrations for “Rentian” and “non-Rentian” interconnect estimation
3. A priori estimation of wirelength, area, power, delay, and noise distributions, with applications to:
   a. Architectural and microarchitectural design space exploration
   b. FPGA architectural design and re-configurable interconnect networks
   c. Interconnect-centric design methodologies
   d. Multilevel interconnect architecture optimization and planning
   e. Interconnect technology and architecture/resource planning
   f. Manufacturing optimization and advanced yield estimation
   g. Self-consistency evaluation of ITRS projections
4. Interconnect planning flows for specific target technologies
   (e.g. ASIC/SoC, FPGA, System-in-package, RF, 3-D integration, integrated photonics, and molecular/nanoelectronics)

Authors of papers presented at the SLIP 2003 workshop are particularly encouraged to submit an extended version of their paper. Submissions of relevant work not presented at the workshop are also welcome.

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Submission Guidelines

Paper submission deadline is September 10, 2003 with a target publication date in spring 2004. Papers will be submitted electronically through IEEE’s Manuscript Central by accessing tvlsi-ieee.manuscriptcentral.com with your web browser to upload a PDF or postscript version of your manuscript submission.

During the Manuscript Central login, when prompted for MANUSCRIPT TYPE, be sure to indicate that your submission is for a SPECIAL ISSUE. Also, you will be prompted for additional comments to the editor-in-chief. Please include the following comment at this stage and also on the title page of your actual manuscript:

SPECIAL ISSUE FOR SYSTEM LEVEL INTERCONNECT PREDICTION (SLIP) -- GUEST EDITORS: DENNIS SYLVESTER AND ANDREW KAHNG

Regular paper submissions should be 8-10 pages in length and brief papers should be 3-4 pages in length. Please follow the submission guidelines specified by the IEEE Transactions on VLSI Systems.