Stochastic Wire Length Sampling For Cycle Time Estimation

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Cycle time models are used for a-priori estimation of chip Clock Rate.

- Standard model incorporates delays incurred due to
  1. Standard Cell.
  2. Interconnection Wire.

- Electrical Characterization of Interconnecting Wire is based upon
  wire geometry of the layer where the wire of average length resides.
Sample wires from the Global Wire length Distribution.

Before sampling we need

Sampling model incorporates the effects of varying wire geometries in different layers.

Provides an estimate of variation due to inherent stochastic nature of layout process.
Electrical Characterization:

- $R_{int}$: Interconnect Resistance
- $C_{int}$: Interconnect Capacitance
- $R_{cell}$: Gate Resistance
- $C_{cell}$: Gate Capacitance
- $l(i)$: Wire length

Sakurai model for 50% Rise time:

$$t(i) = 0.377R_{int}C_{int}l(i)^2 + 0.693(R_{cell}C_{int}l(i) + C_{cell}R_{int}l(i) + R_{cell}C_{cell})$$

Collecting terms:

$$t(i) = 0.377R_{int}C_{int}l(i)^2 + 0.693(R_{cell}C_{int} + C_{cell}R_{int})l(i) + 0.693(R_{cell}C_{cell})$$

- Purely interconnect term
- Cross Coupling term
- Pure device term

• Quadratic nature of Sakurai delay model may induce non-linearity in delay estimates, if the pure interconnect term dominates.
Local Delay:

$$t_{local} = \sum_{i=1}^{Logic \ depth} t(i)$$

Cycle time:

$$t_{cycle} = t_{local} + t_{global} + t_{setup} + t_{\text{flip-flop}}$$

1-skew

Where

$$T_{\text{flip-flop}}$$: Time take from the clock edge data is captured at the input latch to when its available at output (200 ps)

$$T_{\text{setup}}$$: Stabilizing time for inputs of latches of prior to next rising clock edge (200 ps).

skew : worst case skew between clocks (10 % of cycle time).
Global Wire length estimate –
Pseudo – placement

- Global Wire length distribution extracted from a standard netlist, ibm03p (ISPD) of approximately 27000 cells.
- The length distribution (N) is determined by using

\[ N(L) = KqD \]

Where

- \( N(L) \) is number of wires of length \( L \).
- \( q \) is occupancy probability given by

\[ q = l^{2\rho-4} \]

\( \rho \) = rent exponent.
- \( K \) is a normalization coefficient.
- \( D \) is all probable sites for cell placement for a given floor plan.
Parameters for determining wiring capacity

- Geometrical parameters for the layer
- Placement efficiency
- Floor plan

Layer Capacity:

\[ C = \eta(n) C_{tot} \left\{ \frac{w_c h_c}{\eta_p p(n)} \right\} \]
- The global wire length distribution is allocated to a six-layer process.

- Pseudo-Routing renders an *allocated distribution* which is used in wire sampling.
The Roulette – Layer Selection

Layer boundaries

Layer 1

Layer 2

Layer 3

Layer 4

Layer 5

Layer 6

Weighted Random Pointer (WRP)

(WRP)
Weighted Random Sampling

Roulette layer Selection

Allocated Layers

Layer 1
Layer 2
Layer 3
Layer 4
Layer 5
Layer 6

Sampling Space

Bisection Algorithm

Sampled Wire & Layer

Electrical & Computer Engineering
The Bisection Algorithm

- Efficient Search Algorithm for heavily skewed distributions.
- Search process requires $O(\log N)$ steps
- The Algorithm is searching for the value 48.
• Wire allocation, layer selection and Wire sampling algorithms work together to recover approximately the Actual Wire length.

• The weighted random sampling of wires reflects the behavior of actual wire length distribution with reasonable accuracy.
The Setup

- Cycle Time Estimates with
  1. Local Delays (Excluding $t_{\text{global}}$ term in Sakurai Equation)
  2. Local and Global Delay (Including $t_{\text{global}}$)

Cycle time:

$$t_{\text{cycle}} = t_{\text{local}} + t_{\text{global}} + t_{\text{setup}} + t_{\text{flip-flop}} \times (1 - \text{s skew})$$

- Fixed Fan Out range from 1 to 3.
- Calculation of $\text{Clk}_{\text{avg}}$ (based on Mean Value model).
- Each Experiment was run of 1000 trials for above conditions.
Results – Local Estimates

- 1000 trials of clock rate estimates based on stochastic local delay with fixed FanOut of (a) 1 (b) 2 (c) 3. Clk\text{avg} is cycle time estimated using average wire lengths.
Results – Global Estimates

- 1000 trials of clock rate estimates local delay and deterministic global delay with fixed FanOut of (a) 1 (b) 2 (c) 3. $\text{Clk}_{\text{avg}}$ is cycle time estimated using average wire lengths.
### Local Clock Estimate

<table>
<thead>
<tr>
<th>Statistical Analysis</th>
<th>Fanout 1</th>
<th>Fanout 2</th>
<th>Fanout 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Deviation (Ghz)</td>
<td>0.0573</td>
<td>0.0731</td>
<td>0.8266</td>
</tr>
<tr>
<td>Mean (Ghz)</td>
<td>1.3740</td>
<td>1.3276</td>
<td>1.2860</td>
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<tr>
<td>$\text{Clk}_{\text{avg}}$ (Ghz)</td>
<td>1.3751</td>
<td>1.3070</td>
<td>1.2598</td>
</tr>
</tbody>
</table>

### Global Clock Estimate

<table>
<thead>
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<th>Fanout 2</th>
<th>Fanout 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Deviation (Ghz)</td>
<td>0.0495</td>
<td>0.0574</td>
<td>0.0679</td>
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<tr>
<td>Mean (Ghz)</td>
<td>1.2805</td>
<td>1.2096</td>
<td>1.1499</td>
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<tr>
<td>$\text{Clk}_{\text{avg}}$ (Ghz)</td>
<td>1.2683</td>
<td>1.1951</td>
<td>1.1298</td>
</tr>
</tbody>
</table>
Observations

- Fixed FanOut Vectors ranging from 1 to 3 shows a decreasing mean clock rate and increasing Standard Deviation with increasing FanOuts.

- Including a wire of maximum length (Global Estimates) reduces mean clock rate with relative reduction in standard deviation.

- The $\text{Clk}_{\text{avg}}$ values based on mean value model lies in close vicinity of mean clock rate estimated for each set of experiments.
Conclusions

- The scheme is suitable for investigating variable geometries in multi-layer wiring schemes.

- The estimates have an expected mean value and a standard deviation of approximately 5%.

- The median *global* clock rates do not differ significantly from *local* rates.

- There is a sharp fall in the clock rate distribution after the median values.

- The scheme gives a measure of distribution *skewness*, thereby modeling the inherent stochastic nature of layout process.

- The $\text{Clk}_{\text{avg}}$ being in close vicinity of the median rates, validates the appropriateness of the mean value model for logic depth of 25.