

Dennis Sylvester

Professor

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Professional Experience

Professor, University of Michigan, Ann Arbor	2010 – present
Associate Professor	2005 – 2010
Assistant Professor	2000 – 2005
• Department of Electrical Engineering and Computer Science	
• Director of Michigan Integrated Circuits Laboratory (MICL)	
Co-founder and Director, Ambiq Micro	2010 – present
Visiting Associate Professor, National University of Singapore	2006 – 2007
• Department of Electrical and Computer Engineering	
Senior R&D Engineer, Synopsys, Inc., Mountain View, CA	1999 – 2000
TCAD Engineer, Hewlett-Packard Laboratories, Palo Alto, CA	1996 - 1998

Education

University of California, Berkeley, Berkeley, California

Ph.D. Electrical Engineering, 1999

Dissertation: *Analytical Modeling and Characterization of Deep Submicron Interconnect*

M.S. Electrical Engineering, 1997

Thesis: *Interconnect Capacitance Characterization Using Charge-Based Capacitance Measurement (CBCM) Technique*

University of Michigan, Ann Arbor, Michigan

B.S. Electrical Engineering, 1995

Summa Cum Laude

Honors and Awards

- IEEE Fellow, 2011, “for contributions to energy-efficient integrated circuits”

- University of Michigan College of Engineering Ted Kennedy Family Team Excellence Award, 2009-2010
- Best Paper Award, *ACM/IEEE International Symposium on Low-Power Electronics and Design*, 2009
- University of Michigan College of Engineering Ted Kennedy Family Team Excellence Award, 2008-2009
- Best Paper Award, *IEEE International Symposium on Quality Electronic Design*, 2006
- Henry Russel Award, University of Michigan, given in recognition of distinguished scholarship and conspicuous ability as a teacher, 2006
- University of Michigan College of Engineering Vulcans Education Excellence Award, 2005-2006
- Semiconductor Research Corporation Inventor Recognition Award, 2005
- 1938E Award, U-M College of Engineering, given for outstanding teaching, counseling, and scholarly integrity, 2004
- IBM Faculty Award, IBM Austin Center for Advanced Studies, 2004
- Association for Computing Machinery (ACM) Special Interest Group on Design Automation (SIGDA) Outstanding New Faculty Award, 2003
- Ruth and Joel Spira Outstanding Teaching Award, U-M College of Engineering, 2003
- NSF Faculty Early Career Development (CAREER) Award, 2002
- David J. Sakrison Memorial Prize for best dissertation, UC-Berkeley EECS department, 2000
- Beatrice Winner Award, *IEEE International Solid-State Circuits Conference*, 2000
- Synopsys Special Recognition Award (for excellent performance and outstanding contribution to Synopsys Engineering), 2000
- Best Paper Award, Semiconductor Research Corporation Graduate Fellowship Program, 1999
- Outstanding Research Presentation Award, Semiconductor Research Corporation Technical Conference, 1998
- Best Student Paper Award, *IEEE International Semiconductor Device Research Symposium*, 1997
- Semiconductor Research Corporation Graduate Fellow, 1997 – 1999

Research Interests

- Low power integrated circuit design and design automation
- Design for manufacturability (DFM)
- On-chip interconnect modeling for timing and signal integrity
- Variation-tolerant circuit design styles

Professional Activities and Service

- Associate Editor, *IEEE Transactions on Computer-Aided Design*, 2006 – present
- Executive Committee member, *ACM/IEEE Design Automation Conference*, 2008 – 2009
- Tutorials Chair, *ACM/IEEE Design Automation Conference*, 2009
- Steering Committee member, *ACM/IEEE International Symposium on Physical Design*, 2006 – 2008
- Co-organizer, *ACM Workshop on Test Structure Design for Variability Characterization (TSD)*, 2008.

- Associate Editor, *IEEE Transactions on VLSI Systems*, 2003 – 2007
- Planning Committee member, Semiconductor Research Corporation Interconnect Forum, Santa Cruz, CA, 2006
- General Chair, *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems* (TAU), 2005
- Panel moderator, “Who is responsible for design for manufacturability issues in the era of nanotechnologies?”, *ACM/IEEE Asia-South Pacific Design Automation Conference*, 2005.
- Technical Program Committee co-Chair, *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems* (TAU), 2004
- Tutorials Chair, *IEEE International Symposium on Quality Electronic Design* (ISQED), 2004
- Guest co-Editor, *IEEE Transactions on VLSI Systems*, special issue on System-Level Interconnect Prediction, October 2004
- General Chair, *ACM/IEEE International Workshop on System-Level Interconnect Prediction* (SLIP), 2003
- Co-organizer, panel on low-power design automation tools, *ACM/IEEE Design Automation Conference* (DAC), 2003
- Co-organizer and co-chair, special session on nanoscale CMOS, *ACM/IEEE Design Automation Conference*, 2002
- Member, U.S. Design Technology Working Group (TWG) for the International Technology Roadmap for Semiconductors (ITRS), 2001–2003
- Technical Program Committee Chair, *ACM/IEEE International Workshop on System-Level Interconnect Prediction* (SLIP), 2001 (co-chair), 2002
- Technical Program Committee member:
 - *ACM/IEEE Design Automation Conference* (DAC), 2003–2006, sub-committee chair 2004–2006
 - *IEEE International Workshop on Design for Manufacturability and Yield* (DFM&Y), 2006
 - *ACM/IEEE International Symposium on Low-Power Electronics Design* (ISLPED), 2004–2005
 - *ACM/IEEE Asia-South Pacific Design Automation Conference* (ASP-DAC), 2005
 - *IEEE International Symposium on Quality Electronic Design* (ISQED), 2002–2003, chair of sub-committee on device, interconnect, and circuit-level modeling and analysis (2003)
 - *ACM/IEEE International Conference on Computer-Aided Design* (ICCAD), 2000–2002
 - *IEEE International Conference on Computer Design* (ICCD), 2001–2003, 2006 (Logic and Circuits Track co-chair)
 - *ACM/IEEE International Workshop on Timing Issues in Digital Systems* (TAU), 2002, 2006
 - *ACM/IEEE International Workshop on System-Level Interconnect Prediction* (SLIP), 2000, 2004–2006
 - *IEEE International Symposium on Circuits and Systems* (ISCAS), 2002–2003
 - *SPIE Design and Process Integration for Microelectronic Manufacturing Conference*, 2005–2008
 - *IEEE International Conference on VLSI and System-on-Chip*, 2010
- Executive committee member, Fabless Semiconductor Association, 2000
- Proposal reviewer for:
 - National Science Foundation
 - University of California MICRO program

- Netherlands Organization for Scientific Research
- Reviewer for:
 - *IEEE Transactions on Computer-Aided Design, IEEE Transactions on VLSI Systems, IEEE Journal of Solid-State Circuits, IEEE Transactions on Electron Devices, IEEE Transactions on Computers, IEEE Design & Test of Computers, IEEE Transactions on Circuits and Systems, Proceedings of the IEEE*
 - *ACM Transactions on Design Automation of Electronic Systems*
 - *Elsevier Integration: The VLSI Journal*

University Service

- CSE chair search advisory committee member (ECE representative), 2010 – 2011
- ECE graduate admissions committee member, 2009 – present
- EE undergraduate advisor, 2010 – present
- ECE financial aid strategy team member, 2009
- ECE executive committee member, 2007 – 2009
- ECE faculty search committee member, 2007 – 2009
- CSE chair search advisory committee member (ECE representative), 2007 – 2008
- VLSI graduate advisor (concurrently a member of EE graduate committee), 2000 – 2010
- Computer Engineering Center task force member, 2006
- ECE faculty search sub-committee chair (VLSI), 2004 – 2005
- EECS strategic planning sub-committee on department structure and faculty environment, 2005
- Eta Kappa Nu (HKN) faculty advisor, 2003 – 2006
- EECS building renovation committee member, 2003 – 2006
- ECE faculty search sub-committee member (RF circuits/MEMS), 2002–2003
- Departmental Computing Organization (DCO) review committee member, 2002
- Organizer, EECS Department VLSI seminar series (renamed the Micron Technology Foundation VLSI Seminar Series), 2001 – 2006
- Marshal, Spring 2002 Commencement Exercises
- Computer Engineering degree program committee member, 2001
- HKN Scholarship faculty reviewer, 2000, 2006
- Promotion and tenure, and/or reappointment casebook committee member or chair, 2005, 2006, 2008, 2010 (chair)

Teaching

Courses Taught:

- EECS 312, Digital Integrated Circuits
- EECS 427, VLSI Design I
- EECS 523, Digital Integrated Circuit Technology
- EECS 627, VLSI Design II
- EECS 628, Advanced High Performance VLSI Design

Courses Developed or Significantly Revised:

- EECS 312, Digital Integrated Circuits (Developed)
- EECS 427, VLSI Design I (Revised, Fall 2003)
- EECS 628, Advanced High Performance VLSI Design (Co-developed)

Consulting

- STMicroelectronics, Geneva, Switzerland, [Technology Council Member, 2006 – present]
- Tela Innovations, Campbell, CA [Technical Advisory Board member, 2009 – present]
- Sequence Design, Inc., Santa Clara, CA [Technical Advisory Board member, 2003 – 2009]
- Blaze DFM, Inc., Sunnyvale, CA [Technical Advisory Board member, 2004 – 2008]
- Cadence Design Systems, San Jose, CA
- Intel Corporation, Santa Clara, CA and Haifa, Israel
- Rader, Fishman, and Grauer PLLC, Bloomfield Hills, MI
- King Abdullah University of Science and Technology, Saudi Arabia
- NEC Research Labs, Princeton, NJ
- Via Technologies, Inc., Taipei, Taiwan

Grants and Contracts

- National Science Foundation, “Collaborative Research: Variability Aware Software for Efficient Computing with Nanoscale Devices ,” 09/01/2010 – 08/31/2015, co-PI under Director Rajesh Gupta, UCSD, \$10,000,000.
- Office of Naval Research, “A Hierarchical Wireless System for Distributed Strain Monitoring in Naval Structures,” SBIR with Civionics, LLC, 05/10/2010 – 11/09/2010, \$33,250.
- King Abdullah University of Science and Technology Saudi Arabia, “Toward efficient nanoelectronic systems for biomedical sensing,” lead PI: Yogesh Gianchandani, 05/01/2010 – 04/30/2012, \$680,000.
- Intel Corporation, “A confidence-driven model for predictable computing in future technologies,” PI: Zhengya Zhang, co-PIs: Dennis Sylvester, David Blaauw, Peter Chen, \$169,000 (gift), 2010.
- Google, gift to support research in energy-efficient memory and processor architectures, joint with Professor Thomas Wenisch, David Blaauw, and Trevor Mudge, \$100,000, 2009.
- National Science Foundation, “Reclaiming Moore's Law through Ultra Energy Efficient Computing,” 08/01/2009 – 07/31/2014, co-PI with David Blaauw (lead PI, U-Michigan), Trevor Mudge (U-Michigan), Chaitali Chakrabarti (Arizona St.), and David Harris (Harvey Mudd), \$2,778,507.
- Microelectronics Advanced Research Corporation (MARCO) and Defense Advanced Research Projects Agency (DARPA), “Resiliency for ultra-low power platforms,” through the Gigascale Systems Research Center (GSRC), 11/01/09 – 10/31/12, \$315,250.
- Medical Innovation Center Innovation Grant, University of Michigan, “Brain Pressure Sensor – Wireless,” co-PI with Dr. Lynda Yang and Mr. Alex Kim, \$10,000, 2009.
- National Institute of Standards and Technology, “Cyber-enabled wireless monitoring systems for the protection of deteriorating national infrastructure systems,” 02/01/2009 – 01/31/2014, \$19,162,000.

- Army Research Laboratory, “COM-BAT: Center for Objective Microelectronics and Biomimetic Advanced Technology,” Kamal Sarabandi (Director), Dennis Sylvester (Processing team leader), 04/01/08 – 03/31/13, \$10,000,000.
- National Science Foundation, “An Engineering Research Center in Wireless Integrated Microsystems,” Kensall D. Wise (Director), Dennis Sylvester (Micropower Circuits thrust leader, 02/01/05 – present), total thrust budget \$417,000 (direct costs) in 2007-2008.
- National Science Foundation, “Probabilistic wearout in nanoscale CMOS: analysis, monitoring, and optimization,” co-PI with David Blaauw, U-Michigan, 09/01/08 – 08/31/11, \$300,000.
- Defense Advanced Research Projects Agency (DARPA), “Strained Si/SiGe/Ge HETEROJUNCTION Tunneling Transistor (HETT) Technology with Steep Subthreshold Slope for Extremely Low Power Electronics,” (IBM lead organization), 01/01/08 – 12/31/09, \$444,000 (UM share).
- Semiconductor Technology Academic Research Center (Japan), “Low-cost body biasing and reliability-aware CAD,” 01/01/08 – 12/31/08, \$180,000.
- Semiconductor Technology Academic Research Center (Japan), “Soft-edge flip-flops for timing yield and parametric yield budgeting across functional units,” 09/01/06 – 08/31/07, \$180,000.
- Microelectronics Advanced Research Corporation (MARCO) and Defense Advanced Research Projects Agency (DARPA), “ElastIC: An Adaptive Self-Healing Architecture for Unpredictable Silicon,” 09/01/06 – 10/31/09, \$378,000
- National Science Foundation, “Formal Design Techniques for Adaptive Circuit Fabrics,” co-PI with Michael Orshansky, U-Texas, Austin, 09/01/06 – 08/31/09, \$464,440
- Semiconductor Research Corporation, “A Design Optimization Framework for Process Variation Tolerance,” co-PI with David Blaauw, U-Michigan, 09/01/06 – 12/31/09, \$390,000
- Semiconductor Research Corporation, “CAD Solutions for Parametric Yield Optimization,” co-PI with David Blaauw, U-Michigan, 09/01/05 – 08/31/08, \$360,000
- Semiconductor Technology Academic Research Center (Japan), “Runtime leakage analysis and statistical static timing analysis enhancements,” 09/01/05 – 08/31/06, \$180,000.
- National Science Foundation and Semiconductor Research Corporation, “Communication Fabrics for the Globally Asynchronous Network-on-Chip Era,” co-PI with Michael Flynn, U-Michigan, 9/01/04 – 08/31/07, \$489,500
- Microelectronics Advanced Research Corporation (MARCO) and Defense Advanced Research Projects Agency (DARPA), “System-Level Living Roadmap,” 09/01/03 – 08/31/06, \$592,000
- National Science Foundation, “CAREER: Improving Technology-EDA Integration through Interconnect Design Tools for Nanometer Design,” 01/01/02 – 12/31/08, \$375,000
- National Science Foundation, “ITR: Methodologies for Robust Design of Information Systems under Multiple Sources of Uncertainty,” co-PI with David Blaauw, U-Michigan, Sachin Sapatnekar, U-Minnesota, and Sarma Vrudhula, U-Arizona, 09/01/02 – 08/31/08, \$1,800,000
- Semiconductor Research Corporation, “Analysis and Reduction of Simultaneous Gate-Oxide Tunneling and Subthreshold Leakage Current,” co-PI with David Blaauw, U-Michigan, 07/01/03 – 06/30/06, \$360,000
- Semiconductor Research Corporation, “Algorithmic and Circuit-level Approaches to Leveraging Multi-Vth processes,” co-PI with Kurt Keutzer, UC-Berkeley, 07/01/01 – 04/30/05, \$490,000
- Semiconductor Research Corporation, “Layout Techniques for Cost-driven Control of Lithography-induced Variability,” co-PI with Andrew B. Kahng of UC-San Diego, 07/01/01 – 01/31/05, \$420,000
- Defense Advanced Research Projects Agency (DARPA), “Complex Signal Processing Application Specific Integrated Circuit Designs,” lead PI: Richard Brown, University of Michigan, subcontract of BAE Systems, 09/18/01 – 03/15/03, \$225,000

- Microelectronics Advanced Research Corporation (MARCO) and Defense Advanced Research Projects Agency (DARPA), “GSRC Technology Extrapolation (GTX) Engine,” 01/01/01 – 08/31/03, \$285,000
- IBM Corporation, Austin Center for Advanced Studies, “Joint Statistical Optimization of Static Power Consumption and Performance,” Faculty Award (gift), \$40,000, 2004.
- Intel Corporation, “VLSI Design Curriculum,” co-PI with Richard Brown, David Blaauw, and Michael Flynn, 09/01/03 – 08/31/04, \$202,173.
- Intel Circuits Research Laboratory, gift to support research in the areas of global signaling and multi-Vdd circuit design, \$120,000, 2003–2005.
- Intel Corporation, “Current Source Cell Models with Variability,” \$20,000, 2005.
- Intel Corporation, “An Alternative Framework for Statistical Optimization Based on Variation Space Sampling, including Current Source Models,” \$10,000, 2006.
- NEC USA, gift to support research in the area of noise-aware timing analysis, \$38,000, 2001.
- Mentor Graphics Corporation, gift to support research in the area of design for manufacturability, \$100,000, 2002–2005.
- Sun Microsystems Academic Equipment Grant, to support research in the area of multi-Vth and multi-Vdd circuit design, 2 Sun Blade 1000 workstations, \$51,000, 2002.
- Intel Corporation, equipment donation to support research in global signaling and multi-Vdd circuit design, \$19,645, 2003.
- Intel Corporation, equipment donation to support research in current source modeling and statistical optimization, \$5,959, 2006.
- Intel Corporation, equipment donation to support the development of a showcase circuit design graduate student office space, \$66,878, 2009.
- U-M College of Engineering, to support the creation of a VLSI seminar series, 09/01/01 – 04/30/03, \$11,500 (supplemented with \$3,500 of support from Solid-State Electronics Laboratory)
- Micron Technology Foundation, to support the VLSI seminar series, 09/01/03 – 04/30/06, \$15,700

Selected Invited Talks and Tutorials

- IEEE Circuits and Systems Forum on Emerging and Selected Topics (CAS-FEST), Variation-Aware Design for Nanoscale VLSI, “Mitigating variability in near-threshold computing,” Athens, Greece, December 2010.
- National Science Foundation Workshop on Interdisciplinary Challenges Beyond the Scaling Limits of Moore’s Law, “Enabling Ubiquitous Computing with Ultra-Low Power Integrated Circuits,” Arlington, VA, August 2010.
- Columbia University, “Enabling Ubiquitous Computing with Ultra-Low Power Integrated Circuits,” Dean’s Distinguished Lecture, April 2010.
- University of Illinois, “Circuit design advances for ultra-low power sensing platforms,” ECE Colloquium, April 2010.
- Michigan State University, “Low voltage circuits to enable widespread sensing applications,” East Lansing, MI, October 2009.
- University of Texas VLSI seminar series, “Circuit design advances for wireless sensing applications,” Austin, TX, September 2009.
- Panelist, “Steep slope or slippery slope,” *IEEE Device Research Conference*, State College, PA, June 2009.

- *IEEE International Solid-State Circuits Conference (ISSCC)*, “Device sizing for variability in energy constrained systems,” Low-voltage design forum speaker and panelist, February 2009.
- Electronic Design Systems Fair, System Design Forum, invited speaker, “Coping with variability in nanoscale CMOS: analyze, sense, correct, exploit,” Yokohama, Japan, January 2009.
- IBM Design Automation Professional Interest Community Seminar, “Extending nanoscale CMOS: analyze, sense, correct, and exploit,” Austin, TX, August 2008.
- Invited lecturer, EPFL summer school on Nanoelectronic Circuits and Tools, “Pushing nanoscale CMOS: Design-related challenges,” and “Extending nanoscale CMOS: analyze, sense, correct, and exploit,” Lausanne, Switzerland, July 2008.
- University of Waterloo, “Low-voltage circuit design for widespread sensing applications,” July 2008.
- UCLA Departmental Seminar Series in Electrical Engineering, “Energy-driven circuit design for ubiquitous sensing applications,” March 2008.
- Panelist, “Scaling the power wall,” *IEEE International Symposium on System-on-Chip*, Tampere, Finland, November 2007.
- IBM Experts Workshop on Low Voltage CMOS, “Highly parallel adaptive systems for low voltage operation,” Yorktown Heights, NY, November 2007.
- ST Microelectronics, “Low power circuit design research at the University of Michigan,” Crolles, France, November 2006.
- Panelist, “How deep is it in here? Will variation-aware analysis be the savior for the nanometer era?”, *ACM/IEEE Design Automation Conference*, July 2006.
- Intel Physical Verification and Physical Design (PVPD) research seminar, “Directions in low-power CAD,” Haifa, Israel, July 2006.
- University of Utah, “IC design at ultra-low supply voltages,” February 2006.
- Georgia Tech Electrical and Computer Engineering Departmental Seminar, “IC design at a crossroads: Enabling low-power and robust computing in nanometer CMOS,” November 2005
- International Conference on Computer-Aided Design, half-day tutorial co-presenter, “Gate characterization and modeling for 90nm and below,” November 2005.
- Cadence Design Systems Distinguished Speaker Series, “IC design at a crossroads: Enabling low-power and robust computing in nanometer CMOS,” October 2005.
- Panelist, Manufacturing for Design meets Design for Manufacturing Forum, Semiconductor Research Corporation, October 2005.
- Northwestern University Seminar Series in Computational Sciences, “New approaches to parametric yield estimation and dual-V_{th} assignment,” October 2005.
- Invited lecturer, Mead Engineering short course, “Circuit design challenges in nanometer-scale CMOS,” Lausanne, Switzerland, July 2005.
- Semiconductor Research Corporation e-Workshop, “Multiple supply and threshold voltage design: guidelines, algorithms, and circuit solutions,” March 2005.
- Austin Center for Advanced Studies Annual Conference, “Parametric yield estimation considering power/performance correlation,” February 2005.
- Asia-South Pacific Design Automation Conference, full-day tutorial co-presenter, “Power-aware design for performance,” January 2005.
- International Symposium on Microarchitecture, full-day tutorial co-presenter, “Low-power robust computing,” December 2004.

- Sequence Design NanoCool Low-power Design Initiative Seminar Keynote, “New approaches to total power reduction including runtime leakage,” San Jose, CA, August 2004.
- Intel VLSI curriculum development two-day workshop, presenter, Hangzhou, China, July 2004.
- Intel VLSI curriculum development two-day workshop, presenter, Penang, Malaysia, July 2004.
- Design Automation Conference, full-day tutorial co-presenter, “Getting Your ‘Cool ASIC’ Up to Speed: Practical Techniques and Tools to Achieve Custom-like Performance in a Power-Aware Design Flow,” June 2004.
- Synopsys technology offsite, “EDA and Design Challenges with 45nm Devices,” Half Moon Bay, CA, May 2004.
- *IEEE Annual Workshop on Interconnections within High-Speed Digital Systems*, “Modeling and characterization of chip-level metal interconnects,” Santa Fe, NM, May 2004.
- Panelist, “Buffering and Agony: What does the Future Hold?” *ACM/IEEE International Symposium on Physical Design*, Phoenix, AZ, April 2004.
- University of California, Berkeley, Distinguished Lecture Series, “IC Design at a Crossroads: Enabling Low-Power and Robust Computing in Nanometer CMOS,” April 2004.
- University of Texas, Austin VLSI seminar series, “New Approaches to Total Power Reduction Including Runtime Leakage,” March 2004.
- IBM Austin Research Laboratories and T.J. Watson Research Center, “Multi-Vdd/Vth Design Space and Early Algorithmic Results,” Austin, TX and Yorktown Heights, NY, August 2003.
- Advanced Micro Devices, “Minimum Cost of Correction and Related Design for Value Topics,” Sunnyvale, CA, July 2003.
- Panelist, “Judgment Day for Power Management,” *IEEE VLSI Symposium on Circuits*, joint panel with *IEEE VLSI Symposium on Technology*, Kyoto, Japan, June 2003.
- Fujitsu Laboratories, “Multi-Vdd/Vth Design and Interconnect Tuning Strategies,” Tokyo, Japan, June 2003.
- Mentor Graphics, “Towards Performance-driven Reduction of the Cost of RET-based Lithography Control,” Wilsonville, OR, May 2003.
- Cypress Semiconductor, “Low-power Design for Global Interconnects and Dual-Supply Systems,” San Jose, CA, March 2003.
- Panelist, 2002 International Technology Roadmap for Semiconductors conference, “Challenges and opportunities for a low-power roadmap in consistence with ITRS CMOS scaling,” San Francisco, CA, July 2002.
- IEEE Solid-State Circuits Society Kansai Chapter technical seminar, “High Performance Design in Nanometer Technologies,” Kyoto, Japan, May 2002.
- Hitachi Central Research Laboratories, “High Performance Design in Nanometer Technologies,” Tokyo, Japan, May 2002.
- Sequence Design NanoCool Low-power Design Initiative Seminar Keynote, “Power-driven Challenges in Nanometer Design,” Ottawa, Canada, May 2002.
- Intel Physical Design Symposium, “Global Signaling Strategies for Nanometer CMOS,” Santa Clara, CA, April 2002.
- University of California, Berkeley Electronics System Design (ESD) Seminar, “Global Signaling Strategies for Nanometer CMOS,” April 2002
- International Conference on Computer-Aided Design, full-day tutorial co-presenter, “Electrical Integrity Design and Verification for Digital and Mixed-Signal Systems-on-a-chip,” November 2001.

- NEC Computers and Communications Research Labs (CCRL), “Approaches to Noise-Aware Static Timing Analysis,” Princeton, NJ, December 2000.
- International Conference on Computer-Aided Design, full-day tutorial co-presenter, “Interconnect-centric Design and Analysis for Electrical Integrity in Systems-on-a-chip,” November 2000.
- University of California, Berkeley Solid-State Technology and Device Seminar, “Insights on Deep Submicron Design: An EDA Perspective,” January 2000.
- Fabless Semiconductor Association Modeling Workshop, “The Role of Interconnect in System-Level Performance: Delay, Power, Noise,” invited tutorial, San Jose, CA, May 1999
- IEEE Electron Devices Society Summer Symposium, “Interconnect Scaling: Signal Integrity and Performance in Future High-Speed CMOS Designs,” Santa Clara, CA, June 1998

Patents

Patents Issued

- Dennis Sylvester and Himanshu Kaul, “Transition-aware signaling,” US patent 6,870,402, March 22, 2005.
- Dennis Sylvester, Himanshu Kaul, and David Blaauw, “Actively shielded signal wires,” US patent 6,919,619, July 19, 2005.
- Trevor Mudge, Todd Austin, David Blaauw, Dennis Sylvester, and Krisztian Flautner, “Memory system having fast and slow data reading mechanisms,” US patent 6,944,067, September 13, 2005.
- Todd Austin, David Blaauw, Trevor Mudge, Dennis Sylvester, and Krisztian Flautner, “Memory system having fast and slow data reading mechanisms,” US patent 7,072,229, July 4, 2006.
- Andrew B. Kahng, Puneet Gupta, Dennis Sylvester, and Jie Yang, “Method for correcting a mask layout,” US patent 7,149,999, December 12, 2006.
- Andrew B. Kahng, Puneet Gupta, Dennis Sylvester, and Jie Yang, “Method for correcting a mask layout,” US patent 7,614,032, November 3, 2009.

Disclosures filed

- Scott Hanson, Nurrachman Liu, David Blaauw, and Dennis Sylvester, “Critical path monitoring circuit,” UM file number 3761.
- Mingoo Seok, Yoonmyung Lee, Scott Hanson, David Blaauw, and Dennis Sylvester, “Low leakage memory circuit,” UM file number 3760.
- Yu-Shiang Lin, David Blaauw, and Dennis Sylvester, “An ultra-low power timer for sensor monitoring systems,” UM file number 3759.
- Jae-Sun Seo, David Blaauw, and Dennis Sylvester, “New encoding methods for on-chip data communication using pulse width modulation,” UM file number 3815.
- Ronald Dreslinski, Greg Chen, Trevor Mudge, David Blaauw, Dennis Sylvester, and Kristzian Flautner, “Reconfigurable energy efficient near-threshold cache architecture,” UM file number 3929, provisional patent filed, “Cache memory system for a data processing apparatus.”
- Vineeth T. Veetil, Dennis Sylvester, and David Blaauw, “Method for fast incremental evaluation of a fixed percentile delay of a circuit,” UM file number 3989, provisional patent filed.
- Yoonmyung Lee, Michael Wieckowski, David Blaauw, and Dennis Sylvester, “Logic non-volatile memory with MIM capacitor and stacking,” UM file number 3999, provisional patent filed.
- Brian T. Cline, Vivek Joshi, Dennis Sylvester, and David Blaauw, “Stress-enhanced standard cells for CMOS devices,” UM file number 4042.
- Mingoo Seok, Scott Hanson, Greg Chen, Dennis Sylvester, and David Blaauw, “Pico-power reference voltage generator,” UM file number 4051, provisional patent filed.
- Yu-Shiang Lin and Dennis Sylvester, “Static subthreshold to I/O voltage level shifter,” UM file number 4131, provisional patent filed.

- Yu-Shiang Lin, Dennis Sylvester, and David Blaauw, “Low power temperature sensor,” UM file number 4152.
- Michael Wieckowski and Dennis Sylvester, “Low frequency, low power oscillator using monostable CMOS multivibrators,” UM file number 4154.
- Michael Wieckowski, Greg Chen, and Dennis Sylvester, “Hybrid DC-DC converter for ultra-low power, low voltage applications,” UM file number 4155.
- Scott Hanson and Dennis Sylvester, “Low voltage comparator circuit,” UM file number 4158.
- Mingoo Seok, Scott Hanson, Jae-Sun Seo, David Blaauw, and Dennis Sylvester, “Robust low voltage read-only memory,” UM file number 4159.
- Sudhir Satpathy, David Blaauw, Dennis Sylvester, Trevor Mudge, “An SRAM-based crossbar,” provisional patent filed.
- David Blaauw, Dennis Sylvester, David Fick, Stuart Biles, Michael Wieckowski, Scott Hanson, and Gregory Chen, “Operating parameter control of an apparatus for processing data,” provisional patent filed.
- Sudhir Satpathy, David Blaauw, Trevor Mudge, Dennis Sylvester, “Packet-switching interconnect fabric with single cycle arbitration latency,” provisional patent filed.
- Greg Chen, Dennis Sylvester, David Blaauw, “Integrated circuit memory access mechanisms,” provisional patent filed.
- Greg Chen, Dennis Sylvester, David Blaauw, “Integrated circuit memory power supply,” provisional patent filed.
- Matt Fojtik, Dennis Sylvester, David Blaauw, “Circuit level timing speculation for latch based design by propagating stall events,” provisional patent filed.
- Scott Hanson, Dennis Sylvester, David Blaauw, “Low power reference current generator with tunable temperature sensitivity,” UM file number 4608.
- Scott Hanson, Michael Wieckowski, David Blaauw, and Dennis Sylvester, “Integrated circuit with sleep mode,” UM file number 4657.
- Scott Hanson, Michael Wieckowski, David Blaauw, and Dennis Sylvester, “Low leakage, low voltage memory cell,” UM file number 4656.
- Nurachmann Liu, Scott Hanson, Dennis Sylvester, David Blaauw, “On-Chip One-Time Random ID Generation Using Oxide Breakdown,” UM file number 4726.
- Sudhir Satapathy, Trevor Mudge, Dennis Sylvester, David Blaauw, “A Self Updating Least Recently Grant Arbitration Technique for Advanced Extended Interconnect,” UM file number 4727.
- Sudhir Satapathy, Trevor Mudge, Dennis Sylvester, David Blaauw, “A Fast Scalable Technique for Distributed Quality of Service Arbitration,” UM file number 4918.

Students

Ph.D. committees chaired:

Name	Project Area	Graduation/Status
Kanak Agarwal	On-chip interconnect modeling	2004 (IBM)
Himanshu Kaul	Global signaling strategies for nanometer VLSI	2004 (Intel)
Ashish Srivastava	Statistical CAD tools for low power	2005 (Magma)
Sarvesh Kulkarni	Multi-voltage CAD and design	2006 (Intel)
Matt Guthaus	On-chip clock network optimization (co-chair)	2006 (UC-Santa Cruz)
Harmander Singh	Robust low-power design techniques	2006 (Intel)
Youngmin Kim	Exploiting design-process interactions	2007 (UNIST-Korea)
Saumil Shah	Parametric yield optimization tools	2007 (Magma)
Jie Yang	Design for manufacturability	2007 (AMD)

Eric Karl	Dynamic reliability management (co-chair)	2008 (Intel)
Yu-Shiang Lin	Ultra-low energy communication/computation	2008 (IBM)
Scott Hanson	Towards cubic millimeter computing	2008 (Ambiq Micro)
Jae-Sun Seo	Circuits for fast on-chip global signaling	2009 (IBM)
Vineeth Veetil	Fast Monte Carlo-based statistical CAD	2010 (Synopsys)
Mingoo Seok	Extreme power-constrained IC design	2010 (Texas Instruments)
Vivek Joshi	Variability-driven CAD	Candidate (expected 05/11)
Greg Chen	Millimeter-scale sensing systems	Candidate (expected 05/11)
Daeyeon Kim	Robust low-voltage memories	Candidate (expected 09/11)
Dave Fick	3D energy efficient computing (co-chair)	Candidate (expected 05/12)
Matthew Fojtik	Adaptive error-correcting circuit design	Pre-candidate (expected 05/13)
M. Hassan Ghaed	Wireless communication in implantable devices	Pre-candidate (expected 05/13)
Dongsuk Jeon	Energy efficient signal processing for VLSI	Pre-candidate (expected 05/14)
Gyouho Kim	CMOS imaging in sensor nodes (co-chair)	Pre-candidate (expected 05/14)
Mahmood Barangi	Low-power analog/digital conversion	Pre-candidate (expected 05/14)
Yen-Po Chen	TBD	Pre-candidate (expected 05/15)
Suyoung Bang	TBD	Pre-candidate (expected 05/15)

M.S. students supervised:

Robert Bai	Level-converting flip-flops for dual-Vdd CMOS	2003 (UBS bank)
Tejasvi Kachru	Statistical timing analysis of sequential elements	2006 (AMD)
Michelle Chang	Fast CAD algorithms using multi-processing	2010

Ph.D. committees served on:

Biju Edamana	Control strategies for micro-robots	Candidate
Youngmin Park	Synthesizing analog/RF designs	Candidate
Hongtao Zhong	Multicore processing for single threaded apps	Candidate
Geoffrey Blake	Transactional memory	Candidate
Jorge Pernillo	High-speed analog/digital converters	Candidate
Korey Sewell	Architectures for network processors	Candidate
Rach Liu	Integrated circuits for security	Candidate
Amir Hormati	Compilers for streaming applications	Candidate
Prashant Singh	Reliability monitoring for nanoscale CMOS	Candidate
Ron Dreslinski	Low power microarchitectures	Candidate
Dongjin Lee	Clock network optimization	Candidate
Puneet Gupta	Design-manufacturing interface	2006 (University of California, San Diego)
Bulusu Anand	DTMOS for scaled low-voltage circuits	2006 (External examiner, Indian Institute of Tech., Bombay)
Ahmed Youssef	Power management for microprocessors	2008 (External examiner, University of Waterloo)

Javid Jaffari	Statistical timing analysis	2010 (External examiner, University of Waterloo)
Do Anh Tuan	Low voltage SRAM	2010 (External examiner, Nanyang Technological University)
Stevan Vlaovic	x86 microarchitecture performance simulation	2002
Mikhail Smelyanskiy	Approaches to efficient software pipelining	2003
Koushik Das	Robust low-power circuits in PD-SOI	2003
Nam Sung Kim	Low-power cache architecture and design	2004
Conrad Zeisler	Energy recovering pipelines	2004
Saurabh Adya	Algorithms for VLSI layout design	2004
Rahul Rao	Low-power SOI VLSI design	2004
Erik Hallnor	Advanced cache architectures	2004
Aseem Agarwal	Statistical static timing analysis	2005
David Oehmke	Novel register file architectures	2005
Daniel Ernst	Virtual global communication	2005
Dongwoo Lee	Leakage current analysis and reduction	2005
R. Venkatasubramanium	Fault detection in wireless networks	2005
Alan Drake	Local resonant clocking for low-power	2005
Jay Sivagnaname	Pseudo-NMOS SOI circuit design	2005
Leyla Nazhandali	Architecture for sensor networks	2006
Allen Cheng	Application specific instruction sets	2006
Jia-Yi Chen	Low-power wireless transceivers	2006
Rajeev Rao	Uncertainty-aware CAD tools	2006
Sunghyun Park	High-speed analog/digital converters	2006
Maher Mneimneh	Microprocessor verification	2006
Michael Geiger	Region-based caching	2006
Rajiv Ravindran	Compiler-driven memory power optimization	2007
Yoonna Oh	Constructive logic and layout synthesis	2007
Bo Zhai	Ultra-low power processors and memories	2007
Mini Nanua	Circuit modeling for signal integrity	2007
Taeho Kgil	Energy efficient servers using 3D integration	2007
Robert Senger	Micropower ASIC design techniques	2007
Sanjay Pant	On-chip power distribution networks	2008
Junyoung Park	High-speed CMOS serial links	2008
Jeff Ringenberg	Benchmarking for future microarchitectures	2008
Mark Ferriss	Low-power transmitters for sensor networks	2008
Debbie Marr	Simultaneous multithreading microarchitectures	2008
Stephen Plaza	Hierarchical logic synthesis and verification	2008
Kaviraj Chopra	Statistical CAD: Analysis and optimization	2008
Yuan Lin	Software-defined radio	2008
Smita Krishnaswamy	Design and test of logic circuits under uncertainty	2008

Carlos Tokunaga	Circuit design for security applications	2008
Jaeyoung Kang	Successive-approximation ADCs	2008
Shidhartha Das	Variation-tolerant circuit design	2009
Ali Saidi	Full-system critical path analysis	2009
Shahrzad Naraghi	Analog/digital converters	2009
Jarrod Roy	Placement and routing in nanometer CMOS	2009
Ravi Gandikota	Crosstalk noise analysis in VLSI	2009
Lisa Hsu	Cache resource allocation in multiprocessors	2009
Chun Chieh Lee	Low-power analog/digital converters	2009
Brian Cline	Design for manufacturability	2010
David Papa	Physical synthesis tools	2010
Cheng Zhuo	CAD for reliability	2010
David Roberts	Fault-tolerant architectures	2010

Postdoctoral scholars supervised:

Dr. Mike Wieckowski	Low-voltage memory and voltage regulators	2007-2010
Dr. Scott Hanson	Ultra-low power microcontrollers	2009-2010

Professional and Honor Societies

- Fellow, Institute of Electrical and Electronics Engineers (IEEE)
- Member, Association for Computing Machinery (ACM)
- Member, Eta Kappa Nu (HKN)

Publications

h-index = 38 (Google Scholar, January 2011)

Books and book chapters

1. A. Srivastava, D. Sylvester, and D. Blaauw, *Statistical Analysis and Optimization for VLSI: Timing and Power*, Springer Publishers, New York, 2005.
2. D. Lee, B. Zhai, D. Blaauw, and D. Sylvester, "Static leakage reduction through simultaneous V_t /Tox and state assignment," in *Ultra Low-Power Electronics and Design*, E. Macii, Ed. Kluwer Academic Publishers, Boston, 2004.
3. L. Stok, R. Puri, S. Bhattacharya, J. Cohn, D. Sylvester, A. Srivastava, and S.H. Kulkarni, "Pushing ASIC performance in a power envelope," in *Closing the Power Gap Between ASIC and Custom*, D. Chinnery and K. Keutzer, ed., Springer Publishers, New York, 2007.
4. S.H. Kulkarni, A. Srivastava, D. Sylvester, and D. Blaauw, "Power optimization techniques using multiple supply voltages," in *Closing the Power Gap Between ASIC and Custom*, D. Chinnery and K. Keutzer, ed., Springer Publishers, New York, 2007.

Journal publications

5. V. Veetil, K. Chopra, D. Blaauw, and D. Sylvester, "Fast statistical static timing analysis using smart Monte Carlo techniques," accepted for publication in *IEEE Transactions on Computer-Aided Design*.

6. J-S. Seo, D. Blaauw, and D. Sylvester, "Crosstalk-aware PWM-based on-chip links with self-calibration in 65nm CMOS," accepted for publication in *IEEE Journal on Solid-State Circuits*.
7. M. Seok, S. Hanson, D. Blaauw, and D. Sylvester, "Sleep mode analysis and optimization with minimal-sized power gating switch for ultra-low V_{dd} operation," accepted for publication in *IEEE Transactions on VLSI Systems*.
8. M. Seok, G. Chen, S. Hanson, M. Wiecekowsi, D. Blaauw, and D. Sylvester, "Mitigating variability in near-threshold computing," accepted for publication in *IEEE Journal on Emerging Topics in Circuits and Systems*.
9. J-S. Seo, D. Sylvester, D. Blaauw, H. Kaul, and R. Krishnamurthy, "A robust edge encoding technique for energy-efficient multi-cycle interconnect," *IEEE Transactions on VLSI Systems*, pp. 264-273, February 2011.
10. G.K. Chen, S. Hanson, D. Blaauw, and D. Sylvester, "Circuit design advances for wireless sensing applications," *Proceedings of the IEEE*, pp. 1808-1827, December 2010. **[invited]**
11. G. Chen, D. Sylvester, D. Blaauw, and T. Mudge, "Yield-driven near-threshold SRAM design," *IEEE Transactions on VLSI Systems*, pp. 1590-1598, November 2010.
12. V. Joshi, B. Cline, D. Sylvester, D. Blaauw, and K. Agarwal, "Mechanical stress aware optimization for leakage power reduction," *IEEE Transactions on Computer-Aided Design*, pp. 722-736, May 2010.
13. S. Hanson, Z. Foo, D. Blaauw, and D. Sylvester, "A 0.5V sub-microwatt CMOS image sensor with pulse-width modulation read-out," *IEEE Journal of Solid-State Circuits*, pp. 759-767, April 2010.
14. R.G. Dreslinski, M. Wiecekowsi, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold voltage scaling for energy optimal systems," *Proceedings of the IEEE*, pp. 253-266, February 2010. **[invited]**
15. R. Gandikota, K. Chopra, D. Blaauw, and D. Sylvester, "Victim alignment in crosstalk-aware timing analysis," *IEEE Transactions on Computer-Aided Design*, pp. 261-274, February 2010.
16. H. Singh, R.M. Rao, D. Sylvester, R. Brown, and K. Nowka, "Dynamically pulsed MTCMOS with bus encoding for total power and crosstalk minimization," *IEEE Transactions on VLSI Systems*, pp. 166-170, January 2010.
17. R.R. Rao, V. Joshi, D. Blaauw, and D. Sylvester, "Circuit optimization techniques to mitigate the effects of soft errors in combinational logic," *ACM Transactions on Design Automation of Electronic Systems*, pp. 5:1-5:27, December 2009.
18. P. Singh, C. Zhou, E. Karl, D. Blaauw, and D. Sylvester, "Sensor driven reliability and wearout management," *IEEE Design & Test of Computers*, pp. 40-49, Nov/Dec 2009. **[invited]**
19. B. Zhai, S. Pant, L. Nazhandali, S. Hanson, J. Olson, A. Reeves, M. Minuth, R. Helfand, T. Austin, D. Sylvester, and D. Blaauw, "Energy efficient subthreshold processor design," *IEEE Transactions on VLSI Systems*, pp. 1127-1137, August 2009. [top 25 downloaded manuscripts, TVLSI 2009]
20. Y. Kim, D. Petranovic, and D. Sylvester, "Simple and accurate models for capacitance increment due to metal fill insertion," *IEEE Transactions on VLSI Systems*, pp. 1166-1170, August 2009.
21. S. Hanson, M. Seok, Y-S. Lin, Z. Foo, D. Kim, Y. Lee, N. Liu, D. Sylvester, and D. Blaauw, "A low voltage processor for sensing applications with picowatt standby mode," *IEEE Journal of Solid-State Circuits*, pp. 1145-1155, April 2009.
22. Y-S. Lin, D. Sylvester, and D. Blaauw, "Alignment independent chip-to-chip communication for sensor applications using passive capacitive signaling," *IEEE Journal of Solid-State Circuits*, pp. 1156-1166, April 2009.
23. F. Albano, Y-S. Lin, D. Blaauw, D. Sylvester, K.D. Wise, and A.M. Sastry, "A fully integrated microbattery for an implantable microelectromechanical system," *Elsevier Journal of Power Sources*, 185 (2), pp.1524-1532, December 2008.

24. B. Zhai, S. Hanson, D. Blaauw, and D. Sylvester, "A variation-tolerant sub-200mV 6-T subthreshold SRAM," *IEEE Journal of Solid-State Circuits*, pp. 2338-2348, October 2008.
25. P. Singh, J-S. Seo, D. Blaauw, and D. Sylvester, "Self-timed regenerators for high-speed and low-power on-chip global interconnect," *IEEE Transactions on VLSI Systems*, pp. 673-677, June 2008.
26. D. Sylvester, K. Agarwal, and S. Shah, "Variability in nanometer CMOS: Impact, analysis, and minimization," *Integration, the VLSI Journal*, vol. 41, no. 3, pp. 319-339, May 2008. **[invited]**
27. S. Hanson, B. Zhai, M. Seok, B. Cline, K. Zhou, M. Singhal, M. Minuth, J. Olson, L. Nazhandali, T. Austin, D. Sylvester, and D. Blaauw, "Exploring variability and performance in a sub-200mV processor," *IEEE Journal of Solid-State Circuits*, pp. 881-891, April 2008.
28. E-H. Toh, G. H. Wang, L. Chan, D. Sylvester, C.-H. Heng, G. Samudra, and Y.-C. Yeo, "Device design and scalability of a double-gate tunneling field-effect transistor with silicon-germanium source," *Japanese Journal of Applied Physics*, vol. 47, no. 4, pp. 2593-2597, April 2008.
29. E. Karl, D. Blaauw, D. Sylvester, and T. Mudge, "Multi-mechanism reliability modeling and management in dynamic systems," *IEEE Transactions on VLSI Systems*, pp. 476-487, April 2008.
30. S.H. Kulkarni, D. Sylvester, and D. Blaauw, "Design time optimization of post-silicon tuned circuits using adaptive body bias," *IEEE Transactions on Computer-Aided Design*, pp. 481-494, March 2008.
31. A. Srivastava, K. Chopra, S. Shah, D. Sylvester, and D. Blaauw, "A novel approach to perform gate-level yield analysis and optimization considering correlated variations in power and performance," *IEEE Transactions on Computer-Aided Design*, pp. 272-285, February 2008.
32. S. Hanson, M. Seok, D. Sylvester, and D. Blaauw, "Nanometer device scaling in subthreshold logic and SRAM," *IEEE Transactions on Electron Devices*, pp. 175-185, January 2008.
33. J. Lin, E.-H. Toh, C. Shen, D. Sylvester, C-H. Heng, G. Samudra, and Y-C. Yeo, "Compact HSPICE model for IMOS device," *IET Electronics Letters*, vol. 44, no. 2, pp. 91-92, January 17 2008.
34. P. Gupta, A.B. Kahng, D. Sylvester, and J. Yang, "Performance-driven optical proximity correction for mask cost reduction," *SPIE Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, pp. 031005-1 – 031005-8, July-September 2007.
35. H. Singh, K. Agarwal, D. Sylvester, and K. Nowka, "Enhanced leakage reduction techniques using intermediate strength power gating," *IEEE Transactions on VLSI Systems*, pp. 1215-1224, November 2007. [top 25 downloaded manuscripts, TVLSI 2008]
36. P. Gupta, A.B. Kahng, Y. Kim, and D. Sylvester, "Self-compensating design for reduction of timing and leakage sensitivity to systematic pattern dependent variation," *IEEE Transactions on Computer-Aided Design*, pp. 1614-1624, September 2007.
37. K. Agarwal, R.M. Rao, D. Sylvester, and R. Brown, "Parametric yield analysis and optimization in leakage dominated technologies," *IEEE Transactions on VLSI Systems*, pp. 613-623, June 2007.
38. F. Albano, M.D. Chung, D. Blaauw, D. Sylvester, K.D. Wise, and A.M. Sastry, "Design of an implantable power supply for an intraocular sensor, using POWER (Power Optimization for Wireless Energy Requirements)," *Elsevier Journal of Power Sources*, v. 170 (1), pp. 216-224, June 2007.
39. D. Sylvester and A. Srivastava, "Computer-aided design for low-power robust computing in nanoscale CMOS," *Proceedings of IEEE*, pp. 507-529, March 2007. **[invited]**
40. R.R. Rao, K. Chopra, D. Blaauw, and D. Sylvester, "Soft error rate computation of combinational logic using parameterized descriptors," *IEEE Transactions on Computer-Aided Design*, pp. 468-479, March 2007.
41. A. Srivastava, T. Kachru, and D. Sylvester, "Low-power design space exploration considering process variation using robust optimization," *IEEE Transactions on Computer-Aided Design*, pp. 67-79, January 2007.

42. D. Sylvester, D. Blaauw, and E. Karl, "ElastiC: An adaptive self-healing architecture for unpredictable silicon," *IEEE Design & Test of Computers*, special issue on process variation and stochastic design and test, pp. 484-490, Nov/Dec 2006.
43. D. Lee, D. Blaauw, and D. Sylvester, "Runtime leakage minimization through probability-aware optimization," *IEEE Transactions on VLSI Systems*, pp. 1075-1088, October 2006.
44. R.R. Rao, A. Devgan, D. Blaauw, and D. Sylvester, "Analytical yield prediction considering leakage/performance correlation," *IEEE Transactions on Computer-Aided Design*, pp. 1685-1695, September 2006.
45. P. Gupta, A.B. Kahng, P. Sharma, and D. Sylvester, "Gate-length biasing for runtime leakage control," *IEEE Transactions on Computer-Aided Design*, pp. 1475-1485, August 2006.
46. S.H. Kulkarni and D. Sylvester, "Power distribution techniques for dual Vdd circuits," *Journal of Low Power Electronics*, pp. 217-229, August 2006.
47. K. Agarwal, M. Agarwal, D. Sylvester, and D. Blaauw, "Statistical modeling of VLSI interconnect for physical design optimization," *IEEE Transactions on Computer-Aided Design*, pp. 1273-1288, July 2006.
48. S. Hanson, B. Zhai, K. Bernstein, D. Blaauw, A. Bryant, L. Chang, K. Das, W. Haensch, E. Nowak, and D. Sylvester, "Ultra low-voltage, minimum energy CMOS", *IBM Journal of Research and Development*, pp. 469-490, July/September 2006.
49. K. Agarwal, D. Sylvester, and D. Blaauw, "Modeling and analysis of crosstalk noise in coupled RLC interconnects," *IEEE Transactions on Computer-Aided Design*, pp. 892-901, May 2006.
50. A. Sultania, D. Sylvester, and S. Sapatnekar, "Gate oxide leakage and delay tradeoffs for dual-Tox circuits," *IEEE Transactions on VLSI Systems*, pp. 1362-1375, December 2005.
51. R.R. Rao, H. Deogun, D. Blaauw, and D. Sylvester, "Bus encoding for total power reduction using a leakage-aware buffer configuration," *IEEE Transactions on VLSI Systems*, pp. 1376-1383, December 2005.
52. H. Kaul, D. Sylvester, M. Anders, and R. Krishnamurthy, "Design and analysis of spatial encoding circuits for peak power reduction in on-chip buses," *IEEE Transactions on VLSI Systems*, pp. 1225-1238, November 2005.
53. B. Zhai, D. Blaauw, D. Sylvester, and K. Flautner, "The limit of dynamic voltage scaling and extended DVS," *IEEE Transactions on VLSI Systems*, pp. 1239-1252, November 2005.
54. Y. Cao, X. Yang, X. Huang, and D. Sylvester, "Switch-factor based loop RLC modeling for efficient timing analysis," *IEEE Transactions on VLSI Systems*, pp. 1072-1078, September 2005.
55. R.R. Rao, A. Devgan, D. Blaauw, and D. Sylvester, "Modeling and analysis of parametric yield under power and performance constraints," *IEEE Design & Test of Computers*, special issue on design and test methodologies for scaled technologies, pp. 376-385, July-August 2005. **[invited]**
56. D. Lee, D. Blaauw, and D. Sylvester, "Static leakage reduction through simultaneous V_t /Tox and state assignment," *IEEE Transactions on Computer-Aided Design*, pp. 1014-1029, July 2005.
57. Y. Cao, X. Huang, D. Sylvester, T-J. King, and C. Hu, "Impact of on-chip frequency-dependent $R(f)$ $L(f)$ on digital and RF design," *IEEE Transactions on VLSI Systems*, pp. 158-162, January 2005.
58. H. Kaul, D. Sylvester, and D. Blaauw, "Performance optimization of critical nets through active shielding," *IEEE Transactions on Circuits and Systems I*, pp. 2417-2435, December 2004.
59. S.H. Kulkarni and D. Sylvester, "Fast and energy-efficient asynchronous level converters for multi-Vdd design," *IEEE Transactions on VLSI Systems*, pp. 926-936, September 2004.
60. K. Agarwal, D. Sylvester, and D. Blaauw, "A simple metric for slew rate of RC circuits based on two circuit moments," *IEEE Transactions on Computer-Aided Design*, pp. 1346-1354, September 2004.

61. A. Srivastava and D. Sylvester, "Minimizing total power by simultaneous Vdd/Vth assignment," *IEEE Transactions on Computer-Aided Design*, pp. 665-677, May 2004.
62. H. Kaul and D. Sylvester, "Low-power global IC communication based on transition-aware global signaling," *IEEE Transactions on VLSI Systems*, pp. 464-476, May 2004.
63. D. Lee, D. Blaauw, and D. Sylvester, "Gate oxide leakage current analysis and reduction for VLSI circuits," *IEEE Transactions on VLSI Systems*, pp. 155-166, February 2004.
64. R.R. Rao, A. Srivastava, D. Blaauw, and D. Sylvester, "Statistical analysis of subthreshold leakage current for VLSI circuits," *IEEE Transactions on VLSI Systems*, pp. 131-139, February 2004.
65. K. Agarwal, D. Sylvester, and D. Blaauw, "Effective capacitance based driver output model for on-chip RLC interconnects," *IEEE Transactions on Computer-Aided Design*, pp. 128-134, January 2004.
66. Y. Cao, M. Orshansky, D. Sylvester, T. Sato, and C. Hu, "SPICE up your MOSFET modeling: presenting a new paradigm of predictive MOSFET modeling for early circuit design innovation," *IEEE Circuits and Devices*, pp. 17-23, July 2003.
67. T. Sato, Y. Cao, K. Agarwal, D. Sylvester, and C. Hu, "Bi-directional closed-form transformation between on-chip coupling noise waveforms and interconnect delay change curves," *IEEE Transactions on Computer-Aided Design*, pp. 560-572, May 2003.
68. Y. Cao, C. Hu, X. Huang, A.B. Kahng, I. Markov, M. Oliver, D. Stroobandt, and D. Sylvester, "Improved a priori interconnect predictions and technology extrapolation in the GTX system," *IEEE Transactions on VLSI Systems*, pp. 3-14, Feb. 2003.
69. Y. Cao, X. Huang, N. Chang, S. Lin, O.S. Nakagawa, W. Xie, D. Sylvester, and C. Hu, "Effective on-chip inductance modeling for multiple signal lines and application to repeater insertion," *IEEE Transactions on VLSI Systems*, pp. 799-805, Dec. 2002.
70. D. Sylvester and H. Kaul, "Power-driven challenges in nanometer design," *IEEE Design & Test of Computers*, pp. 12-22, Nov/Dec. 2001.
The above paper was also included in a 2002 special report on design and test strategies compiled by the editors of IEEE Design and Test.
71. T. Sato, D. Sylvester, Y. Cao, and C. Hu, "Accurate in-situ measurement of peak noise and delay change induced by interconnect coupling," *IEEE Journal of Solid-State Circuits*, pp. 1587-1591, Oct. 2001.
72. D. Sylvester and C. Hu, "Analytical modeling and characterization of deep submicron interconnect," *Proceedings of IEEE*, pp. 634-664, May 2001. **[invited]**
73. D. Sylvester and K. Keutzer, "Microarchitectures for systems on a chip in small process geometries," *Proceedings of IEEE*, pp. 467-489, April 2001. **[invited]**
74. D. Sylvester and K. Keutzer, "A global wiring paradigm for deep submicron design," *IEEE Transactions on CAD*, pp. 242-252, February 2000.
75. D. Sylvester and K. Keutzer, "Rethinking deep submicron circuit design," *IEEE Computer*, November 1999, pp. 25-33.
76. O.S. Nakagawa, D. Sylvester, J.G. McBride, and S-Y. Oh, "Closed-form modeling of on-chip crosstalk noise in deep-submicron ULSI interconnect," *Hewlett-Packard Journal*, pp. 39-45, August 1998.
77. J.C. Chen, D. Sylvester, and C. Hu, "An on-chip interconnect capacitance characterization method with sub-femto-farad resolution," *IEEE Transactions on Semiconductor Manufacturing*, pp. 204-210, May 1998.
78. D. Sylvester, J.C. Chen, and C. Hu, "Investigation of interconnect capacitance using charge-based capacitance measurement (CBCM) technique and 3-D simulation," *IEEE Journal of Solid-State Circuits*, pp. 449-453, March 1998.

79. B.W. McGaughy, J.C. Chen, D. Sylvester, and C. Hu, "A simple method for on-chip sub-femto-farad interconnect capacitance measurement," *IEEE Electron Device Letters*, pp. 21-23, January 1997.

Conference publications

80. M. Seok, D. Jeon, C. Chakrabarti, D. Blaauw, and D. Sylvester, "Pipeline strategy for improving optimal energy efficiency in ultra-low voltage design," *ACM/IEEE Design Automation Conference*, in press, 2011.
81. D. Jeon, M. Seok, C. Chakrabarti, D. Blaauw, and D. Sylvester, "Energy-optimized high-performance FFT processor," *IEEE International Conference on Acoustics, Speech, and Signal Processing*, in press, 2011.
82. D. Fick, R.G. Dreslinski, B. Giridhar, G. Kim, S. Seo, M. Fojtik, S. Satpathy, Y. Lee, D. Kim, N. Liu, M. Wiecekowski, G. Chen, T. Mudge, D. Sylvester, and D. Blaauw, "Design and Implementation of Centip3De, a 7-layer Many-Core System," *ACM/IEEE Design Automation Conference, DAC/ISSCC student design contest award winner*, in press, 2011.
83. D. Kim, G. Chen, M. Fojtik, M. Seok, D. Blaauw, and D. Sylvester, "A 1.85fW/bit ultra low leakage 10T SRAM with speed compensation scheme," *IEEE International Symposium on Circuits and Systems*, in press, 2011.
84. G. Chen, M. Wiecekowski, D. Blaauw, and D. Sylvester, "A dense 45nm half-differential SRAM with lower minimum operating voltage," *IEEE International Symposium on Circuits and Systems*, in press, 2011.
85. M. Wiecekowski, G. Chen, D. Kim, D. Blaauw, and D. Sylvester, "A 128kb high density portless SRAM using hierarchical bitlines and thyristor sense amplifiers," *IEEE International Symposium on Quality Electronic Design*, in press, 2011.
86. C-H. Chen, Y. Kim, Z. Zhang, D. Blaauw, D. Sylvester, H. Naeimi, and S. Sandhu, "A confidence-driven model for error-resilient computing," *ACM/IEEE Design, Automation, and Test in Europe*, in press, 2011.
87. Y. Lee, B. Giridhar, Z. Foo, D. Sylvester, and D. Blaauw, "A 660pW multi-stage temperature compensated timer for ultra-low power wireless sensor node synchronization," *IEEE International Solid-State Circuits Conference*, in press, 2011.
88. M. Seok, D. Jeon, C. Chakrabarti, D. Blaauw, and D. Sylvester, "A 0.27V, 30MHz, 17.7nJ/transform 1024-pt complex FFT core with super-pipelining," *IEEE International Solid-State Circuits Conference*, in press, 2011.
89. G. Chen, H. Ghaed, R. Ul-Haque, M. Wiecekowski, Y. Kim, G. Kim, D. Fick, D. Kim, M. Seok, K. Wise, D. Blaauw, and D. Sylvester, "A 1 cubic millimeter energy-autonomous wireless intraocular pressure monitor," *IEEE International Solid-State Circuits Conference*, in press, 2011.
90. Y. Lee, M-T. Chen, J. Park, D. Sylvester, and D. Blaauw, "A 5.42nW/kB retention power logic-compatible embedded DRAM with 2T dual-Vt gain cell for low power sensing applications," *IEEE Asian Solid-State Circuits Conference*, 2010.
91. V. Veetil, D. Blaauw, and D. Sylvester, "A lower bound computation method for evaluation of statistical design techniques," *IEEE/ACM International Conference on Computer-Aided Design*, pp. 562-569, 2010.
92. C. Zhuo, K. Agarwal, D. Sylvester, and D. Blaauw, "Active learning framework for post-silicon variation extraction and test cost reduction," *IEEE/ACM International Conference on Computer-Aided Design*, pp. 508-515, 2010.

93. V. Joshi, D. Blaauw, D. Sylvester, "Analysis and optimization of SRAM robustness for double patterning lithography," *IEEE/ACM International Conference on Computer-Aided Design*, pp. 25-31, 2010.
94. P. Singh, E. Karl, D. Sylvester, and D. Blaauw, "Dynamic NBTI management using a 45nm multi-degradation sensor," *IEEE Custom Integrated Circuits Conference*, 2010. **[Intel/CICC Student Scholarship Award]**
95. V. Joshi, M. Wieckowski, G.K. Chen, D. Blaauw, and D. Sylvester, "Analyzing the impact of double patterning lithography on SRAM variability in 45nm CMOS," *IEEE Custom Integrated Circuits Conference*, 2010. **[AMD/CICC Student Scholarship Award]**
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