There's been a lot of confusion over 1024 vs 1000, kbyte vs kbit, and the capitalization for each. Here, at last, is a single, definitive standard:

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>NAME</th>
<th>SIZE</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>kB</td>
<td>KILOBYTE</td>
<td>1024 bytes or 1000 bytes</td>
<td>1000 bytes during leap years, 1024 otherwise</td>
</tr>
<tr>
<td>KB</td>
<td>KELLY-BOOTLE STANDARD UNIT</td>
<td>1012 bytes</td>
<td>Compromise between 1000 and 1024 bytes</td>
</tr>
<tr>
<td>KiB</td>
<td>IMAGINARY KILOBYTE</td>
<td>1024.937528 bytes</td>
<td>Used in quantum computing</td>
</tr>
<tr>
<td>kb</td>
<td>INTEL KILOBYTE</td>
<td>1023.937528 bytes</td>
<td>Calculated on Pentium FPU</td>
</tr>
<tr>
<td>Kb</td>
<td>DRIVEMAKER'S KILOBYTE</td>
<td>CURRENTLY 908 bytes</td>
<td>Shrinks by 4 bytes each year for marketing reasons</td>
</tr>
<tr>
<td>KBa</td>
<td>BAKER'S KILOBYTE</td>
<td>1152 bytes</td>
<td>9 bits to the byte since you're such a good customer</td>
</tr>
</tbody>
</table>
EECS 370 Discussion

Exam 2

High: 97    Low: 10    Average 60.4
EECS 370 Discussion

Roadmap to end of semester

• Project 4 – Friday 12/6 (Due tonight at 11:59 w/ 3 slip days)

• Homework 7 – Tuesday 12/7 (Tomorrow)

• Final Exam – Monday 12/16 10:30 am – 12:30 pm
  make sure you don’t have a conflict...
EECS 370 Discussion

• Virtual Memory
  – Physically Addressed & Virtually Addressed
  – Hierarchical Page Tables

• Hard Drives
  – Overview
  – Access Time

• General Review
Virtual Memory

Concepts

Physical Addresses are in?

Virtual Addresses are in?

What does the TLB hold?
Virtual Memory

Concepts

Physical Addresses are in?
Hardware

Virtual Addresses are in?
Software

What does the TLB hold?
Physical Page Numbers
EECS 370 Discussion

Caches

Problem:

Where do we put the cache in a VM system?
Physically Addressed

Caches

CPU

TLB

Virtual Address

Physical Address

Cache
EECS 370 Discussion

Virtually Addressed

Caches

CPU

Cache

TLB

Virtual Address

Physical Address
Caches

Performance Problem

<table>
<thead>
<tr>
<th></th>
<th>Hit Rate</th>
<th>Access Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLB</td>
<td>99%</td>
<td>1 cycle</td>
</tr>
<tr>
<td>Cache</td>
<td>90%</td>
<td>1 cycle</td>
</tr>
<tr>
<td>Main Memory</td>
<td>99.99%</td>
<td>100 cycles</td>
</tr>
<tr>
<td>Disk</td>
<td>100%</td>
<td>1,000,000 cycles</td>
</tr>
</tbody>
</table>

Find memory latency for virtually addressed and physically addressed systems.
Effective Address

Cache Access
- **hit**: Data To Processor
- **miss**: TLB Lookup

TLB Lookup
- **hit**: Data To Processor
- **miss**: Page Table Walk

Page Table Walk
- **hit**: Memory Access
- **miss**: Update TLB

Memory Access
- **hit**: Data To Processor & Update Cache
- **miss**: Page Fault

Page Fault
- **Disk Access**: 10000s cycles
- **Update TLB**: 1 to 100s cycles (cached or not)

1 to 10s cycles
≤ 1 cycle
1 to 100s cycles (cached or not)
100s cycles
Hierarchical Page Tables

32-bit virtual addresses
Page Size: 8kB
Page Entry Size: 8B

How many levels of page tables must there be?

Where do each of the address bits go?
Hierarchical Page Tables

32-bit virtual addresses
Page Size: 8kB
Page Entry Size: 8B

How many levels of page tables must there be?

2 levels

Where do each of the address bits go?

10-bit superpage table, 9-bit subpage table, 13-bit page offset
EECS 370 Discussion
EECS 370 Discussion

Hard Drive Disk

Picture of one side of a platter

A - Sector

B - Track
EECS 370 Discussion

Hard Drive Disk

Access Time

• Seek Time – Moving to correct track
• Rotational Delay – Waiting for correct sector
• Transfer Time – Reading data from disk

• Wait Time & Controller Overhead – Additional delays

Is Random Access or Sequential Access better?
Hard Drive Disk

Access Time

5400 RPM
2 kB Sectors
512 Sectors per Track
8 ms Seek Time
No overhead

What is the time to access one sector?
EECS 370 Discussion

Exam Review

There will be two exam review sessions

Thursday, 4-6 pm, Chrysler 220
Sunday, 1-3 pm, Chrysler 220
EECS 370 Discussion

Exam Review

Discussion 1

• How does C work?
• LC2K Instructions
Exam Review

Discussion 2

- ARM Addressing
- Struct Data Layout
- Conditional Assembly
Exam Review

Discussion 3

• Caller / Callee Saved Registers

• Memory Layout

• Linking & Object Files

<table>
<thead>
<tr>
<th>Memory Stack</th>
<th>FP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Return Address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Previous Frame Pointer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Callee Saved Registers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Local Variables</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spilled Registers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Caller Saved Registers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Outgoing Parameters</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
EECS 370 Discussion

Exam Review

Discussion 4

• Floating Point

• Finite State Machines

• Combinational Logic

• Sequential Logic
Exam Review

Discussion 5

- Single Cycle Datapath
LC2Kx Datapath Implementation

Diagram of LC2Kx Datapath Implementation, showing the flow of data through various components such as Instruction memory, Register file, ALU, and Data memory. The diagram also includes a Control ROM and a 3x8 decoder.
EECS 370 Discussion

Exam Review

Discussion 6

• Multi Cycle Datapath
EECS 370 Discussion

Multi Cycle Datapath
EECS 370 Discussion

Exam Review

Discussion 7

• Pipelined Processor

• Data Hazards
EECS 370 Discussion
Discussion 8

- Control Hazards
- Branch Prediction
Discussion 9

- Caches
EECS 370 Discussion

Exam Review

Discussion 10
• Exam Review

Discussion 11
• Virtual Memory

Discussion 12
• Virtual Memory
• Disks