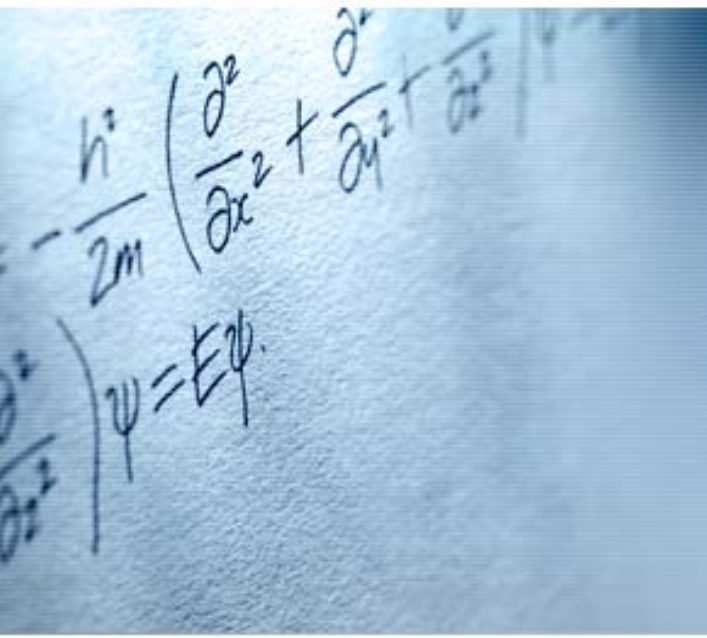

A New, High-Performance, Low-Power, Floating-Point Embedded Processor for Scientific Computing and DSP Applications

Simon McIntosh-Smith
Director of Architecture

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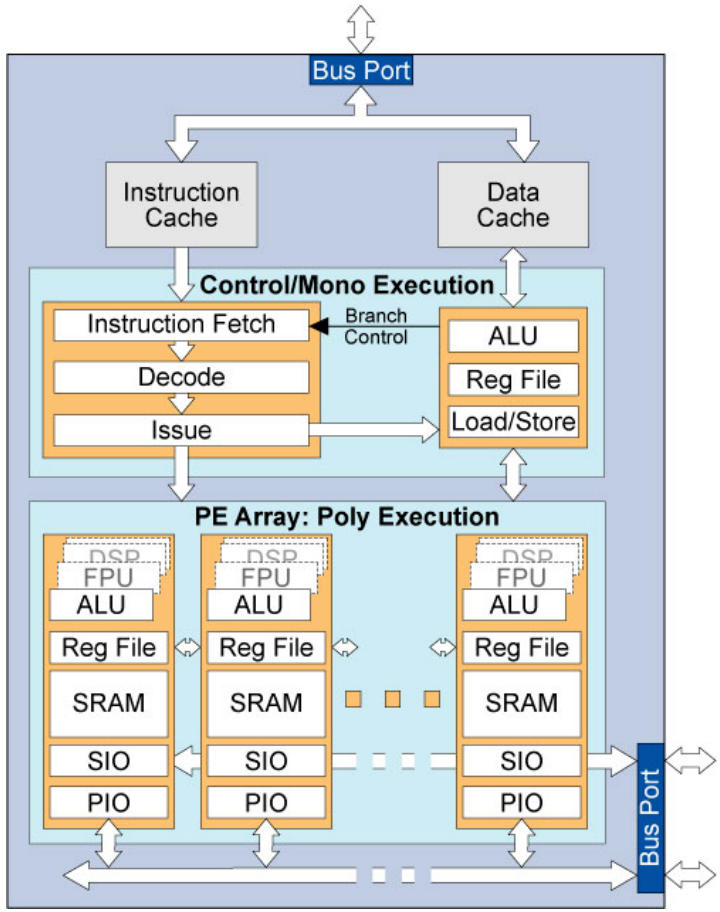
Multi-Threaded Array Processing Architecture



- Multi-Threaded Array Processor
  - Fully programmable in C
  - Hardware multi-threading
  - Extensible instruction set
- Scalable internal parallelism
  - Array of processing elements (PEs)
  - Compute, bandwidth scale together
  - From 10s to 1,000s of PEs
  - Built-in PE redundancy
- High performance, low power
  - ~10 GFLOPS/watt
- Multiple high-speed I/O channels

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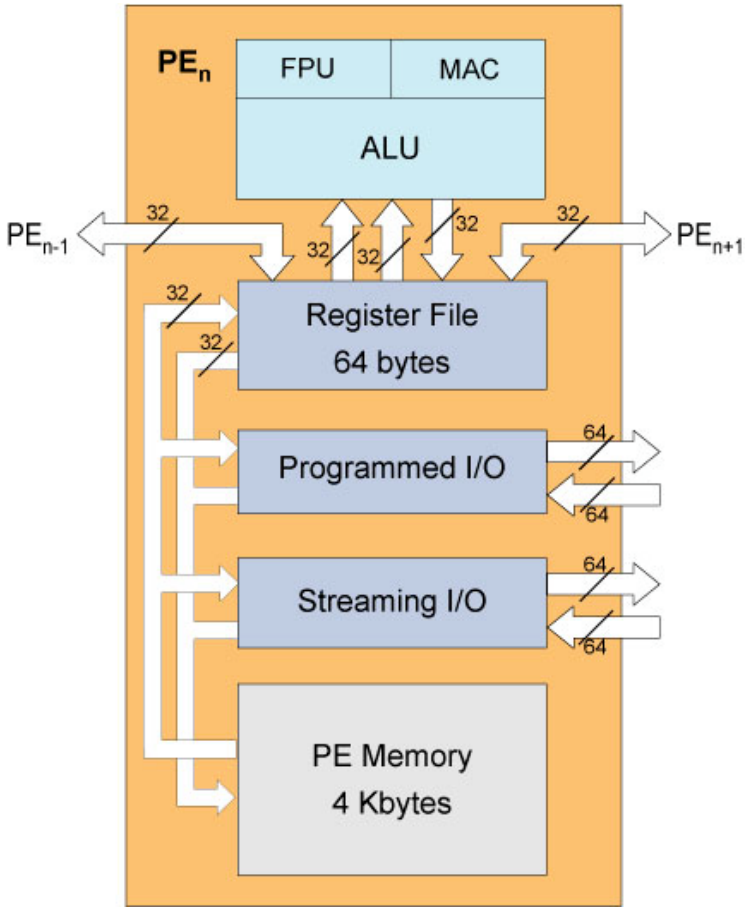
Processing Elements



- PEs are highly optimised execution units
  - ALU, MAC, FPU
  - High-bandwidth, multiport register file
  - High bandwidth per PE DMA (PIO, SIO)
  - Closely coupled SRAM for data
- 64 PEs at 200MHz
  - 25.6 GFLOPS
  - 51.2 Gbyte/s bandwidth to PE memory
  - 12,800 MIPS
- Supports multiple data types
  - 8, 16, 24, 32-bit, ... fixed-point arithmetic
  - 32-bit IEEE floating-point arithmetic

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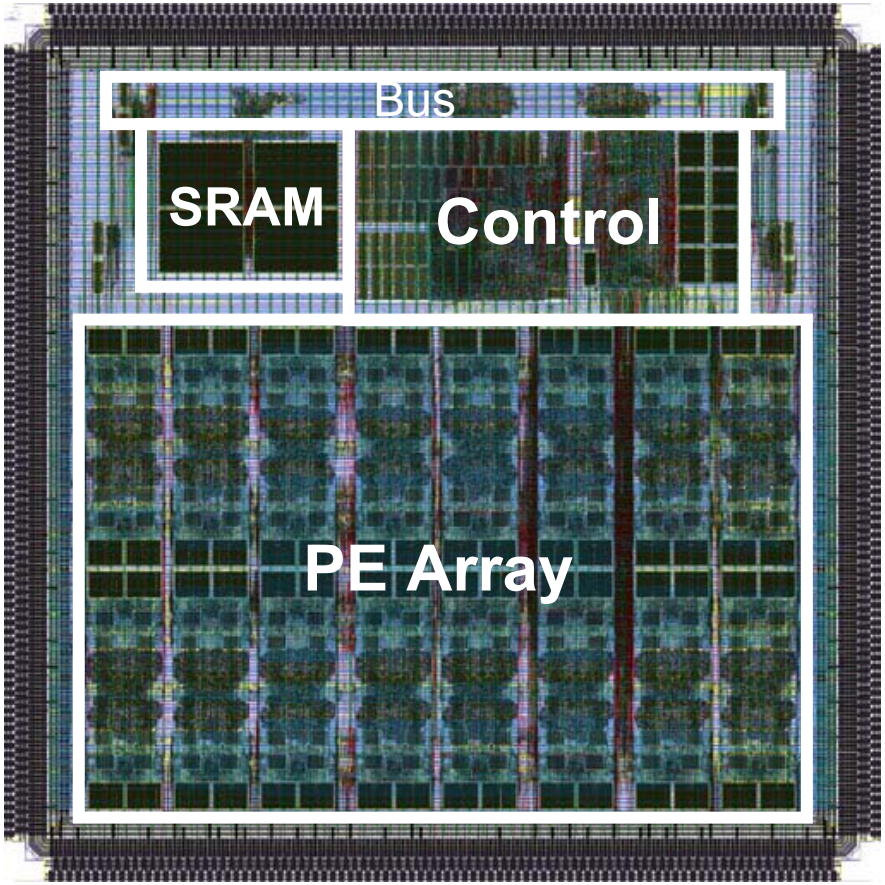
CS301 Up Close



- Multi-Threaded Array Processor
  - 25.6 GFLOPS
  - 3W worst-case, 2W typical
  - 200MHz
  - 64 PEs, 4 Kbytes each
- ClearConnect bus
  - 64-bit full duplex
  - 1.6 Gbyte/s each direction
  - 2x 0.8-Gbyte/s bridge ports
- Scratchpad memory
  - 128 Kbytes of SRAM
- Availability
  - Sampling Q4 2003

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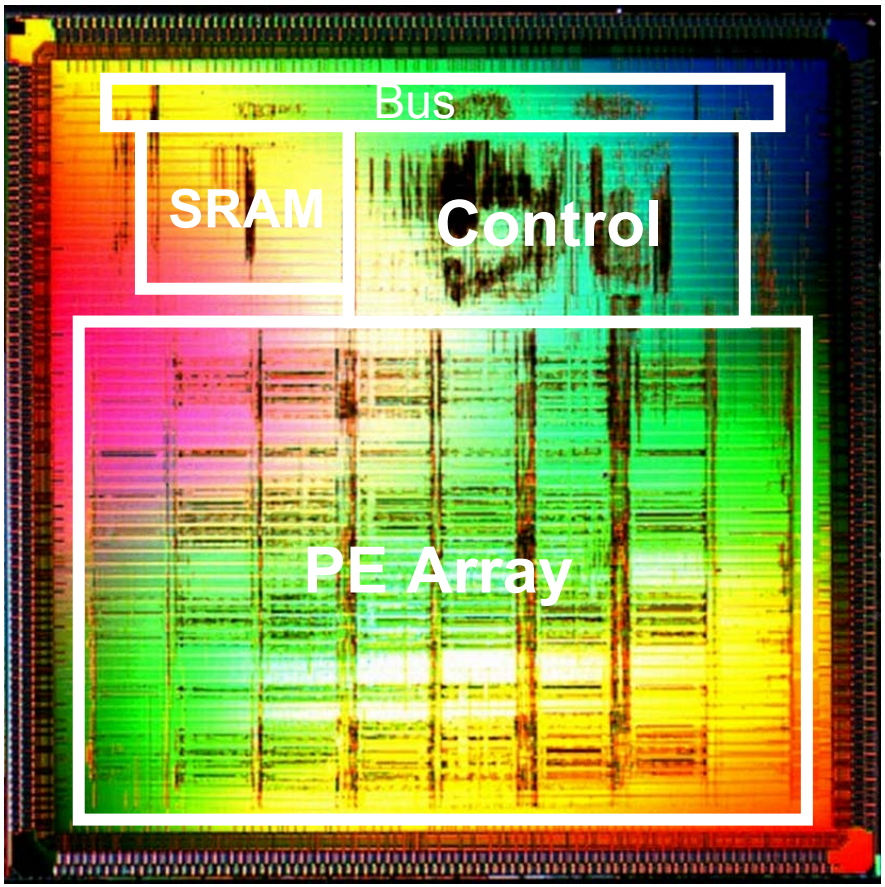
CS301 Up Close



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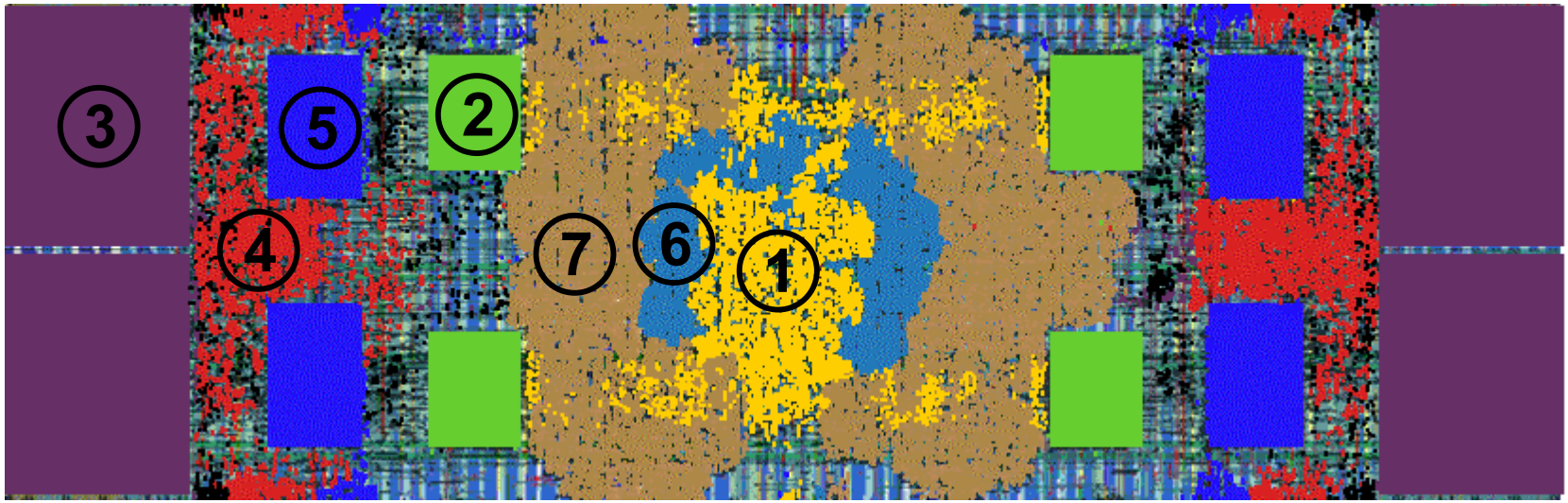
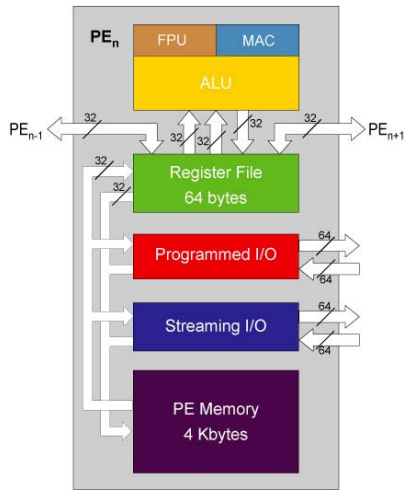
4 PEs - Array Building Block



1. ALUs
2. Register files
3. PE memories
4. PIO
5. SIO
6. Integer MACs
7. FPUs



* Captured using Magma's Blast Fusion®

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CS301 Facts and Figures

- IBM 0.13µ FSG process, 8-layer metal (copper)
- Standard cell library, fully synthesized design
- 8.5 x 8.5mm active logic area — 72mm^2
- 41 million transistors (32% logic, 68% memory)
- 1.2V core, 2.5V I/O (3.3V tolerant)
- 343 signal pins (235 mission mode, 108 diagnostic)
- Plastic PBGA package

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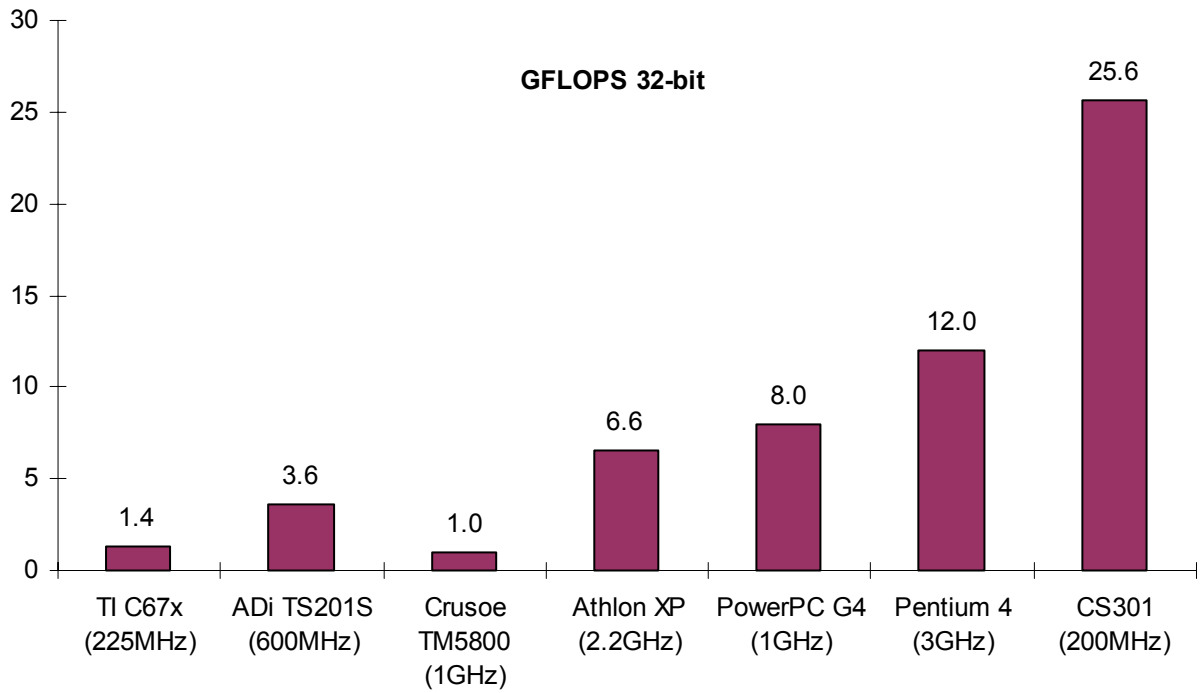
Peak GFLOP Comparison

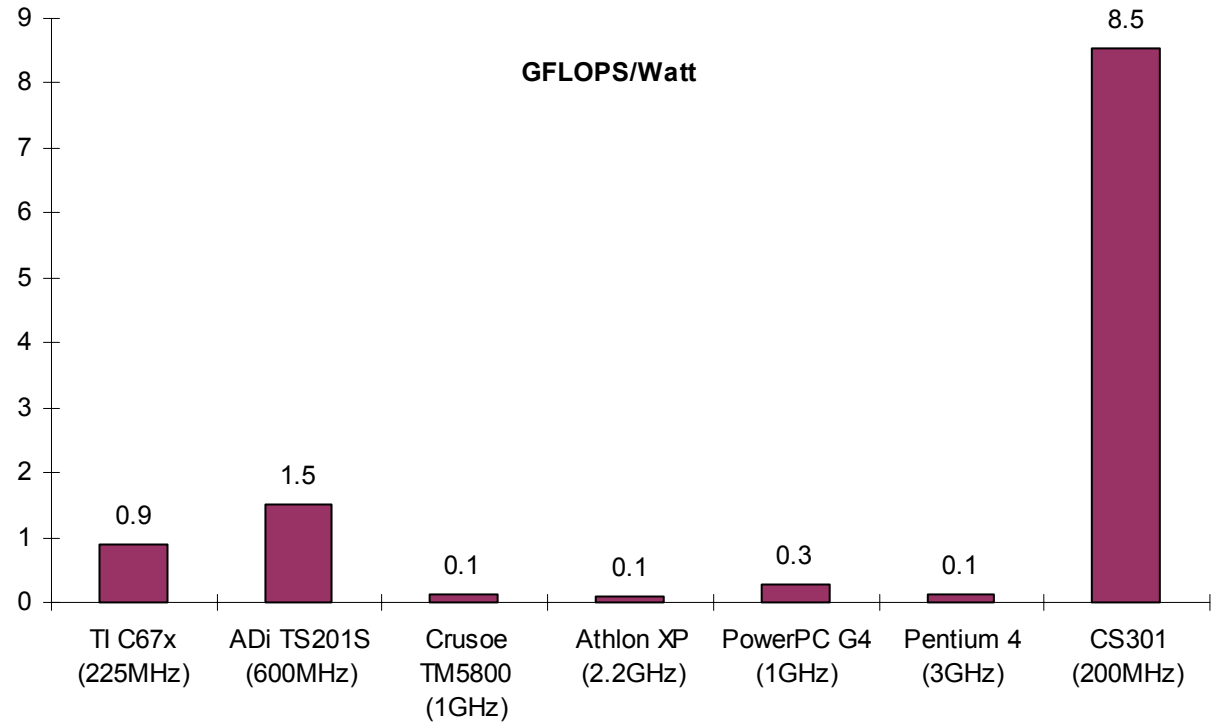


CS301 can accelerate, amongst others:

- High-performance computing tasks in PC and blade server systems
- Embedded DSP applications

Sources: vendor websites

GFLOPS Per Watt Comparison



CS301's high performance and low power enables:

- New levels of density in PC and blade server systems
- New levels of performance in embedded DSP applications.

Sources: vendor websites

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FFT Performance Comparison

LOCKHEED MARTIN

WorldScape Defense

- Lockheed Martin has benchmarked two applications with optimised code supplied by WorldScape Defence on the CS301 cycle-accurate simulator:

- A 1024-point, complex, floating-point FFT, 8 FFTs performed in parallel
- Pulse compression: an FFT, a complex multiply by a stored reference FFT, and an IFFT, with 8 pulse compressions performed in parallel

Processor	Clock	Power	FFT/sec /Watt	Pulse Compressions /sec/Watt
PowerPC 7410	400 MHz	8.3W	3,052	782
ClearSpeed **CS301**	**200 MHz**	**2.0W***	**56,870**	**24,980**
Improvement	**----**	**----**	**18.6 X**	**31.9 X**

* Measured on gate level sim with Magma's Blast Rail

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Development Environment

Software Development Kit (SDK)

- C compiler, assembler, libraries, visual debugger, etc.
- Instruction-set and cycle-accurate simulators
- Available for Windows, Linux, and Solaris
- Development boards, early silicon available from Q4 2003

Application development support

- Reference source code for various applications
- Consult directly with *ClearSpeed's* experts
- Consultancy and optimised code from *ClearSpeed's* partners

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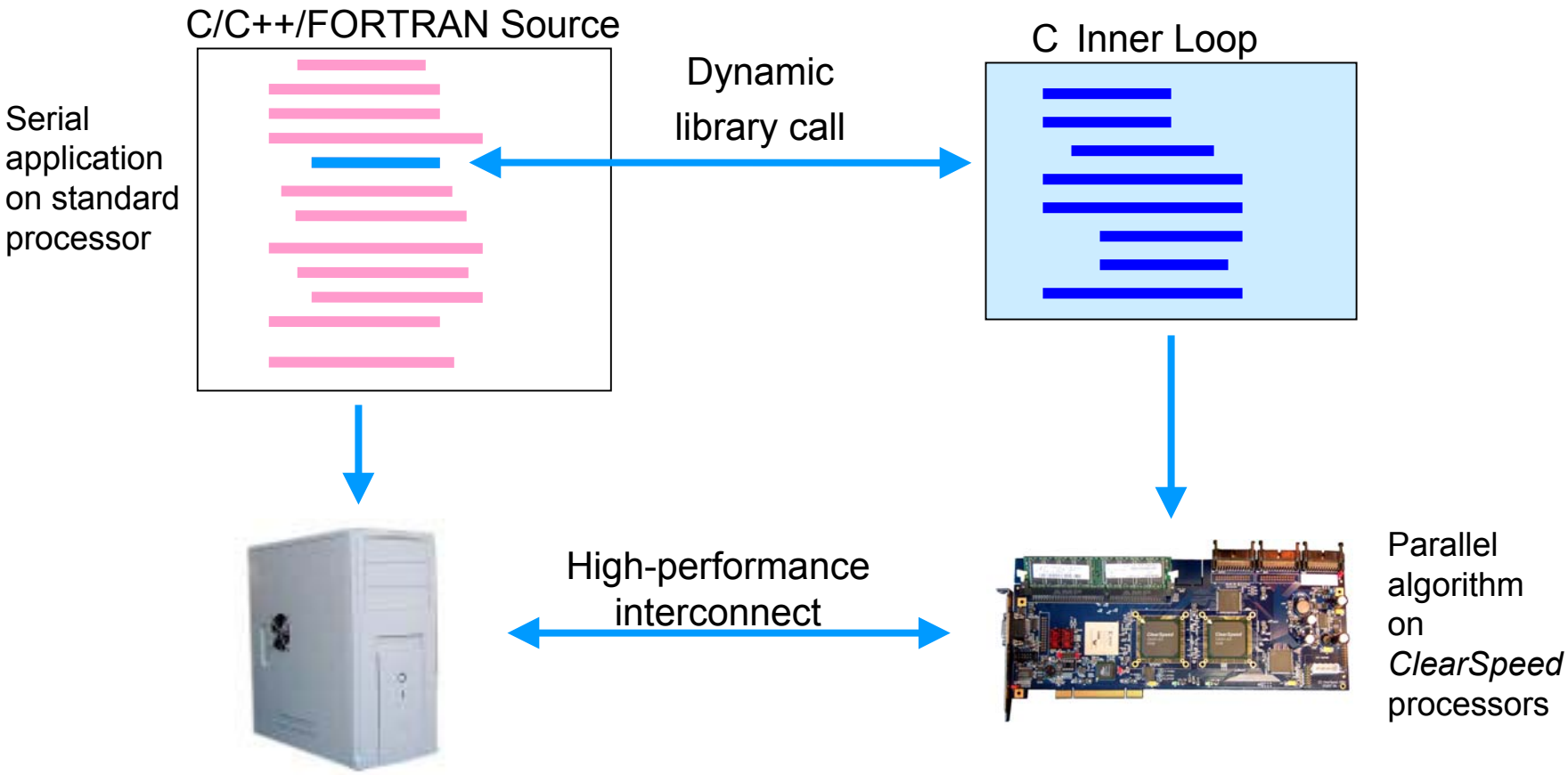
Accelerated Applications

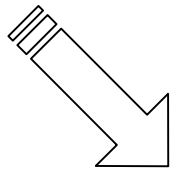
ClearSpeed's co-processor technology is designed to accelerate the *inner loops* of compute-intensive algorithms.



Porting C Code

```
float sum[N], a[N], b[N];

do {
  sum[i] = a[i] + b[i];
  i += 1;
} while (i<N)
```



```
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do {
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} while (i<N)
```

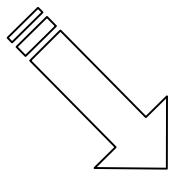

```
_do_while::
  ld     r_t1:p4f, r_i:m2u,  a;
  ld     r_t2:p4f, r_i:m2u,  b;
  add    r_t3:p4f, r_t1:p4f, r_t2:p4f;
  st     r_i:m2u,  r_t3:p4f, sum;
  add    r_i:m2u,  r_i:m2u,  4;
  j.if.lt r_i:m2u, r_Nx4:m2u, _do_while;
```

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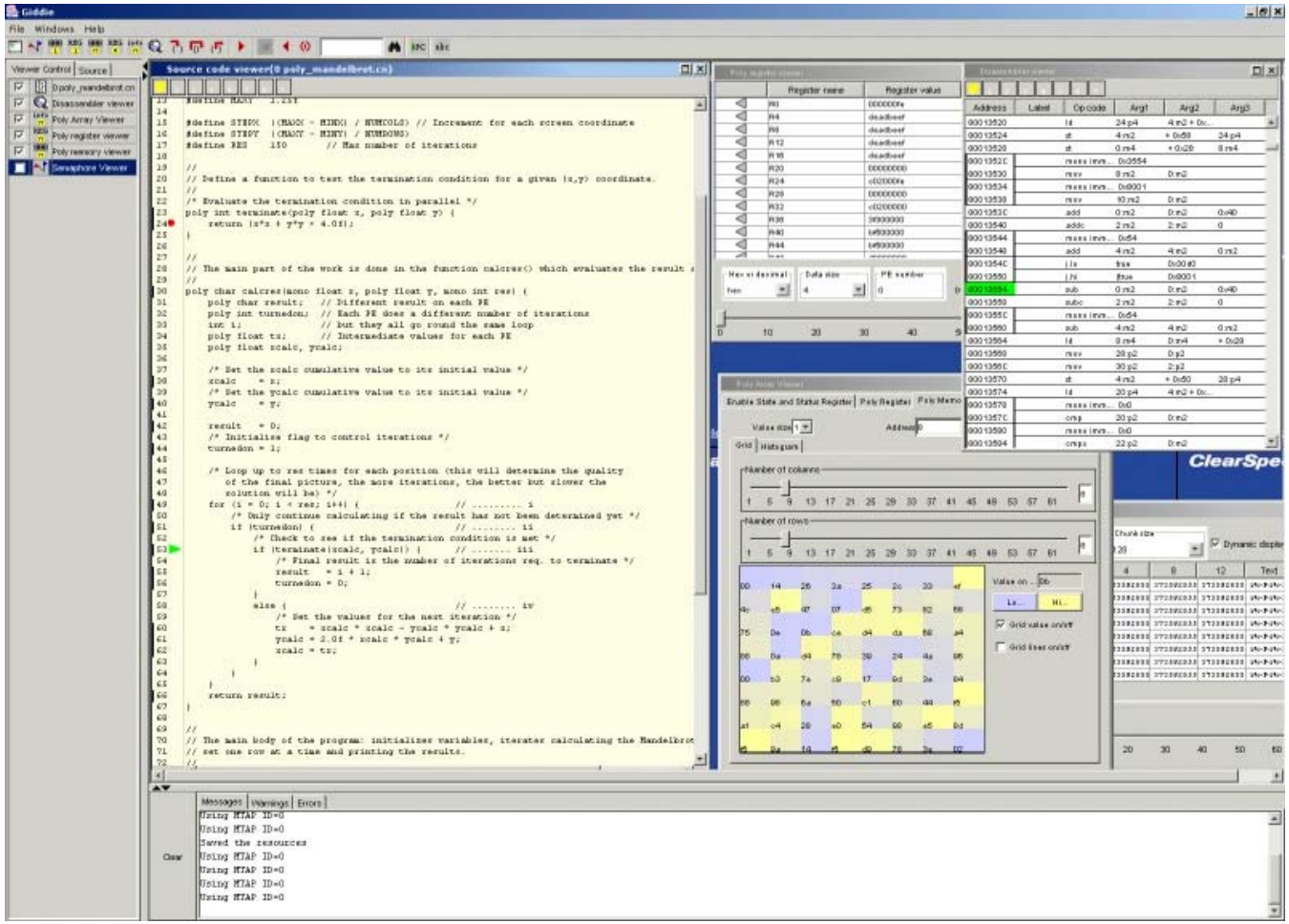
ClearSpeed Debugger



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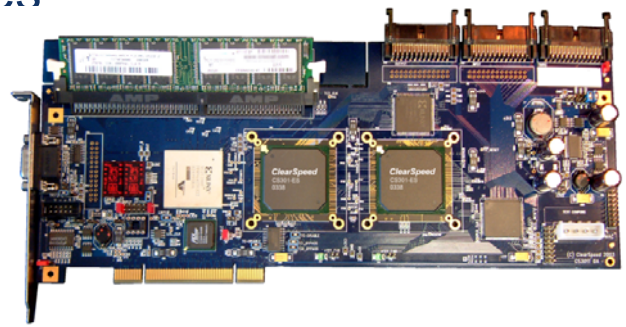
Systems Integration Examples

Laptop plug-in accelerator



PC plug-in accelerator

Coprocessors in a PC server*

Coprocessors in a blade server*

* Images courtesy of Angstrom Microsystems

ClearSpeed CS301 Summary

ClearSpeed's CS301 fully programmable accelerator delivers compelling floating-point performance and performance per watt.

- 25.6 GFLOPS
- 3W worst-case, 2W typical
- 8.5 GFLOPS/watt
- 3.2 Gbyte/s off-chip bandwidth
- Gluelessly daisy-chain multiple devices for higher performance
- Program in C with a familiar, simple programming model
- Sampling Q4 2003

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