

# BPS: Bug Positioning System

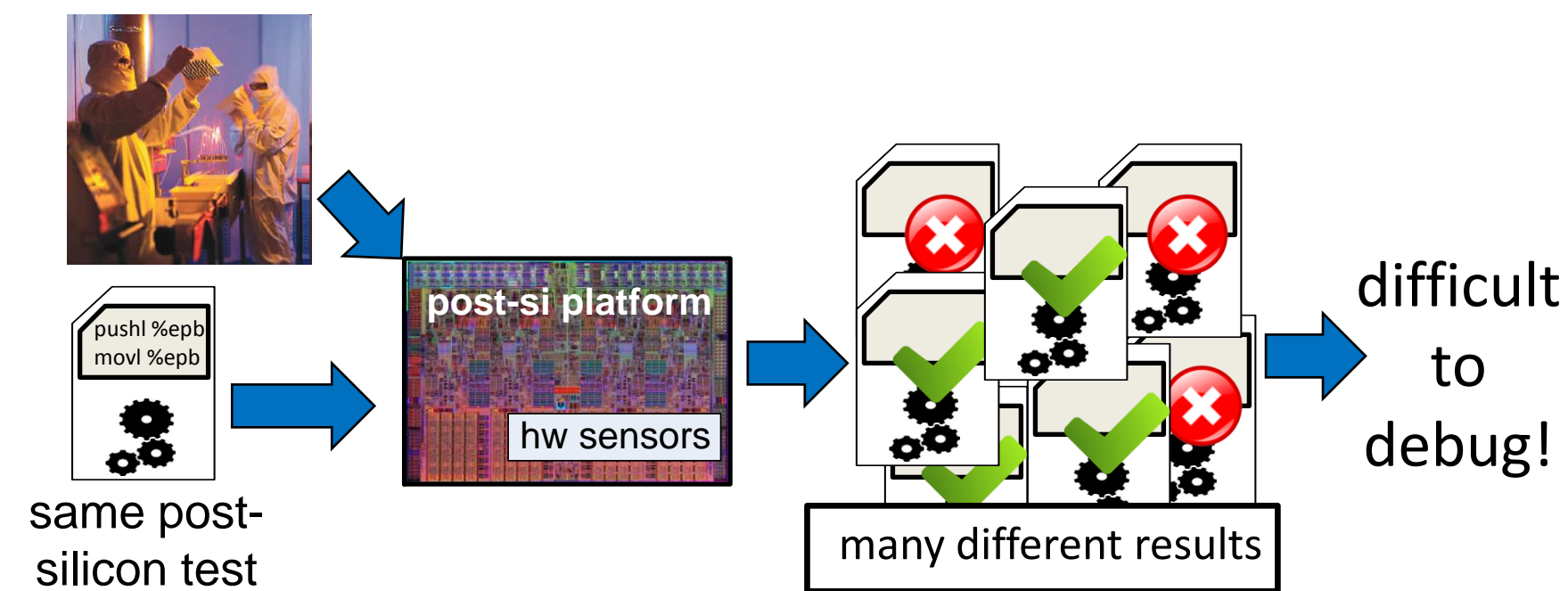


DAC 2011

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## Post-silicon debugging

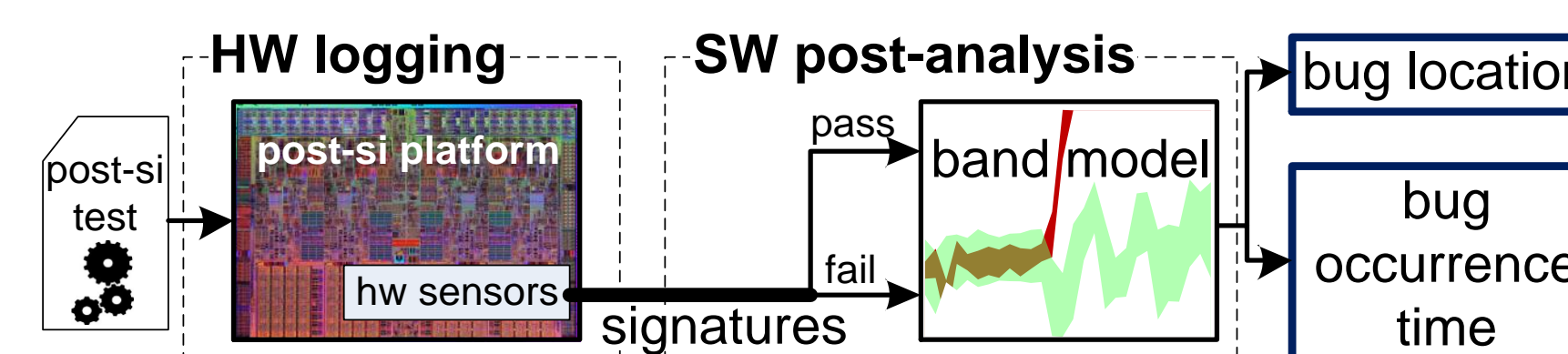
- The most challenging post-silicon bugs are intermittent:
  - A same test does not expose the bug in every run
  - Each run exhibits different behaviors



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## Post-silicon debugging with BPS

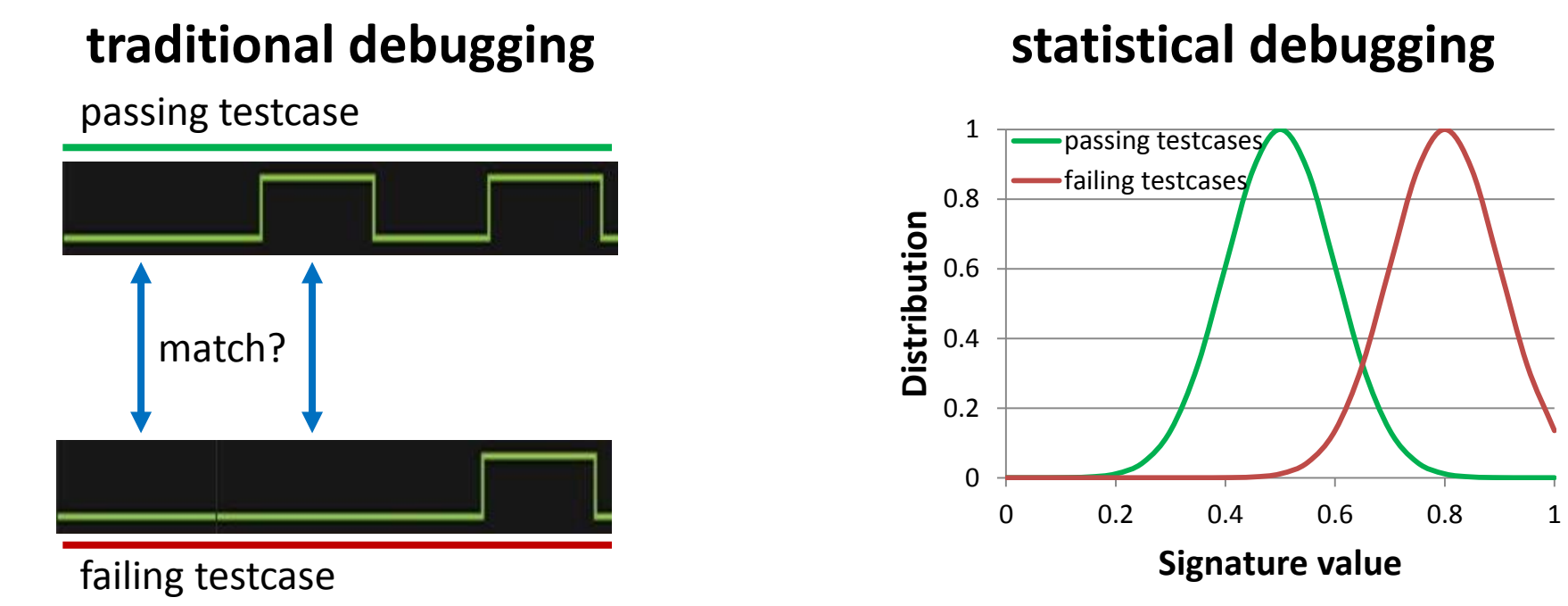
- Locate failures in time and space
  - Online hardware logging
  - Offline software post-analysis
- Environment: noisy, non-deterministic



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## Statistical approach

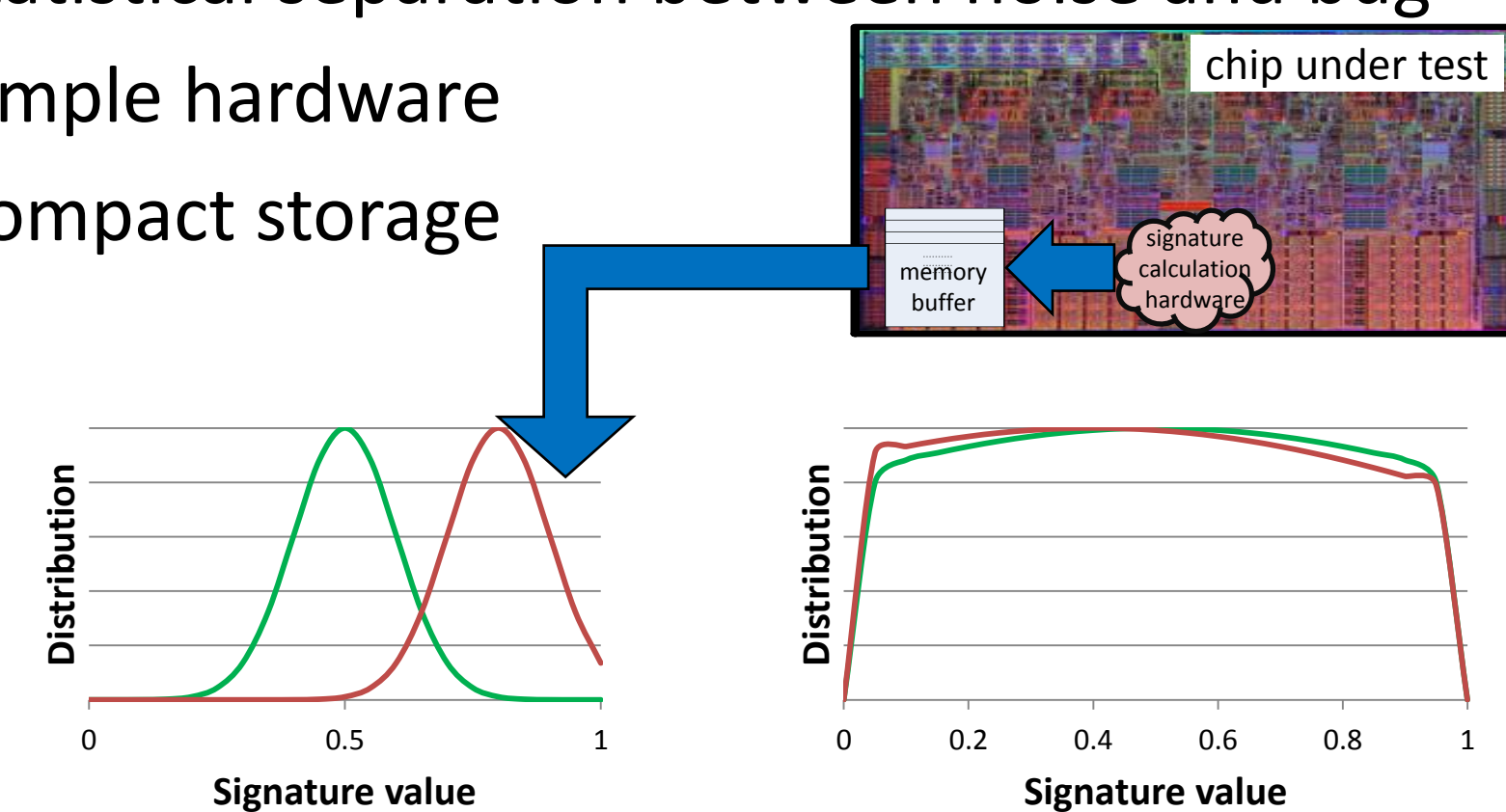
- Characterize signal activity statistically
- Multiple executions of a same tests are divided into two groups: passing and failing runs



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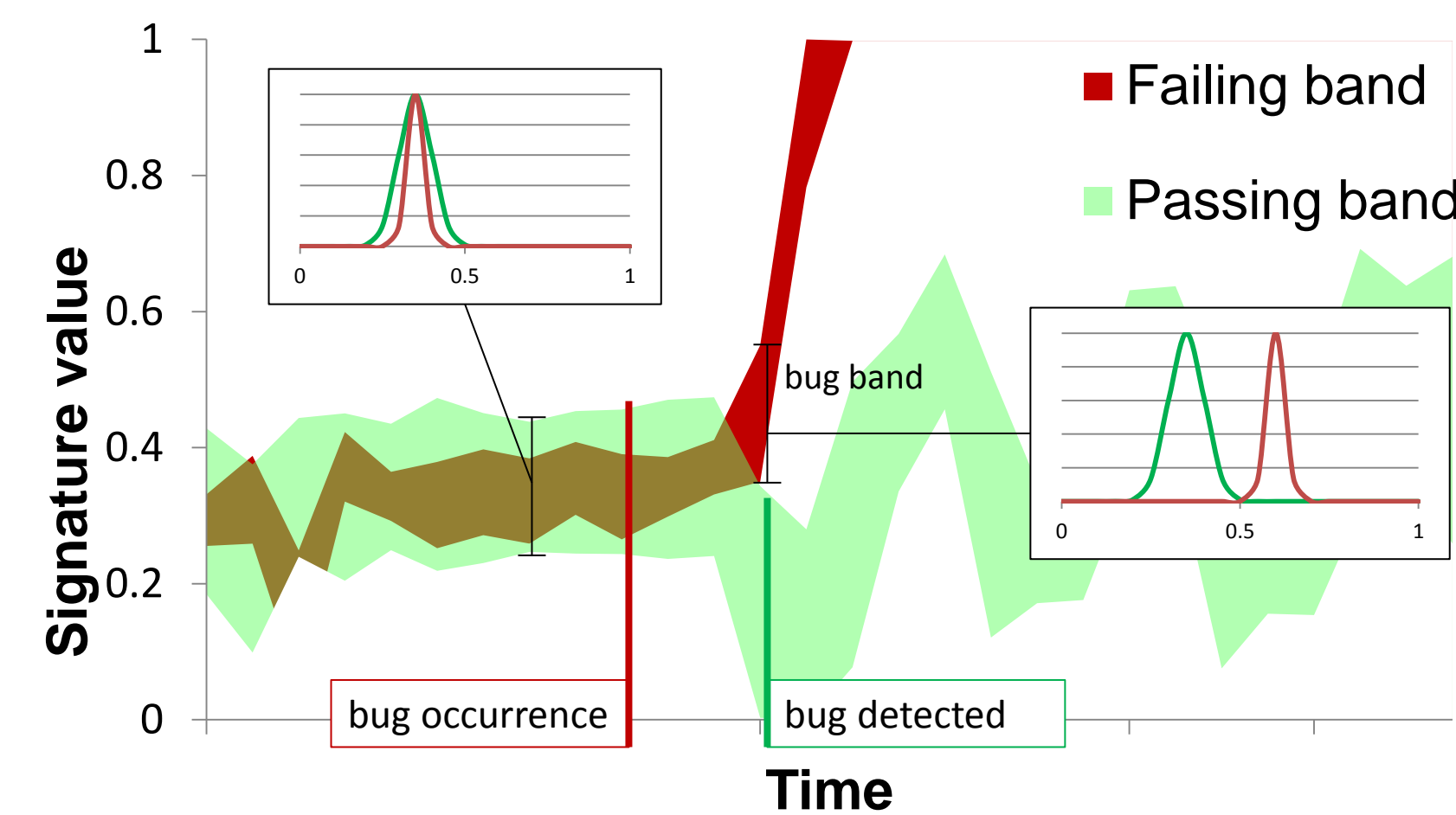
## Signature collection during testing

- Summarize signal value over time
- Statistical separation between noise and bug
- Simple hardware
- Compact storage



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## SW post-analysis: bug band model



behavior of 1 signal from the MEM stage of a 5-stage pipeline processor

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## Experimental Setup

- Test Platform**
  - OpenSPARC T2 processor
  - Monitored 41,744 control signals
- Non-determinism**
  - Variable memory delay, crossbar random traffic
- 10 bugs**
  - e.g., functional bug in PCX, electrical error in Xbar
- 10 testcases**
  - e.g., constrained random, floating point

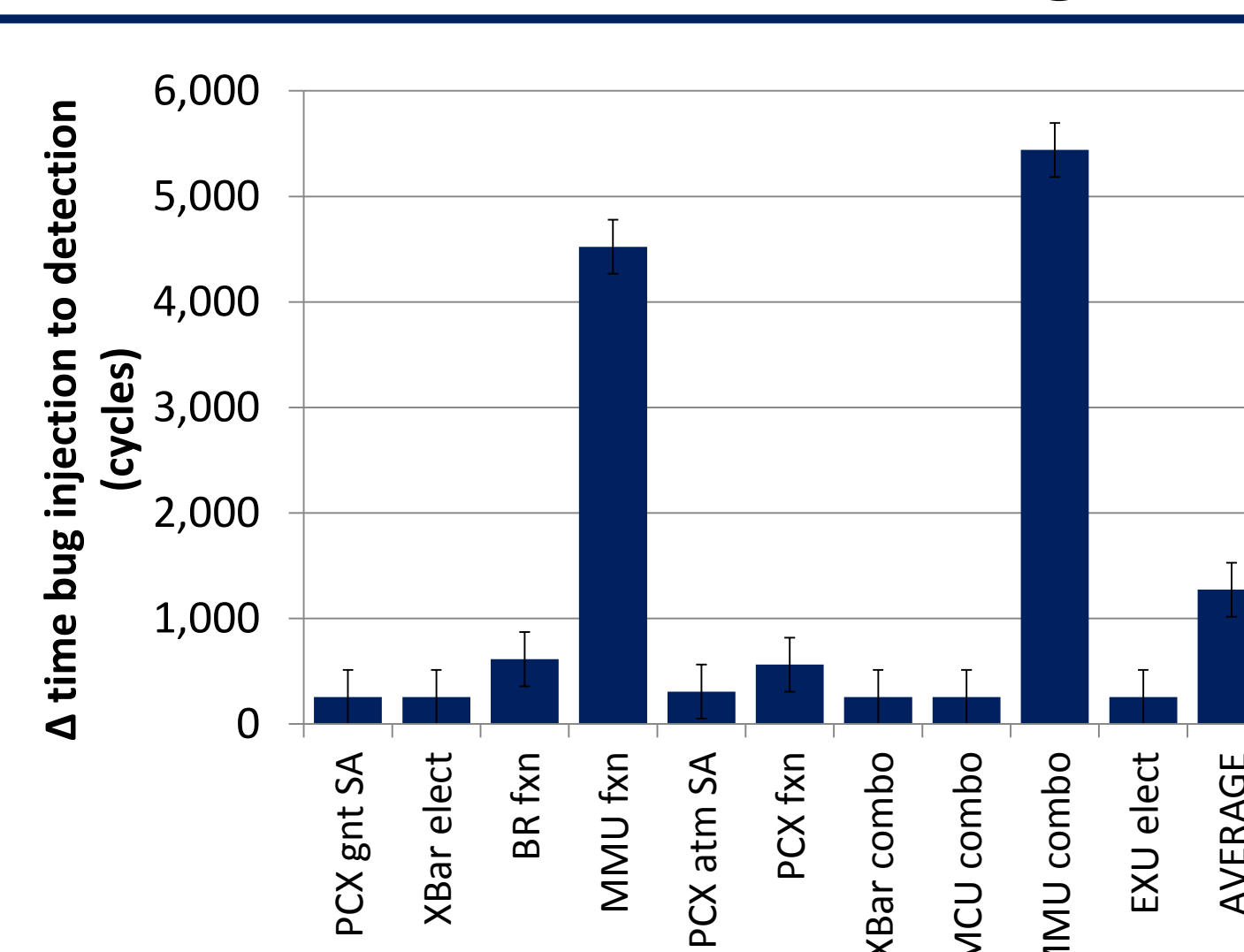
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## Signal Localization

	PCX gnt SA	Xbar elect	BR fxn	MMU fxn	PCX atm SA	PCX fxn	Xbar combo	MCU combo	MMU combo	EXU elect
blimp_rand	v+	v	/	/	v+	v+	v+	f.n.	v+	f.n.
fp_addsub	n.b.	f.p.	v	/	v	v+	f.p.	n.b.	v+	f.p.
fp_muldiv	n.b.	f.p.	v	/	v	v+	f.p.	f.p.	v+	f.p.
isa2_basic	n.b.	f.n.	v	b.	v+	v+	v+	v+	n.b.	f.n.
isa3_asr_pr	n.b.	v	v	v	v+	v	v+	v+	v	v
isa3_window	n.b.	v	v	b.	v+	v	f.n.	f.n.	n.b.	v
ldst_sync	n.b.	v+	v	/	v+	v+	v+	v+	v+	n.b.
mpgen_smc	n.b.	v+	v	/	v+	v+	v+	v+	v+	v+
n2_lsu_asi	n.b.	f.n.	v	n.	v+	v+	v+	v+	v+	n.b.
tlu_rand	n.b.	v+	v	/	v+	v+	v+	v+	v+	v+

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## Time to detect bug



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## Conclusion

- BPS automatically localizes bugs in time and space
- Effective for functional, electrical and manufacturing bugs
- Compact signatures minimize off-chip data transfer
- Submitted to ICCAD'11

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