**COURSE:** EECS 452  
**TITLE:** Digital Signal Processing Design Laboratory  
**PREREQUISITES:** EECS 280 & 306 or Graduate  

**CATALOG DESCRIPTION:** Architectures of single-chip DSP processors. Laboratory exercise using two state-of-the-art fixed-point processors; A/D and D/A conversion, digital waveform generators, and real-time FIR and IIR filters. Central to this course is a team project in real-time DSP design (including software and hardware).

**COURSE OBJECTIVES:**
1. To teach students the basics of using DSP chips to perform real-time digital signal processing;
2. To teach students how quantization and aliasing (due to sampling) affect real-time signal processing;
3. To teach students how to work in a team, how to produce a DSP chip design, and present their results.

**TOPICS COVERED:**
1. Aliasing and quantization
2. Sigma-Delta A/D and D/A
3. DSP chip architectures and programming language
4. FIR and IIR filter design
5. DSP chip programming and design for real-time DSP

**COURSE OUTCOMES [Program Outcomes Addressed]**
1. Ability to analyze the effects of quantization and aliasing in a real-time DSP system; [1,13]
2. Ability to design, using Matlab-based filter design techniques, FIR and IIR digital filters; [1,3,11,13]
3. Ability to design-test, to verify, to evaluate, and to benchmark a real-time DSP system; [2,3,5,11,13]
4. Ability to design DSP hardware in small teams, & present orally & in writing design results. [3,4,5,7]

**ASSESSMENT (Course outcomes)**
1. Weekly problem sets [1,2]
2. In-class exams [1,2]
3. Project oral & written reports [3,4]

**CLASS/LABORATORY SCHEDULE:**
- **LECTURES:** 3 per week @ 50 minutes.
- **LABORATORY:** 1 per week @ 3 hours.

**PROGRAM OUTCOMES ADDRESSED:** 1,2,3,4,5,7,11
**PROFESSIONAL COMPONENT ADDRESSED:** 13
**PREPARED BY:** Andrew E. Yagle on Nov. 25, 2004

**COURSE DESCRIPTION:** University of Michigan, College of Engineering, ELECTRICAL ENGINEERING PROGRAM