COURSE: EECS 427. **TITLE:** VLSI Design I. **PREREQUISITES:** EECS 270 and EECS 312. **ELECTIVE**

TEXTBOOK: J. Rabaey, A. Chandrakasan, B, Nikolic, *Digital Integrated Circuits: A Design Perspective*, Prentice-Hall, 2003.

CATALOG DESCRIPTION: Design techniques for rapid implementations of very large-scale integrated (VLSI) circuits, MOS technology and logic. Structured design. Design rules, layout procedures. Design aids: layout, design rule checking, logic, and circuit simulation. Timing. Testability. Architectures for VLSI. Projects to develop and lay out circuits.

COURSE OBJECTIVES:

1. To teach the students about the issues involved in the custom design of digital circuits.
2. To review CMOS processes and teach the students about static and dynamic logic.
3. To teach the students about low-power design at both the system and unit level.
4. To give the student experience doing significant design using mask-level layout tools.
5. To teach the student how to measure, test and evaluate his/her design.

COURSE OUTCOMES [Program Outcomes Addressed]

1. Ability to use a modern set of design tools to design a digital system. [1,2,3,11]
2. Ability to take a design from a given set of specifications to the complete simulation of a functioning design [2,3,5,11]
3. Ability to work in a group on a project too large for a single student. [2,3,5,7,11]
4. Students understand the issues involved with custom design processes.[1,2,3,5,9]

TOPICS COVERED:

1. Mask-level integrated circuit design with engineering design methodology
2. Design rules, layout and design flows
3. CMOS processes, static and dynamic logic
4. Interconnect design.
5. Low-power, timing, clock distribution, skew/jitter
6. Mask layout method and design rules;
7. Use of an HDL along with mask-level layout;
8. Circuit characterization/performance estimation;
9. Design for testability; robustness.
10. CMOS subsystem and system design.

PROGRAM OUTCOMES ADDRESSED: 1,3,9,10,11
PROFESSIONAL COMPONENT ADDRESSED: 13
PREPARED BY: Mark Brehob on January 24, 2005; modified by Andrew E. Yagle on April 11, 2005.

ASSESSMENT (Outcomes)

1. 4 in-class exams [4]
2. 8 homework designs [4]
3. Capstone project [1-4]

CLASS/DISCUSSION/LAB SCHEDULE:
LECTURES: 2 per week @ 80 minutes.
DISCUSSION: 1 per week @ 1 hour.
LABORATORY: Software (CAD) only

COURSE DESCRIPTION: University of Michigan, College of Engineering, ELECTRICAL ENGINEERING PROGRAM