**COURSE:** EECS 312  
**TITLE:** Digital Integrated Circuits  
**PREREQUISITES:** EECS 215 and EECS 320  
**CATALOG DESCRIPTION:** Design and analysis of static CMOS inverters and complex combinational logic gates. Dynamic logic families, pass-transistor logic, ratioed logic families. Sequential elements (latches, flip-flops). Bipolar-based logic; ECL, BiCMOS. Memories; SRAM, DRAM, EEPROM, PLA. I/O circuits and interconnect effects. Design project(s). Lecture, recitation and software labs.

**COURSE OBJECTIVES:**
1. To teach students analysis and design of static CMOS digital circuits, and to use Accusim software;
2. To develop a thorough understanding of static and dynamic characteristics (delay, power, density, noise immunity) of MOS-based logic families (CMOS, pseudo-NMOS, pass transistor, domino);
3. To teach operation and importance of memory structures (SRAM & DRAM) in large digital systems;
4. To provide students with required knowledge to make informed decisions on when to use different logic styles, and the tradeoffs inherent in those decisions;
5. To teach students how to analyze the effect of interconnect parasitics on circuit performance;

**TOPICS COVERED:**
1. Device fabrication & Accusim
2. CMOS inverter and gates: delay and power analysis
3. Dynamic logic: pass-transistor; domino, np-cmos
4. Sequential elements: flip-flops, latches
5. Memory structures: ROM, SRAM, DRAM
6. Wire parasites
7. Interconnect effects: noise, RC delays, repeaters, buffers

**COURSE OUTCOMES [Program Outcomes Addressed]**
1. Ability to analyze and design static inverters and combinatorial logic gates to determine and meet static & dynamic characteristics and specifications, e.g., noise margin, DC, power, delay; [3,5,11]  
2. Ability to compute delays using differential-equation-based methods for an inverter or gate; [1,14]  
3. Ability to calculate parasitic device capacitances from a given CMOS gate layout; [1,13]  
4. Ability to design and analyze dynamic combinatorial logic gates to meet a given speed target; [3,5,11]  
5. Ability to design and analyze sequential logic circuits (SR, JK flip-flops, D latches); [3,5]  
6. Ability to design and analyze bipolar-based logic gates and memory structures; [3,5]  
7. Ability to design a VLSI subsystem (e.g., adder, shifter, decoder) to meet performance specifications (e.g., delay, power, energy-delay product) using Accusim and techniques learned in the course [3,4,5]  

**PROGRAM OUTCOMES ADDRESSED:** 1,3,4,5,7,11  
**PROFESSIONAL COMPONENT ADDRESSED:** 13,14  
**PREPARED BY:** Andrew E. Yagle on Nov. 8, 2004

**ASSESSMENT (Course outcomes)**
1. 10 problem sets [1,2,3,4,5,6]  
2. 5 laboratories [4,5,6]; students work in pairs; written reports  
3. Design project; students work in teams to meet specifications [7]  
4. 3 examinations [1,2,3,4,5,6]  

**CLASS/LABORATORY SCHEDULE:**  
**LECTURES:** 2 per week @ 90 minutes.  
**LABORATORY:** 5 software out-of-class

**COURSE DESCRIPTION:** University of Michigan, College of Engineering, ELECTRICAL ENGINEERING PROGRAM