A Low-cost Audio Computer for Information Dissemination among Illiterate People Groups

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***Abstract*-We present LIT, a low power, low cost audio processor for information dissemination to and among illiterate people in developing regions. The 265K gate, 8 million transistor, 23mm^2, ARM Cortex M0 processor uses a novel memory hierarchy consisting of an on chip 128kB true LRU cache and off-chip flash. It is designed for efficient operation on Carbon Zinc batteries and has a high-level of integration to reduce cost.**

I. Introduction

Studies have shown that providing timely information about health, agriculture and education to populations in developing regions can greatly aid their livelihoods. The well-known One Laptop per Child (OLPC) initiative aimed to address this by connecting populations in developing regions to the internet [1]. However, this does not address 17% (824M) of the global population who are illiterate [2] (Fig. 1) and among the poorest in the world. To bridge this gap, we developed an SOC which forms the heart of an audio computer for information dissemination addressing an untapped market of $10B. Using only buttons, the audio computer allows users to navigate through menus, access information, program information collection through its radio links, and otherwise configure the device. In a pilot study where these audio computers were loaded with agricultural information and handed out to illiterate farmers, average crop production increased by 48% when compared to a control group [3].

The chief obstacle to disseminating these devices in an economically viable manner is the low purchasing power of the end users who typically subsist on $1-2/day. Hence the device must cost between $10–15, which means all the electronics, including PCB, speakers, microphone, radio, button, etc. must remain below approximately $6.

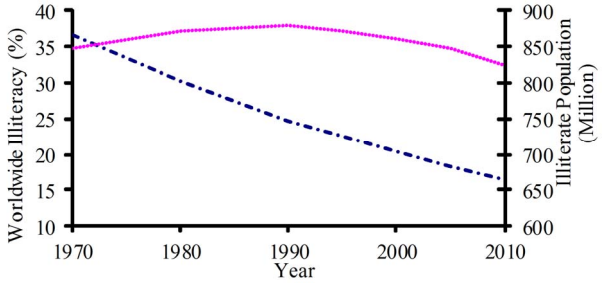


Fig. 1. Worldwide Literacy Rate: Percentage of illiterate people is decreasing, but total illiterate population is remaining constant

II. Proposed Solution

The Literacy Information Technology (LIT) chip (Fig. 2), tackles cost three ways: 1) A novel memory architecture with 128kB 4-way True LRU cache is directly backed by NAND Flash and removes the need for costly DRAM or NOR Flash. In addition, by integrating all analog components on-chip, including microphone amplifier, ADC, class-D amplifier, four LDOs, two voltage references, and two step-up converters, the total number of chips in the system is reduced to only three, saving cost and PCB size, which in turn reduces the plastic and handling costs of the final device. 2) For remaining components, we have made design choices that reduce cost. For instance, a coil is directly traced on the PCB for a near-field inductive link for close range communication between devices instead of costly USB connectors/wires. Also, 10 CDCs were integrated on- chip to allow push-membrane

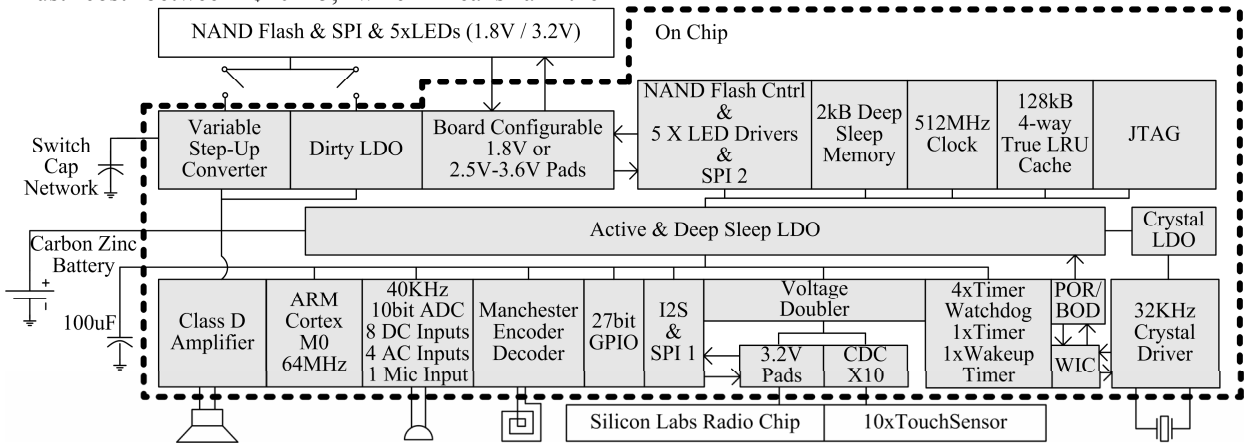


Fig. 2. System Level Diagram & Power Connectivity Showing On-Chip Components and On-Board Components. The NAND Flash Controller IO can be powered by either the Variable Charge Pump or the Dirty LDO depending whether a 3.2V or 1.8V NAND Flash is used. We accomplish this by connecting the Variable Charge Pump or Dirty LDO to the PAD Dirty VDD.

978-1-4673-1556-2/12/$31.00@2012 IEEE

buttons, which incur significant cost, to be replaced with capacitive sensors, also traced on the PCB.

A. Memory Hierarchy

LIT was implemented in 0.18um CMOS, measures 3.57mmX6.46mm (23.06mm^2), has 8 million transistors, 265K gates, with an expected cost < $1 in moderate volumes (Fig. 2). LIT's memory hierarchy is designed to accommodate the need for large code space (up to 16MB) while eliminating the need for expensive and power hungry NOR-flash or DRAM common in micro-controllers and processors. We implemented a large 128kB 4-way true LRU on-chip cache (48% of die area) directly backed by an off-chip NAND-flash (Fig. 3). A configurable pinned section of the cache prevents the lower portion of the address space from being evicted which is used for the OS and file-translation-layer. Upon a miss, the cache causes a precise fault and code in the fault handler loads data from NAND flash into the cache. The pinned section guarantees that fault handling code is never evicted. A consequence of the pinned region is that we must use true LRU, since pseudo LRU cannot provide a fallback address to evict if the returned LRU-way is in the pinned region. The cache uses an explicit data write back architecture since programs that cause cache thrashing would otherwise wear out the NAND flash. Hence, modifiable data is also stored in the pinned section.

Upon boot, the processor loads cache loading software from a 512B boot ROM to fill the cache. Upon a miss, a software handler fetches data from NAND flash and stores it in the cache. When the processor enters Deep Sleep mode, a routine is stored in either a dedicated 2kB of SRAM and the entire cache is power gated or in part of the cache purposely left awake in order to save energy. This routine is used to check the validity of the wake up event (such as touch sensor activity) and execute a cache refill routine if the event is determined to be valid in order for the processor to emerge from deep sleep. The cache consumes an additional 1uA in Deep Sleep if 8kB of memory is left awake and 7.2uA if all 128kB is left awake.

B. Power Operational Modes

LIT was designed to have 3 operational modes: Active, Standby and Deep Sleep, to reduce power draw. It was designed to maximize lifetime when powered by Carbon Zinc batteries, prevalent in developing regions. Unlike Alkaline batteries which have a steep cutoff voltage at 2.2V, Carbon Zinc batteries tend to degrade over a larger voltage range (Fig. 5). To extract maximum energy, we use low drop out regulators and a two phase regulation scheme: 1) At high battery voltages, LDOs regulate the battery to the 1.8V core supply; 2) Below 1.9V (ie: 0.85V per battery), we by-pass LDOs and directly connect the battery reducing our cut-off battery voltage to 1.7V. This allows us to extract 76% of total charge vs. 46% of total charge if our cut-off were at 2.2V.

C. Power Management

LIT provides power solutions for the entire system on a single die with a single battery input. It does not require additional off chip components thereby reducing cost and area, fulfilling our design requirements.

In total, LIT has 4 LDOs with associated VREFs and IREFs (Fig. 6). The LDOs' modes are controlled by the Wakeup Interrupt Controller (Section D.) Active and Deep

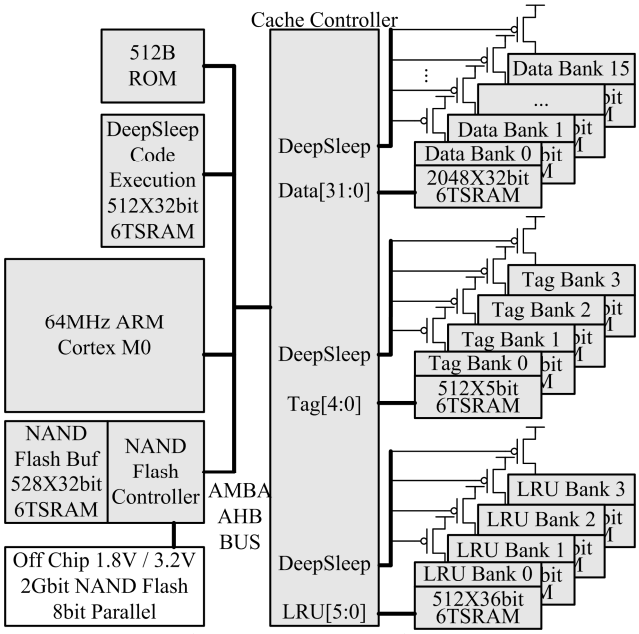


Fig. 3. Memory System Diagram

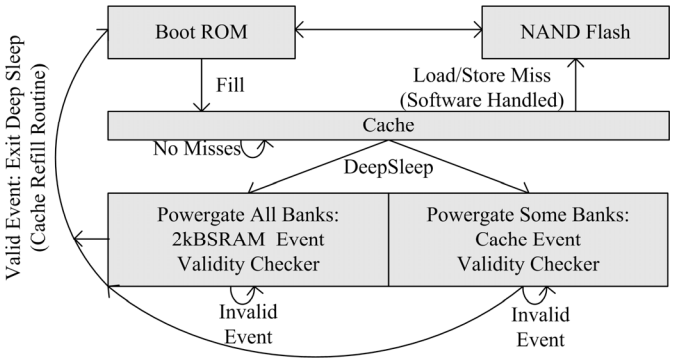
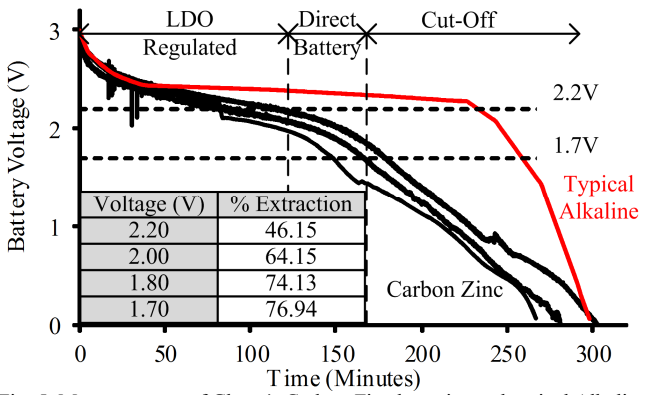
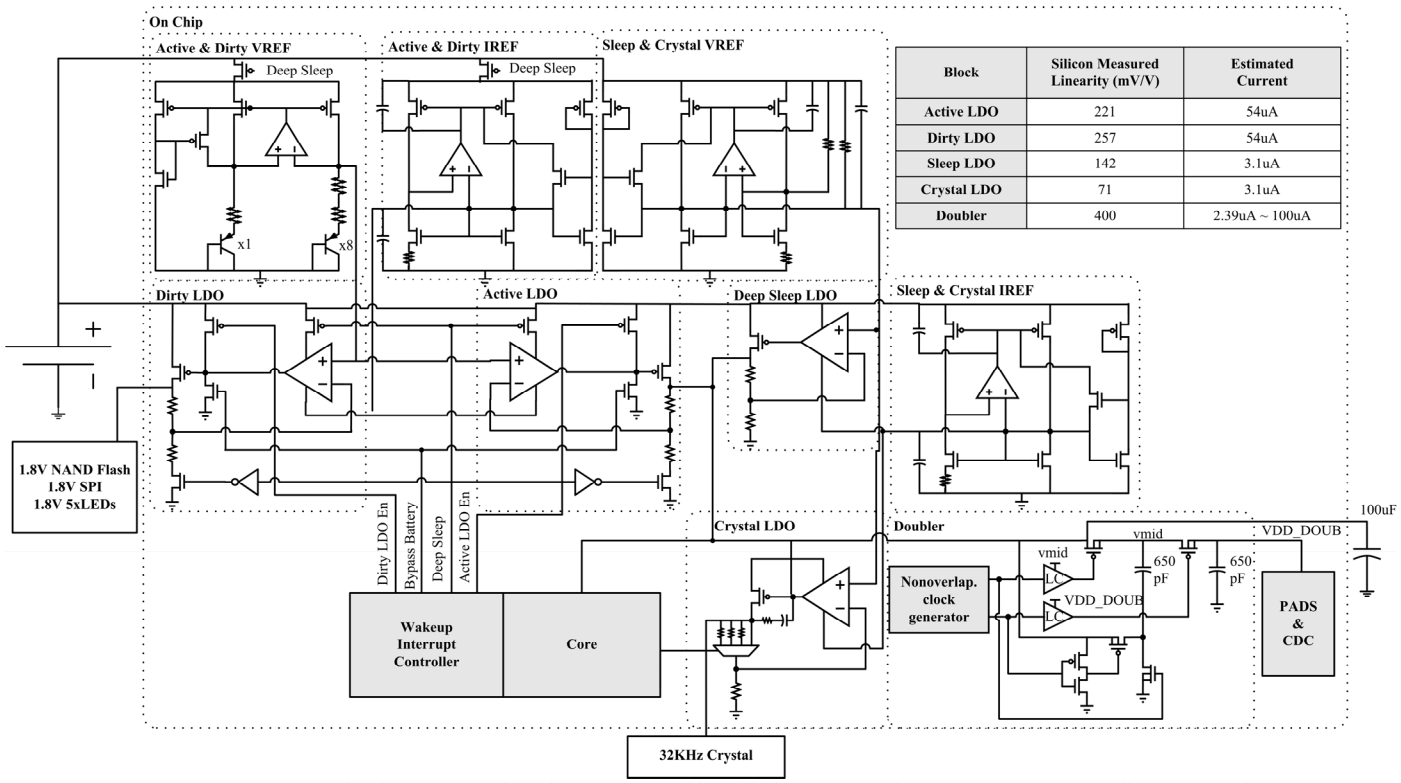


Fig. 4. Memory state diagram



Voltage (V)	% Extraction
2.20	46.15
2.00	64.15
1.80	74.13
1.70	76.94

Fig. 5. Measurements of Ghana's Carbon Zinc batteries and typical Alkaline battery. By extending operational voltage from 2.2V to 1.7V, 30% more energy is extracted.



Block	Silicon Measured Linearity (mV/V)	Estimated Current
Active LDO	221	54uA
Dirty LDO	257	54uA
Sleep LDO	142	3.1uA
Crystal LDO	71	3.1uA
Doubler	400	2.39uA ~ 100uA

Fig. 6. LIT's power diagram showing LDOs, and on chip voltage Doubler with their associated VREFs and IREFs and silicon measured output.

Sleep modes each have a dedicated LDO which coordinate power supply handoff upon mode switch. A 3rd Dirty LDO powers a 1.8V NAND Flash and also the on-chip Voltage Doubler that powers pads and CDCs at 3.2V. A 4th Crystal LDO, unaffected by battery bypass, constantly regulates the 0.95V supply that powers a 32KHz 830nW crystal that is used to tune the Radio Chip and keep real time allowing us to "Tivo" content from the Radio Chip. This allows content distributers to broadcast firmware updates through FM RDS and audio content through FM radio at predetermined times when the processor automatically wake itself up and records new content that can be listened to later by the user.

In traditional systems, when the battery voltage drops below the system's operating voltage, standard Power-On-Resets/Brown-Out-Detectors (POR/BOD) will assert reset. However, Carbon Zinc batteries have the characteristic that their voltage increases significantly after reset is asserted due to the lower current being drawn. The increased voltage will overcome the hysteresis in a typical POR/BOD circuit and cause reset to be de-asserted. This leads to an oscillation that will continuously turn the device on and off near the end life of the battery due to its strong self-healing properties. In order to circumvent this unwanted behavior, we designed a 1.7uA POR/BOD with a lock-off feature (Fig. 8). If the voltage drops below the BOD low-threshold (1.7V), the device locks itself off, until the voltage drops further below 1.2V, (e.g. when changing the batteries) resetting the lock. At this point, if the voltage goes past 1.7V, the device is turned on again.

Finally, LIT has a second voltage booster to power other chips, such as 3.2V NAND Flash and radio. To ensure an output voltage within the 3.2V spec over a wide range of battery voltages (3.2V – 1.7V) while avoiding the expense of inductors used in boost-converters, we created a new hybrid Switch Cap Network (SCN) topology. We combine a Step Down SCN which provides fractional supply voltages, with a Step Up SCN (Fig. 9). The fractional voltages of the Step Down SCN are 25%, 33%, 50%, 66%, 75%, 100% of battery voltage, while the Step Up SCN output voltage range is determined by Step Down SCN + 1V. This combination of fractional voltages from the Step Down SCN and Step Up SCN ensures that we can maintain a boosted voltage within 10% range of 3.2V. The Voltage Booster can also be bypassed to output the battery voltage and can be power gated when unused.

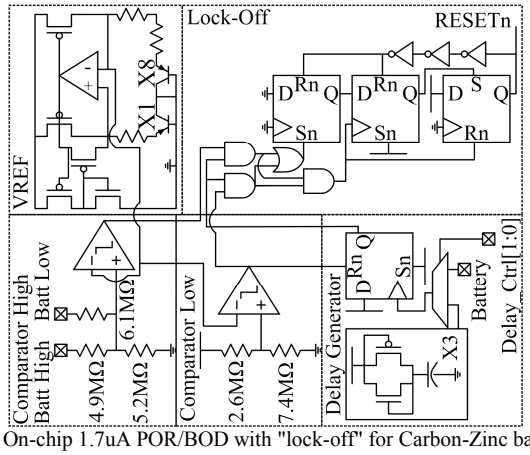


Fig. 7. On-chip 1.7uA POR/BOD with "lock-off" for Carbon-Zinc batteries

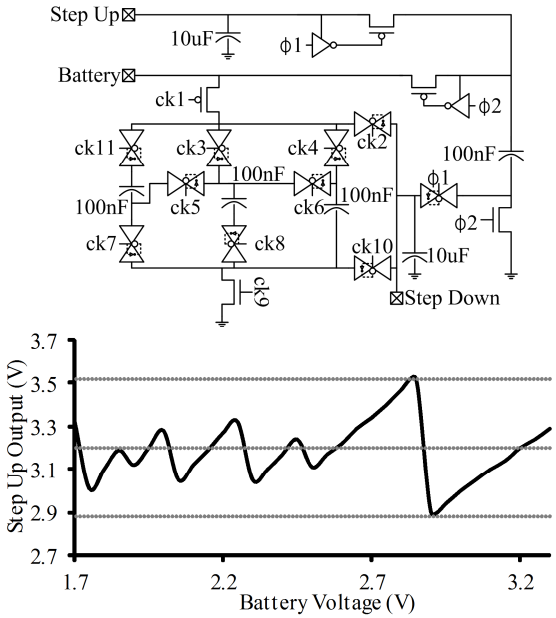


Fig. 8. Variable Step-Up Converter using set-down/-up SCNs. Measured Output is shown to stay within 10% of 3.2 across 3.3V - 1.7V battery voltage range.

D. Operational Mode Wakeup Interrupt Controller

LIT's Active, Standby and Deep Sleep operational modes are coordinated by the Wakeup Interrupt Controller (WIC) (Fig. 9). In Active Mode, blocks can be power gated depending on usage. Measured current is 17.4mA with only the Cortex M0 running at 4MHz and 50.8mA at 64MHz. In Standby Mode, the Cortex M0 is clock-gated and the main system clock is slowed until an event occurs, and draws a measured 15.3mA. In Deep Sleep Mode, clock generator is halted, the Active LDO, cache and unused blocks are power gated. The (WIC) which monitors the CDC controller, 32KHz Timer, or GPIO will wake up the Cortex M0 in an event and draws a measured 17uA (32KHz WakeTimer Monitoring) to 27uA (All Event Monitoring) that results in ~2 years of Deep Sleep lifetime.

We show LIT's design parameters and measured results (Table 1), Shmoo plot (Fig. 10) and die micrograph (Fig. 11).

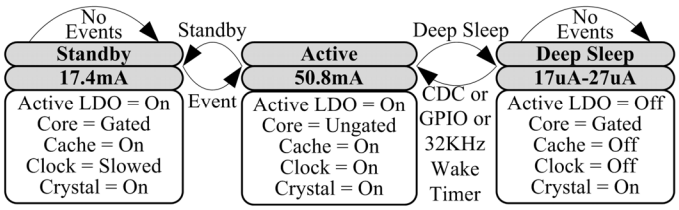


Fig. 9. Wakeup-Interrupt Controller State Diagram

III. Conclusion

The LIT chip provides low energy consumption and high power efficiency for Carbon Zinc batteries that are common in developing world areas. Use of a memory hierarchy and a high level of integration results in a low board-level component count that enables a low cost, affordable solution to disseminate information to illiterate populations.

Table 1. Design Parameters and Measured Results

Technology	180nm
Area	23.06mm^2
Performance	64MHz
# Transistors	8Million
# Gates	265K
Cache	128kB True LRU
Cache Area	46%
Electronics Cost	<$6
Chip Cost	<$1
ADC 8DC Input 4AC Input 1MIC Input	40Ksample/s 3mW 10bit 8.9ENOB
Touch Sensor CDCx10	3 sample/s 0.72mW 13ENOB
Near Field Inductive Coil	BER < 10^{-6} 660kbps at 6.5cm
Active Power	91mW
Standby Power	27mW
Deep Sleep Power	30.6uW
Operating Voltage Range	3.3V – 1.7V
Sleep Lifetime (Carbon Zinc)	~2 years

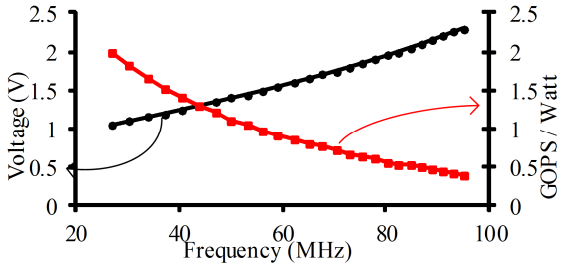


Fig. 10. Shmoo Plot: Measured Clock Frequency vs. Voltage

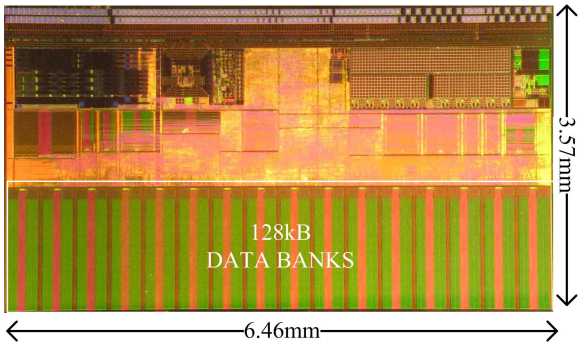


Fig. 11. Die Micrograph

References

[1] One Laptop Per Child, http://one.laptop.org
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