A 4.7nW 13.8ppm/°C Self-Biased Wakeup Timer Using a Switched-Resistor Scheme

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Miniaturized computing platforms typically operate under restricted battery capacity due to their size [1]. Due to low duty cycles in many sensing applications, sleep-mode power can dominate the total energy budget. Wakeup timers are a key always-on component in such sleep modes and must therefore be designed with aggressive power consumption targets (e.g., <10nW). Also, accurate timing generation is critical for peer-to-peer communication between sensor platforms [1]. Although a 32kHz crystal oscillator can provide low power [2] and accurate long-term stability, the requirement of an off-chip component complicates system integration for small wireless sensor nodes (WSNs).

As a result, conventional on-chip oscillators for WSN applications utilize RC time constants, which show relatively accurate frequency stability compared to transistor-delay-dominated ring oscillators. Conventional RC oscillators periodically reset a capacitor using an RC time constant and comparator [3,4]. However, a power-hungry fast continuous comparator is needed to render its delay negligible compared to the RC time constant and thus maintain accurate RC frequency stability. A timer using a frequency-locking technique to allow an ultra-low-power amplifier to replace the comparator is proposed in [5]. However, oscillation frequency cannot be scaled down due to the resistor size, which limits the minimum power consumption. For example, even with a relatively large 55MΩ resistor occupying 0.2mm² in 0.18μm CMOS, the topology consumes 18.2nW at 1V switching amplitude.

To address this challenge and achieve a WSN timer with single-digit nW power consumption, we propose a new timer using a duty-cycled resistor scheme to increase resistance without impacting area. By generating the duty cycle using the frequency from the timer itself, an accurate on/off ratio is ensured. In addition, the mismatch is more linear than that of the diode stack, thus it can be more easily tuned out by trimming TC of RSW. The switching voltages are level-converted through coupling capacitors and a pair of cross-coupled transistors so that the clock feedthrough of each switching transistor is balanced and driving capability is constant regardless of the output voltage [7].

Figure 5.8.2 shows the detailed circuit implementation. Amp1 and Amp2 regulate voltages on RSW and C1SW through MD1 and MD2, respectively. C2G and C1G are connected in parallel with RSW and C1SW to reduce the ripple arising from switching events. However, those capacitors can reduce the frequency of the second pole and make the regulation loops unstable. Furthermore, ultra-low-power design using sub-threshold-biased devices exacerbates sensitivity to PVT variations, complicating the design. This work proposes a self-biasing scheme that uses a replica of IREF to generate amplifier biasing currents. Assuming near 0dB gain of source follower MD, the regulation-loop phase margin is defined by tan⁻¹(gmC1/gmampC1D0) where gmC1 and gmampC1D0 are transconductances of M1 and Amp1’s differential pair, respectively. As the phase margin is determined only by the ratio of transconductance and capacitance, stability can be ensured across a wide range of PVT variation. Furthermore, self-biasing acts to maintain relatively constant power consumption of analog building blocks across temperature and removes the need to include an accurate current reference generator, thereby saving power and area.

Figure 5.8.3 shows transient signal behavior of the reference and control voltages. VDIV is frequency divided from VOUT and provides an accurate on/off ratio for the switching resistor. VSR and VSC are the voltages on RSW and CSW and are regulated by VN and VP, respectively, taken from the downconverter. Voltage ripple on VSR and VSC due to switching operation causes current ripple on IRS and ISC. The difference of IRS and ISC is integrated by C1 and creates a quadratic ripple on VSR. This ripple can perturb the duty cycle of VDIV, creating temperature-dependent offset. To mitigate these non-ideal effects, a sampler is placed in front of the VCO so that the control voltage is constant within a divider cycle. Amp3 drives sampling-transistor body voltages to remove the drain junction leakage from the sampled voltage, VSR.

A key part of the proposed low-power scheme is the switched resistor. Resistor current (IOUT = (VSR-VSC)/(M×RSW)) can be reduced by either lowering the voltage across the resistor or increasing RSW. The lower bound on voltage swing is determined by amplifier input offset. VSR is therefore selected to be 1/16th of the supply voltage in order to allow center-frequency adjustment after trimming RSW and C1SW under wide variation of amplifier offset and process. The practical upper bound of RSW is dictated by area requirements and set to 17MΩ, with resulting area of 0.065mm². The proposed resistor-switching scheme increases the resistor size without increasing area. A switched resistor is usually implemented by placing a switch in series with a resistor [6]. However, current can still flow from the non-disconnected port to parasitic capacitance in the resistor even when the switch is off. This reduces the equivalent resistance and makes it temperature dependent. This effect worsens quadratically with resistor size as the current injected into its parasitic capacitance grows linearly while the current flowing through the resistor reduces inversely with resistance. Instead, we connect both resistor terminals so that charges on the parasitic capacitors are only shared while the switch is off. This eliminates injection of additional current from the parasitic capacitor (Fig. 5.8.2, left).

Reference voltages VS and VR are generated using a series of switched-capacitor 2-to-1 downconverters clocked by the oscillator output. The stable oscillator frequency results in a constant current consumption across temperature (Fig. 5.8.4), especially compared to conventional diode stack-based voltage dividers as shown in Fig. 5.8.4, right. Even though the voltage mismatch between VS and VR is negligible compared to the overall temperature variation, the mismatch is more linear than that of the diode stack, thus it can be more easily tuned out by trimming TC of RSW. The switching voltages are level-converted through coupling capacitors and a pair of cross-coupled transistors so that the clock feedthrough of each switching transistor is balanced and driving capability is constant regardless of the output voltage [7].

The proposed design was fabricated in 0.18μm CMOS with an area of 0.5mm². It uses only a single supply voltage and does not require additional voltage or current references. Measured results in Fig. 5.8.5 show that the design generates 3kHz while consuming 4.7nW with a temperature coefficient of 13.8ppm/°C measured from −25 to 85°C. Power consumption varies by <50% across this wide temperature range due to the self-biasing technique. Measured line sensitivity is 0.48%/V from 0.85V to 1.4V and Allan deviation is less than 63ppm. Figure 5.8.6 provides a comparison table with other wakeup timers and Figure 5.8.7 shows a die micrograph.

References:


Figure 5.8.1: Block diagram of the conventional relaxation oscillator using a comparator and the proposed self-biased current-reusing frequency-locking scheme without using a current reference.

Figure 5.8.2: Circuit diagram of the proposed oscillator (top). At bottom left, the proposed approach of disconnecting both terminals of the resistor during off events enables wider temperature range operation (simulation results). At bottom right, the leakage-based delay cell used in the VCO.

Figure 5.8.3: Transient locking behavior of the output frequency, reference voltages and control voltages of the proposed oscillator (left) and their steady-state behavior (right).

Figure 5.8.4: Reference voltage generation using switched capacitor based DC-DC converter (left) and simulation results of power and accuracy compared to a diode stack (right).

Figure 5.8.5: Measurement results of wakeup timer temperature coefficient (top left), power consumption (top right), line sensitivity (bottom left), and Allan deviation (bottom right).

Figure 5.8.6: Performance summary and comparison to prior work in low-power wakeup timers.
Figure 5.8.7: Chip micrograph of the proposed wakeup timer in 0.18µm CMOS.