A Fully-Integrated 40-Phase Flying-Capacitance-Dithered Switched-Capacitor Voltage Regulator with 6mV Output Ripple

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Abstract

A switched-capacitor voltage regulator (SCVR) that dithers flying capacitance (C_{FLY}) to reduce output ripple is presented. The proposed technique is implemented in a 40-phase SCVR with 4b C_{FLY} modulation in 65nm CMOS. At 2.3V input, on-chip ripple magnitude of 6~16mV at 1V output is measured for 11~142mA load. Peak efficiency is 70.8% at a power density of 0.187W/mm^2.

Introduction

Integrated voltage regulation using on-chip DC-DC step-down converters can provide fast load response as well as reduced package current, which reduces IR and LdI/dt drops. Switched-capacitor voltage regulators (SCVRs) have gained popularity for on-chip regulation [1-5] as they are compatible with CMOS processes and do not require magnetic materials for inductors.

To stabilize the output voltage against fluctuating loads, prior SCVR designs employed closed-loop regulation techniques including single-boundary multi-phase control [1], multi-phase pulse frequency modulation (PFM) [2-3], or PFM combined with discrete-level capacitance modulation [4]. Even with multi-phase interleaving, SCVRs can exhibit >50mV output ripple [2], which incurs power overhead due to increased voltage margins. Partial charging using clock duty cycle [5] or switch conductance modulation [6] can reduce output ripple, but may be limited by challenges in precise timing control, variability tolerance, or intermediate voltage generation. Recently, an open-loop SC converter reported a small ripple of 3.8mV [7], but it requires external frequency modulation.

Proposed Technique

We propose dithered capacitance modulation (DCM) as a new scheme for output ripple minimization. Figs. 1 and 2 show conceptual timing diagrams of DCM and traditional PFM. The key ideas of DCM are to (1) modulate fine-grain flying capacitance (C_{FLY}) according to load current (I_L) rather than modulating phase or frequency, and (2) temporally distribute charge transfer as much as possible. In PFM, clock pulses are generated on demand with a fixed frequency clock and the full C_{FLY} is switched each time a clock pulse is generated. For instance, 1/3 of the maximum load current requires PFM to generate a clock pulse every third cycle (Fig. 1 at T1 and T4 across 6 clock cycles). However, this full C_{FLY} switching followed by no C_{FLY} switching yields high ripple. In contrast, DCM generates a clock pulse every cycle, but the transferred charge in a cycle is modulated by changing C_{FLY} on a cycle-by-cycle basis. To accomplish this, each SC converter phase is split into several parallel structures with binary-sized C_{FLY}. We use 4b modulation (CM[3:0]) to provide discrete C_{FLY} values. In the above example with 1/3 of the maximum load, DCM sets CM[3:0] = 5 at time T0, corresponding to 5/16 of maximum charge transfer in that cycle (Fig. 1). Since 5/16 < 1/3, the output voltage drops slightly and falls below the threshold voltage, triggering DCM to increase CM[3:0] to 6 (or 6/16 of maximum transfer) at T1, increasing the output voltage. Since the output now exceeds the threshold, DCM switches back to CM[3:0] = 5 for T2 and T3, creating a repeating pattern every three cycles with an average transfer of $1/3 \times 6/16 + 2/3 \times 5/16 = 1/3$ of the maximum. A 2-phase SC converter with 4b DCM is built as shown in Fig. 3.

The proposed DCM technique is implemented in a 40-phase SCVR with 4b C_{FLY} modulation. C_{FLY} uses MIM and MOS capacitors with a total value of 3.7nF. C_{FLY} is divided into 40 phases, each consisting of binary-weighted SC converters (C_{LSB} = 5.8pF). No explicit output capacitance is used. The number of phases and the modulation resolution present a trade-off between ripple and area overhead due to capacitor spacing requirements. The chosen configuration minimizes ripple while limiting area overhead to 10%.

The 40-phase DCM SCVR has four SC banks (Fig. 4). Each SC bank comprises five SC converters with 2-phase 4b DCM. A 760MHz master clock is divided to 190MHz and then split into twenty phases by a DLL with 263ps between phases. Each 190MHz clock drives a 2-phase SC converter, where two non-overlapping 95MHz clocks are locally generated. Three comparators (C0~C2) operate at the 760MHz master clock, generating a comparison output every ten SC phases. References $V_{th,p}$ and $V_{th,m}$ are used to adjust CM upon I_L changes, and V_{target} is used to regulate V_{out} in steady state. The steady-state example in Fig. 4 shows CM dithering between CM[3:0] = 3.6, when CMP = 1 (cycles 1-2), and CM[3:0] = 3.4, when CMP = 0 (cycles 3-5). This yields an average CM value of 3.48. Finally, a shunt push-pull regulator is used to mitigate undershoot/overshoot against transient I_L change.

Figs. 5-7 show the DCM controller flow chart and a stabilization example given an I_L transient. Five modulation signals CM0~CM4 are generated as a function of the base modulation level CM and the dithering value N_d (Fig. 6). Upon a large step change in I_L, if $V_{out} < V_{th,m}$, (Fig. 7) counter CNT_M is incremented and added to CM ($CM = CM + CNT_M$). This increases C_{FLY} geometrically for each subsequent cycle as long as $V_{out} < V_{th,m}$. After increasing CM, if $V_{out} > V_{th,p}$ the controller decrements the stored dithering level $N_{d,reg}$ by one in each cycle until $N_{d,reg}$ reaches one, at which point CM is decreased by one and $N_{d,reg}$ is reset to five. In steady-state, when V_{out} lies between $V_{th,p}$ and $V_{th,m}$, only N_d is adjusted.

Measurement Results

DCM is evaluated in a 65nm CMOS testchip that also includes a 40-phase PFM SCVR. Since package parasitics act to attenuate ripple, off-chip ripple measurement is difficult and tends to under-estimate ripple magnitude. Hence, an on-chip ripple measurement circuit [8] is incorporated, consisting of an asynchronously clocked comparator and two counters that record the fraction of cycles with $V_{out} < V_{RMC}$ (Fig. 8). Ripple is defined by the V_{RMC} voltage range with probability = 1% to 99%, while V_{RMC} with 50% probability is defined as the average V_{out}. Also, an on-chip digital-load performance monitor [9] is implemented to measure the impact of ripple on digital circuit delay (Fig. 9). Power and area overhead of DLL, controller, and comparators are 3.3mW and 1.3%, respectively.

Parameters V_{in}, V_{target}, $V_{th,m}$, and $V_{th,p}$ are set to 2.3V, 1V, 0.985V, and 1.015V, respectively. Using the on-chip ripple measuring circuit DCM achieves steady-state 6mV ripple at I_L = 11mA, compared to 145mV for PFM at the same I_L. A periodic load change between 11mA and 48mA (period ~2μs) results in 65mV undershoot and 105mV overshoot in DCM (Fig. 10). The smaller undershoot is a result of the more aggressive controller response to $V_{out} < V_{th,m}$.

Fig. 11 shows measured DCM and PFM ripple versus power density (I_L = 11-142mA). DCM ripple ranges from 6−16mV and scales with load current as expected according to the open-loop ripple expression ($I_L/(F_{SC} \times 40 \times C_{FLY})$). In addition, DCM V_{out} is tightly regulated to V_{target}=1V (Fig. 12). The load performance monitor was used to measure the impact of ripple on digital circuit frequency: the PFM-driven circuit shows 16% slower performance than DCM at large I_L (Fig. 12). DCM achieves peak efficiency of 70.8% at a power density of 0.187W/mm^2 (Fig. 13). Fig. 14 shows the die photo and Fig. 15 compares with prior work.

References

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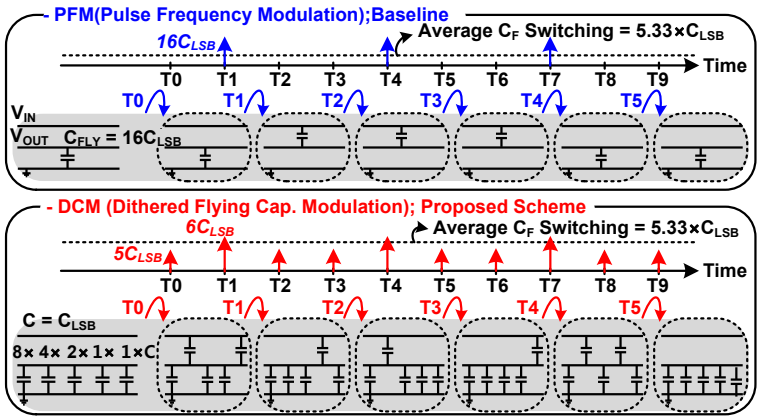


Fig. 1. Conceptual timing diagram of flying capacitance switching (When single-phase SC is assumed).

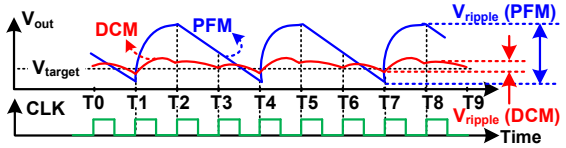


Fig. 2. Conceptual output voltage waveforms for DCM & PFM.

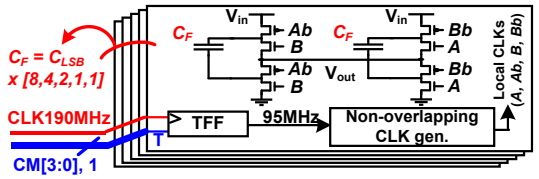


Fig. 3. Converter implementation for 2-phase SC for 4b DCM.

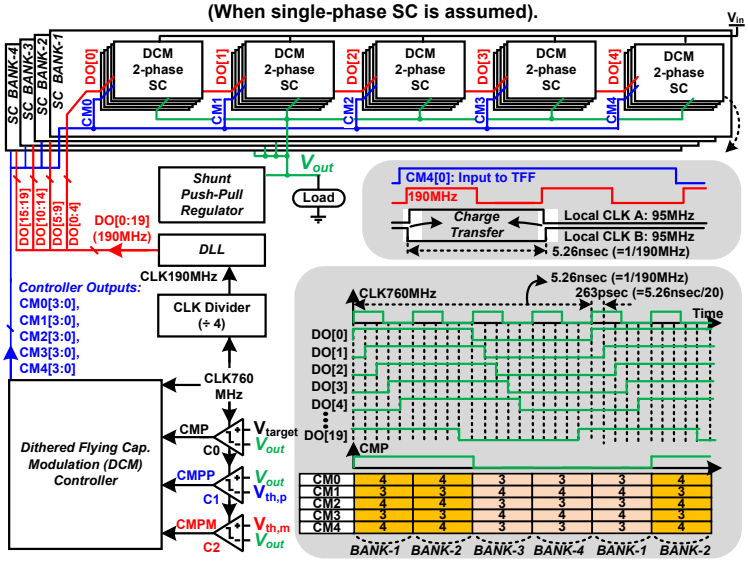


Fig. 4. Top-level diagram of closed-loop 4b DCM SCVR with 40-phases: The 40-phase DCM SCVR is composed of four SC-banks (top). Local clock generation example (right). Timing diagram for DCM operation in steady state (bottom right).

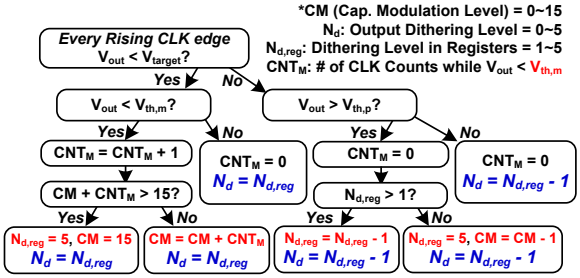


Fig. 5. Flow chart for controller operation.

	N_d					
	0	1	2	3	4	5
CM0	CM-1	CM-1	CM-1	CM	CM	CM
CM1	CM-1	CM-1	CM	CM-1	CM	CM
CM2	CM-1	CM	CM-1	CM	CM-1	CM
CM3	CM-1	CM-1	CM	CM-1	CM	CM
CM4	CM-1	CM-1	CM-1	CM	CM	CM

Fig. 6. Dithered capacitance modulation outputs (CM0~CM4) of controllers as function of CM and N_d.

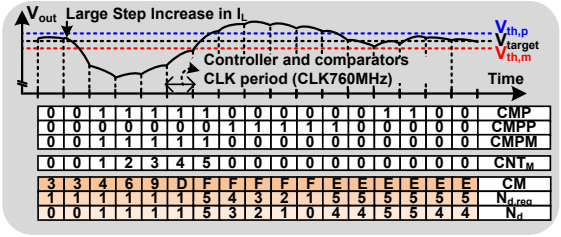
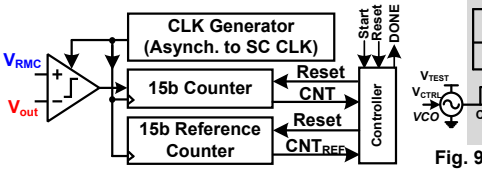


Fig. 7. DCM controller stabilization example upon load change.



(1) At each V_{RMC}, reset CNT and CNT_{REF} = 0 and start
(2) When DONE = 1, calculate probability = CNT/(2^{15}-1)
(3) Find V_{prob99} and V_{prob1}, and calculate V_{ripple} = V_{prob99} – V_{prob1}

Fig. 8. Ripple measuring circuit (Ref. [8]).

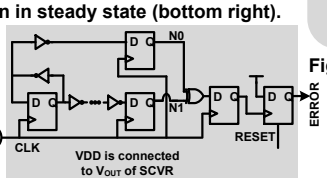
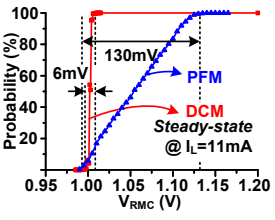


Fig. 9. On-chip digital-load performance monitor (Ref. [9])



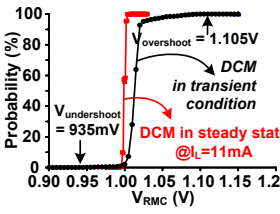


Fig. 10. Ripple measurement: DCM and PFM (top), and DCM in transient condition @ I_L=11mA ↔ 48mA (bot)

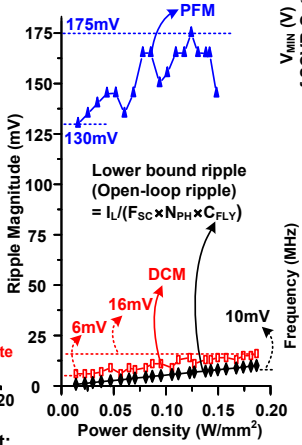


Fig. 11. Measured output ripple vs. power density.

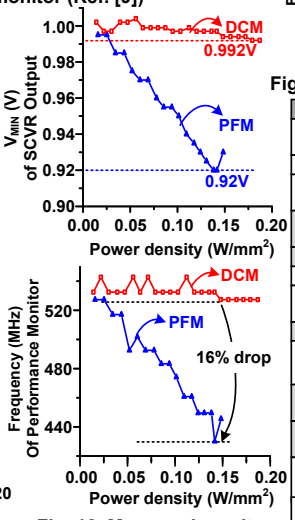


Fig. 12. Measured results: V_{MIN} of output voltage (top), and frequency of on-chip performance monitor (bot).

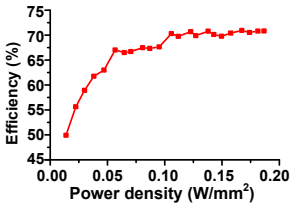


Fig. 13. Measured DCM efficiency.

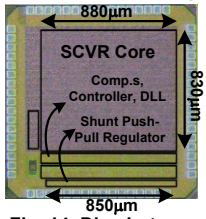


Fig. 14. Die photo.

Metric	[2]	[3]	[4]	This Work
Technology	22nm Tri-gate	32nm SOI	45nm Bulk	65nm Bulk
Capacitor Type	MIM	Deep Trench	MOS	MIM + MOS
Conversion Ratios (M)	2:1, 3:2, 5:4, 1:1	2:1, 3:2	3:2, 2:1	2:1
Closed-loop Modulation	Freq.	Freq.	Freq. (PFM), Capacitance	Capacitance Dithering
Comp. Freq.	2GHz	4GHz	30MHz	760MHz
SC Freq. (F_{SC})	≤ 250MHz	≤ 125MHz	≤ 30MHz	95MHz
Number of Phases (N_{PH})	8	16	2	40
C_{FLY} / C_{OUT} (nF)	[1]N/R / 0.1	16 / 0	0.534 / 0.7	3.7 / 0
V_{in} / V_{out}	1.23V / 0.45 ~ 1V	1.8V / 0.7 ~ 1.1V	1.8V / 0.8~1V	2.3V / 1V
Ripple Measurement	Off-chip	Off-chip	Off-chip	*On-chip*
$V_{ripple,pp}$	60mV @≤88mA	30mV @365mA	50mV @≤10mA	6~16mV @11~142mA
V_{droop}	<25mV @15→30mA	94mV @30→365mA	155mV @2→10mA	65mV @11→48mA
[2]Power Density (ρ, W/mm²)	0.064	2.71	0.050	0.187
Efficiency @ ρ	68%	86.4%	66%	70.8%

Fig. 15. Comparison table ([1]N/R = Not reported, [2]Power density = reported @ M = 2:1).