Wide Input Range 1.7µW 1.2kS/s Resistive Sensor Interface Circuit with 1 cycle/sample Logarithmic Sub-Ranging

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Abstract

A wide input range 1.7µW, 1.2kS/s resistive sensor interface circuit fabricated in 0.18µm CMOS is presented. This circuit consumes 6.6× lower power and 31.8× less energy than previous state-of-the-art work, considering the worst-case cycle count required for correct conversion. The proposed design uses a logarithmic subrange detector based on comparator metastability to convert an input resistance ranging from 10Ω to 10MΩ in 1 cycle/sample.

Introduction

Resistive sensing is widely used in chemical [1], gas [2], and pressure sensing [3], with applications in implantable and point-of-care diagnostics among others. Sensor interface circuits for these systems are challenging due to the wide input resistance (RIN) range (kΩ to MΩ) and µW power constraint to achieve long battery life. In a resistance-to-digital converter (RDC), RIN is first converted to a voltage VIN then measured by an ADC (Fig. 1). The resistance to voltage conversion is performed by connecting the input resistor to a fixed current source. However, accommodating a high RIN range results in one of two issues: the ADC input voltage will saturate at high RIN or an extremely high resolution ADC is required to sense low RIN that produce very small voltages. Hence, a common approach is to divide the RIN range into sub-ranges and apply different currents for each sub-range using a current DAC (I-DAC) [1,5,6]. This technique greatly increases accuracy across the total RIN range (Fig. 1).

A key challenge in sub-ranging RDCs is finding the correct sub-range. Typically, the RDC starts with an arbitrary sub-range, performs a complete conversion (including ADC step), and examines the resulting code. If this code is out of range, the sub-range is changed (+1 step) and the process repeats until the correct range is found [1,4]. This requires worst-case N iterations to obtain the correct code for 2N-1 sub-ranges, increasing energy and slowing the sampling rate.

To address this issue, we propose a new sub-ranging RDC that finds the correct sub-range within 1 sampling cycle using a novel logarithmic converter. We also note that the energy consumed by the I-DAC is a major portion of total energy consumption. This work minimizes I-DAC energy by dynamically adjusting its on-time according to the sub-range setting, whereas previous RDCs enable the I-DAC for the worst-case stabilization time. In addition, a switched capacitor (SC) amplifier is inserted prior to the ADC; it improves ADC resolution and reduces energy via shorter VIN settling time. The proposed design consumes 1.7µW. It reduces energy per conversion by 31.8× compared to current state-of-the-art RDCs [1,2,4] and achieves 1000× RIN range with 0.21% measurement error.

Logarithmic Sub-Range Detector

Fig. 2 shows the logarithmic sub-range detector. The full RIN range is divided into sub-ranges that increase in geometric fashion. Hence, the correct sub-range is found by taking the log of RIN. To implement this log function, we use the intrinsic behavior of a comparator operating near its metastable point. RIN is first converted to VIN by the I-DAC, sampled on C简单 and shifted up by VREF to position both V2 and VR at the metastable point. At this point, q2 switches are opened and a cross-coupled inverter pair starts to resolve V2 and VR. If V2 is large, V2 (V2) resolves to 1.2V (0V) quickly, while this resolution time increases exponentially as V2 becomes smaller. The subsequent inverter chains and XOR output 0 and stop the counter when VR becomes lower than VREF/2 (mathematical analysis in Fig. 2). The proposed log converter determines the correct sub-range in one comparison, enabling 1 cycle/sample operation. To remove the effect of charge injection, the voltage transfer circuit uses bottom-plate sampling and the SC structure uses stray-capacitance insensitive topology. Auto-zeroing is also adopted for offset cancellation, resulting in offset of σ=0.24mV (40× smaller than without auto-zeroing, simulation). Across process corners, comparator gain is one-point calibrated to maintain a consistent code range.

Resistance to Digital Conversion

After the correct sub-range is found for a particular RIN, the corresponding I-DAC current is selected and VIN is generated from the resulting IR drop (Fig. 3). VIN is transferred to VINout and VINout (with opposite sensitivities to VCM) via two SC amplifiers and then digitized by a 10-bit SAR ADC. The SC amplifiers are used for three reasons: 1) they perform pseudo-differential sampling to cancel out common-mode voltage; 2) they increase usable ADC output range by SC amplifier gain and thus enhance resolution by 1.98×; 3) they decouple the large capacitor DAC (C_DAC−, C_DAC+) from the RIN. If the large C_DAC is used as the sampling capacitor, the I-DAC must remain on for a longer time due to the large RC time constant. By scaling the smaller C_SIMPLE− (1pF) and charging C_DAC± (9.3pF) in a different phase, energy is reduced by 7.7× compared to an approach where C_DAC is used as the sampling capacitors.

Fig. 4 shows the flow chart of the RDC conversion process. First, a 300nA current (I_INIT) is applied to the unknown RIN and the resulting I_INIT×RIN is sampled. This I_INIT is chosen to map the entire RIN range (10kΩ – 10MΩ) to the log converter’s operating range. The log converter then produces a counter value that is compared to 4 threshold values to determine 4 coarse sub-ranges. According to the coarse subrange, a second current (6.4mA, 1.6mA, 0.4mA, or 0.1mA) is activated on the I-DAC resulting in an I_COARSE×RIN spanning 50–800mV in each coarse subrange. The same procedure repeats to divide each coarse subrange into 5 fine sub-ranges, yielding 14 possible sub-ranges. Sub-ranges overlap to guarantee correct conversion for the entire RIN range. Each of the 14 fine sub-ranges specifies an I-DAC setting that ensures INL×RIN lies in the SC amplifier operating range. This voltage is then pseudo-differentially sampled and converted into a digital code by the 10b SAR ADC. Also, each fine sub-range specifies a sampling time, minimizing I-DAC activation time and reducing worst-case power consumption by 21%. Finally, recall that in the proposed RDC, sub-range determination is performed every conversion cycle, in contrast to traditional RDCs that can require multiple cycles to determine the correct sub-range.

Measurement Results

Fig. 5 shows measured log converter counter values at different VIN. Because the converter is based on metastability, it is susceptible to noise and hence ±16 curves are shown. Each sub-range overlaps with its adjacent sub-ranges to provide error tolerance and ensure the probability of a sub-ranging failure (i.e., RIN falls outside a correct sub-range) to be < 3.2× probability for sub-range 1 and < 5× probability for sub-ranges 2 – 4. The worst-case measurement error is 0.21%. Off-chip 0.01% precision resistors are used to measure accuracy and the resistor bottom node voltage is swept with a sourcemeter to obtain additional equivalent resistances. The error pattern reveals repeated error behavior in each sub-range. A 10b ADC with SC amplifier shows DNL of +0.37/+0.56LSB and INL of +0.93/-1.48LSB. The SC amplifier slightly degrades INL but improves resolution by 1.98×, resulting in better accuracy overall. At the minimum input resistance, the circuit consumes its maximum 1.7µW at a sampling rate of 1.2kS/s. Power consumption is 6.6× smaller than the state-of-the-art work in [4]. Table 1 compares the RDC with prior work showing large resistive range and similar conversion rate while worst-case energy/conversion is reduced by ~31.8×. A resistive Cds light sensor was successfully measured with the RDC (Fig. 6). Total design area is 1.5×0.82mm² in 0.18µm CMOS (Fig. 7).

References

Fig. 1. An overview of N cycles/sample conventional RDC and a proposed 1 cycle/sample RDC with logarithmic sub-range detector.

Fig. 2. A logarithmic voltage-to-time converter based on comparator metastability resolution time, and its transient voltage behavior and sub-ranging code output vs. $V_{IN}$.

Fig. 3. (a) A switched capacitor amplifier that pseudo-differentially samples input and (b) improvement of ADC resolution by SC amplifier gain.

Fig. 4. Conversion process flow chart of 1 sample. $R_N$ is logarithmically compressed, sub-ranged, and then converted by 10b ADC.

Fig. 5. Measured results of a sub-ranging, DNL & INL of 10b ADC with SC amplifier, and measurement error for input resistance range.

Fig. 6. Conversion result measured with off-the-shelf CdS light sensor.

Fig. 7. Microphotograph (1.5 × 0.82mm$^2$).

### TABLE I. Performance summary and comparison.

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<td>Required device number (cycle worst cases)</td>
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<td>N/A</td>
<td>5</td>
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<td>0.5</td>
<td>3.3</td>
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<td>60k – 10M</td>
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<td>10k – 2G</td>
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<td>200</td>
<td>180</td>
<td>700</td>
<td>200000</td>
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<td>N/A</td>
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<td>MSS. Error (%)</td>
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<td>&lt; 0.32</td>
<td>N/A</td>
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<td>&lt; 0.14</td>
<td>&lt; 2.7</td>
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<tr>
<td>Power (µW)</td>
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<td>N/A</td>
<td>87.4</td>
<td>&gt; 60</td>
<td>N/A</td>
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* Assumes worst case cycle count and maximum input resistance.
* Coarse ADC power is not reported, thus extra energy needed for finding sub-range is not included.