

Racetrack Converter: A Low Power and Compact Data Converter Using Racetrack Spintronic Devices

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Abstract— Current-induced domain wall motion in racetrack memory promises energy-efficient analog computation using compact magnetic nanowires. This paper explores the feasibility of data converters based on current-induced domain wall motion and introduces an n-bit ADC using n racetrack magnetic nanowires. With each magnetic nanowire having a different configuration granularity, an n-bit binary or gray code is generated simultaneously. The proposed ADC structure achieves 21fJ/conversion-step at 20MHz with area under $10\mu\text{m}^2$. The racetrack ADC is suitable for applications requiring dense ADC arrays, such as image sensors. This paper describes one ultra-high speed DPS imaging system benefiting from the racetrack ADC.

Keywords— Racetrack, Domain Wall, ADC, image sensor

I. INTRODUCTION

Low-power and compact analog-to-digital converters (ADC) are an essential part of ultra-high-speed image sensors, in which each photodiode includes a moderate-accuracy ADC for parallel data conversion [1]. CMOS implementations of such data converters face two challenges: large area and high static power. As a result, most high-speed image sensors only use column parallel ADCs in their sensor array to balance area/power and performance [2-3].

Recently, current-induced domain wall (DW) motion has driven the invention of spintronic devices that hold promise for non-volatility, high density, and low power [4]. With perpendicular magnetic anisotropy (PMA) structures, hundreds of magnetic domains separated by DWs can be maintained in one nanowire for multi-bit non-volatile memory [5-7].

This paper presents a novel spintronic-based ADC that leverages the non-volatility, low power, and high density of spintronic devices. We propose an n-bit racetrack ADC using n magnetic nanowires with different configuration granularity for each bit. The current-induced DW motion can convert n bits binary or gray code in parallel. Since most components are spintronic devices, the design achieves compact area, scalability and low power. Compared to a conventional low power CMOS SAR ADC, the proposed racetrack ADC achieves $1000\times$ smaller area with comparable energy efficiency figure-of-merit (FOM). We also describe the potential application of the racetrack ADC to a high-speed imaging system using the 8b racetrack ADC as in-pixel ADC. Results indicate that frame rate can be increased by $50\times$ compared to a CMOS digital pixel sensor (DPS) while retaining high fill factors as in analog pixel sensors (APS).

II. CURRENT-INDUCED DOMAIN WALL MOTION

The racetrack memory device is a magnetic nanowire comprising multiple magnet domains separated by DWs [5-6]. A single data bit is stored as the local spin polarity within the DW magnet strip at a given position. DWs can be shifted along the magnetic strip by induced horizontal charge current.

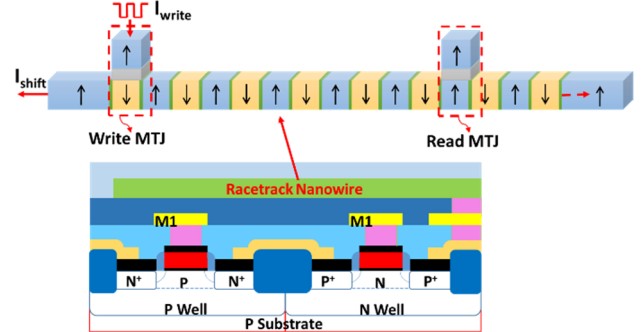


Fig. 1. Structure of a racetrack memory device consisting of a magnetic nanowire and two MTJ heads as the read and write ports. The racetrack nanowire is manufactured on top of MOS, avoiding planar area overhead.

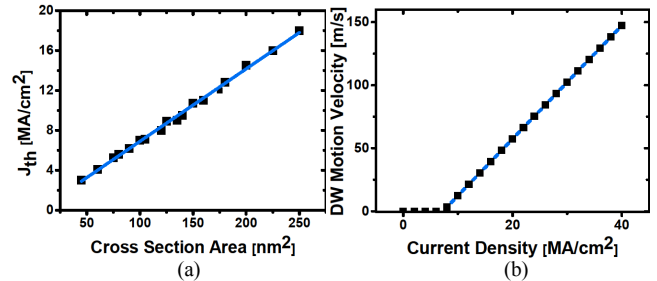


Fig. 2. (a) Threshold current density decreases with reduced cross-sectional area of magnetic nanowire [8]; (b) Once current density exceeds the threshold, DW motion velocity linearly increases with higher current density [7].

According to the adiabatic spin transfer torque model, threshold current density decreases with reduced width and thickness [8]. As shown in Fig. 2(a), when the cross-sectional area of magnetic nanowire is very small (width $< 50\text{nm}$, thickness $< 5\text{nm}$), the threshold current density is linearly proportional to cross-sectional area. When driving current exceeds the threshold current, the DW moves along the nanowire at a speed linear to the driving current. DW velocity can be described as:

$$v = \frac{\beta\mu P}{\alpha e M_s} (J - J_{th}) \quad (1)$$

where β is the non-adiabatic coefficient, μ is the Bohr magneton, P is spin polarization percentage of the tunnel current, α is the damping constant, e is the elementary charge, M_s is the demagnetization field, J is current density, and J_{th} is threshold current density [7]. Given this linear characteristic as shown in Fig. 2(b), current-induced DW motion is suitable for analog computation and data conversion in particular.

III. PROPOSED RACETRACK CONVERTER

A. Overview of Racetrack Converter Operation

1) *Configuration*: Fig. 3 shows the structure of the proposed racetrack converter with 3 bits as an example. An n-bit converter requires n nanowires. Each nanowire will have 2^n DWs, n read MTJs and n write MTJs. Each nanowire

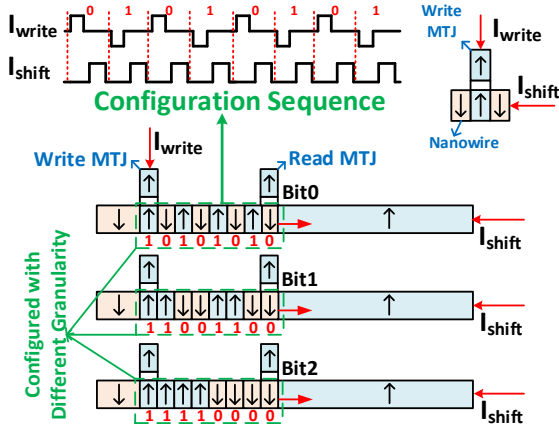


Fig. 3. Structure of a 3b racetrack converter. Each nanowire is configured with different DW granularity and represents an individual bit.

will be configured differently such that each generates a single bit, from LSB to MSB. Then, the polarization of magnetic domain beneath n read MTJs represents the digitalized value from 0 to 2^n-1 . This configuration is done only once post-fabrication, using the write MTJ port. When applying a positive current pulse on the write MTJ, the magnetic domain beneath that MTJ becomes spin-polarized with downward direction representing data 0; a negative current pulse generates upward spin-polarized magnetic domain (data 1). With a sequence of alternating write and shift current pulses, corresponding data can be stored on nanowires one by one. Altogether, such a design can store 256×8 bits on 8 magnetic nanowires to form an 8-bit racetrack data converter.

2) *Reset*: After configuration, the write MTJ will subsequently perform reset point detection. Before conversion, a reset operation is required. Horizontal reset current flows through the nanowire to cause DW motion. When all DWs move back to their original position, write MTJ resistances undergo their resistance transitions, which is detected by sense amplifiers. Once the resistance change is sensed, the shift current is cut-off, signifying the completion of the reset phase.

3) *Data Conversion*: After reset, data conversion begins (Fig. 4). The input current under measurement flows through the nanowire in the opposite direction of the reset current. In this case, all DWs move right simultaneously. As the current under measurement for each nanowire has the same value, the DWs in different nanowires move at the same velocity. After a fixed time T , the DWs will stop. The distance X that DWs move can be expressed as:

$$X = v * T = \frac{\beta \mu P}{aeM_s} \left(\frac{I}{Area} - J_{th} \right) * T \quad (2)$$

The distance X is linearly proportional to the current I or the time T , which makes racetrack nanowires promising for both current-digital and time-digital converters.

4) *Read*: The polarization of the magnetic domain beneath the read MTJs stores the digitized value of the distance a DW has moved (ranging from 0 to 2^n-1). As the read MTJ head is upward spin-polarized, MTJ resistance with a downward spin-polarized nanowire domain could be $2-3 \times$ higher than that with upward polarized nanowire domain. Therefore, by sensing resistance of the whole read MTJ, a 0 or 1 state can be defined. Using sense amplifiers, the data can be read out as a digital value.

B. Racetrack ADC

The proposed racetrack converter is fully compatible with other current-mode spintronic logic devices. However, most CMOS modules remain voltage-based. The interface circuits with CMOS (Fig. 5) require a voltage-current (V-I) converter to provide current at the input of the converter and sense amplifiers to detect current at its output.

Fig. 6(a) shows a 4T all-PMOS V-I converter with the racetrack nanowire as the load. T0, T1, and T2 in the first stage make up an attenuator (amplifier with gain < 1). The output voltage of attenuator V_0 linearly follows the change of the input voltage V_{in} in opposite direction. The range of V_0 is smaller than V_{in} , forcing T3 to operate in the velocity saturation region. As the electrical characteristics of a racetrack nanowire mimic a resistor, the current through the nanowire also changes linearly with input voltage. We can design this lowest current to compensate the threshold current of DW motion. As shown in Fig. 6(b) the transconductance of this 4T V-I converter is linear, with an adjusted R-Square value of 0.9997. Furthermore, this V-I converter is built using all PMOS, which increases its tolerance to process corners. In addition, VSSH can be raised to achieve lower power without affecting the current of source follower T3.

The racetrack nanowire itself is a non-volatile memory. With traditional CMOS sense amplifiers (Fig. 7(c)), stored data can be accessed. An error in reading will occur when a DW moves to the midpoint beneath the read MTJ and the resistance is in the middle. The error becomes significant if most bits are at their flipping point as in Fig. 7(a). To avoid multi-bit flipping, we choose a gray code rather than a binary code to ensure only one bit changes at a time. We also exploit the self-reference sensing scheme to narrow the meta-stability region. As shown in Fig. 7(b), an additional reference MTJ is placed next to the read MTJ. It serves as a reference with opposite phase to the read MTJ. If the read MTJ resistance is high, that of the reference MTJ is low. As illustrated in Fig. 7(d), this technique shortens the meta-stability window of the sense amplifier by 50%. Neither Gray coding nor self-sensing induce area or delay overheads.

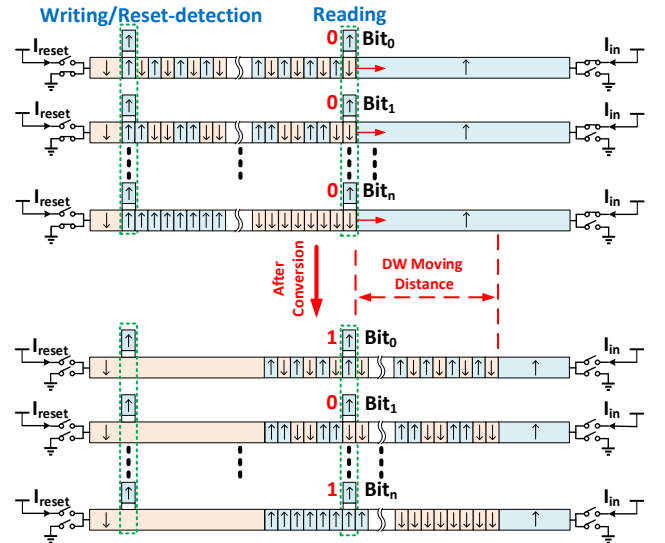


Fig. 4. Data conversion scheme for an n -bit racetrack converter. During conversion, DWs move simultaneously and stop at a distance that is proportional to either input current or pulse duration.

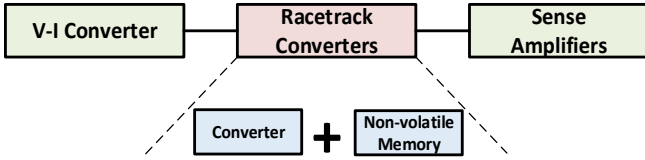


Fig. 5. Racetrack converters function similarly to a combination of data converter and non-volatile memory. Interface circuits to CMOS must provide current to the converter and sense the current at its output.

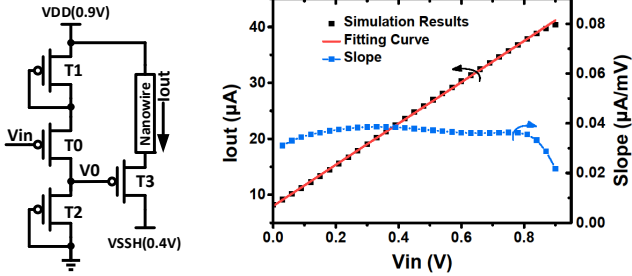


Fig. 6. Schematic of 4T all-PMOS V-I converter and simulation results of its Iout-Vin characteristics.

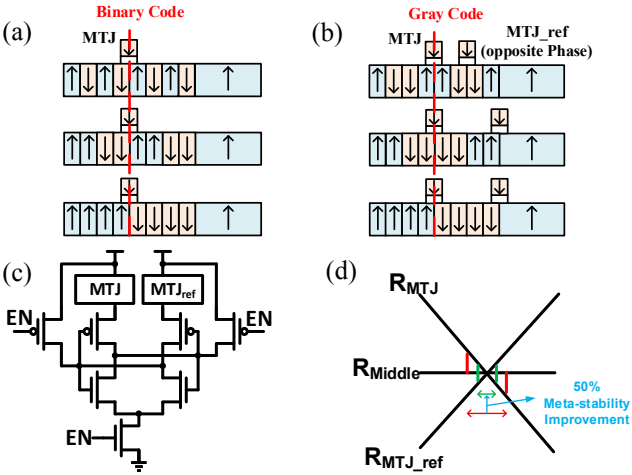


Fig. 7. (a) Midpoint meta-stability problem; (b) Solution with Gray Coding and Self-reference Sensing; (c) Sense amplifier; (d) Sensing dead zone can be narrowed by 2× using self-reference sensing.

IV. SIMULATION RESULTS AND ANALYSIS

A) Simulation Results

We build compact Verilog-A models of MTJ and racetrack nanowire based on published experimental data [4-8]. The dimensions of each nanowire are designed to be $3.5\text{nm} \times 30\text{nm} \times 16\mu\text{m}$, compatible with a 32nm technology. Co-simulation with CMOS circuits (a commercial 32nm SOI technology) is performed by SPICE simulator.

Fig. 9(a) shows data conversion of an 8b racetrack ADC. The ADC input voltage range is $[0, 0.9\text{V}]$ with 3.52mV LSB. Fig. 8 shows the power and area breakdown of each component. Among the three parts, the racetrack nanowires dominate power consumption, taking more than half of the total power. As racetrack nanowires can be placed on the top of the MOS, they do not induce extra area overhead. Another advantage of the proposed racetrack ADC is that total area and power scale linearly with resolution rather than exponentially as in CMOS ADCs (Fig. 9(c)). Adding one bit requires only one additional magnetic nanowire, an added second stage of V-I converter (first stage is shared), and one sense amplifier. Racetrack ADCs also benefit from the significant scalability of spintronic devices. With technology scaling, the total nanowire length can be shortened, which will lower the required velocity to achieve same sample rate. As DW motion

is based on current density, smaller cross-sectional area translates to smaller current to achieve same velocity. Therefore, average power at constant sample rate reduces cubically with scaling (Fig. 9(d)).

Table I shows the characteristics of a racetrack ADC in 32nm technology. At 20MHz, the racetrack ADC consumes $96\mu\text{W}$ with only $10\mu\text{m}^2$ in area, which is 3 orders of magnitude smaller than state-of-the-art CMOS low power SAR ADCs with comparable FOMs (~ 20 fJ/conversion-step). The average power increases with higher sample rate of the ADC (Fig. 9(b)). We designed it with a modest operating frequency of 20MHz to ensure DW velocity linearity and reliability. With a wider linear region of DW velocity, higher sampling rates can be achieved.

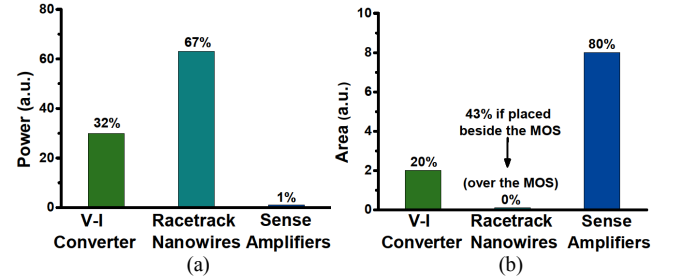


Fig. 8. Power (a) and area (b) breakdown of each ADC component. Racetrack nanowires consume the most power though area overhead can be ameliorated by placement above MOSFETs.

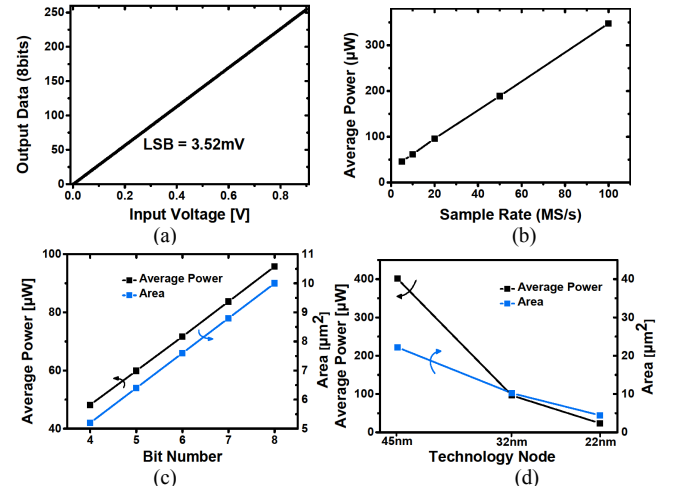


Fig. 9. (a) Simulated data conversion of ADC; (b) Average power increases with higher sample rate; (c) Total area and power increase linearly with more bits; (d) Average power reduces cubically with technology scaling.

TABLE I. Comparison to 8b CMOS ADCs with comparable sampling rates

	CMOS ADC [9]	CMOS ADC [10]	This work
Technology (nm)	90	40	32
Sample Rate (MHz)	10	20	20
Resolution (b)	8	8	8
Power (μW)	26.3	84.9	96.5
FOM (fJ/conv.)	12	19.2	21
Area (mm^2)	0.021	0.0153	0.00001

B) Analysis

1) *Process Variation*: For the racetrack nanowire, the major sources of variation include: 1) MTJ layer area; 2) tunneling oxide thickness; 3) cross-sectional area of the nanowire. Both 1) and 2) affect MTJ resistance [11] and may lead to read failure. The proposed self-reference sensing helps

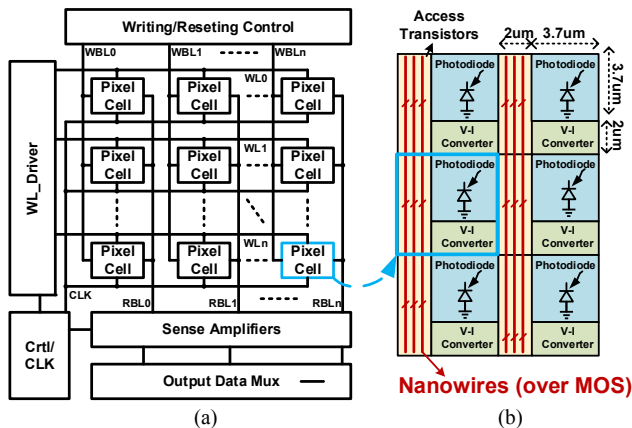


Fig. 10. (a) DPS block diagram with racetrack ADC. (b) Layout of 2×3 pixels. Racetrack nanowires can be placed on top of the access transistors.

TABLE II. Comparison between CMOS APS/ DPS and Racetrack DPS

	CMOS APS [2]	CMOS DPS [1]	Racetrack DPS
Sensor Fill Factor	40%	15%	42%
Frame Rate	3 500	10 000	>500 000
ADC Resolution (b)	12	8	8
ADC Conv. Time (ns)	500	25	50
Energy/frame (μ J)	280	5	0.04

alleviate this influence. LER induced nanowire cross-sectional area variation can affect the threshold current density for DWs to move and shift the v - J_{th} curve of DWs. Fortunately, similar to threshold voltage mismatch in CMOS devices, the threshold current mismatch arising from cross-sectional area random variation can be alleviated by variation-aware circuit design techniques (current offset compensation methods) or post-silicon calibration techniques. This paper focuses on the concept of a racetrack nanowire based converter, however advanced design techniques used in CMOS converters, such as pipelining and time-interleaving, can also be applied to improve its accuracy or performance. Moreover, thanks to the compact area, an additional bit can be included to compensate for potential accuracy losses arising from variation with only 12.5% area and power overhead for 8-bit ADC, as an example.

2) *Noise*: The proposed racetrack converter works in current mode during data conversion, which suffers less from noise compared to voltage operation in CMOS ADCs [12]. Moreover, during conversion a constant current flows through the nanowires, with no switching related noise. Only the V-I converter and racetrack nanowires will contribute thermal noise. Spintronic devices generate 3 times less thermal noise than MOS transistors because of their smaller resistance [13].

V. HIGH-SPEED IMAGE SENSOR WITH RACETRACK ADCS

High speed imaging systems employing in-pixel ADC, also known as digital pixel sensor (DPS), have several advantages over widely-used conventional analog pixel sensor (APS) architecture with column-wise ADC, including much higher speed, better scalability, and less noise (read-related column fixed-pattern noise and column readout noise). However, the major bottleneck limiting the application of CMOS DPS is the large pixel size and low fill factor due to the area overhead of in-pixel ADC and memory. [1] reported a high-speed DPS with per-pixel single-slope moderate-accuracy ADC and 8b 3T DRAM. The dynamic range and

frame rate are greatly enhanced but area and fill factor are unreasonably high [2-3].

The proposed racetrack ADC is a combination of ADC and non-volatile memory with extremely compact area, making it well suited for the DPS image. Fig. 10 shows the DPS structure with the proposed racetrack ADC in each pixel. Both the V-I converter and access transistors can be implemented with only PMOS devices, further minimizing the required area as large N-P well spacing is avoided. The racetrack nanowires can be placed on top of PMOS transistors with no area overhead. Fig. 10(b) illustrates a layout of 2×3 pixels. The nanowire is rectangular, hence 1×3 pixels can be arranged together to match nanowire length. 3×8 nanowires are placed above the access PMOS. In this arrangement, area is dictated by transistors rather than the nanowires so that the fill factor is significantly improved over CMOS only DPS pixels.

Table II compares CMOS APS and DPS image sensors with Racetrack DPS image sensor. Sensor fill factor matches CMOS APS and is $3 \times$ better than CMOS DPS. Frame rate is improved by $50 \times$ with lower power consumption. The proposed racetrack ADC is promising for this high-speed imaging application.

VI. CONCLUSIONS

We analyze the potential of current-induced domain wall motion for data converter application and present an ADC design scheme based on racetrack magnetic nanowires. The 8-bit ADC can achieve $1000 \times$ smaller area than state-of-the-art CMOS ADC with similar energy efficiency. The results indicate that racetrack converters hold promise for future low-power small-area applications requiring multiple ADCs. We propose a high-speed racetrack ADC based DPS image sensor system to show the potential of this technology.

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