A 5.8nW, 45ppm/°C On-Chip CMOS Wake-up Timer Using a Constant Charge Subtraction Scheme

Seokhyeon Jeong, Inhee Lee, David Blaauw, Dennis Sylvester
University of Michigan, Ann Arbor, MI
seojeong@umich.edu, inhee@umich.edu, blaauw@umich.edu, dmcs@umich.edu

Abstract— This work presents an ultra-low power oscillator designed for wake-up timers in compact wireless sensors. A constant charge subtraction scheme removes continuous comparator delay from the oscillation period, which is the source of temperature dependence in conventional RC relaxation oscillators. This relaxes comparator design constraints, enabling low power operation. In 0.18µm CMOS, the oscillator consumes 5.8nW at room temperature with temperature stability of 45ppm/°C (-10°C to 90°C) and 1%V line sensitivity.

I. Introduction

Power consumption is a critical factor in the design of battery-powered compact wireless systems with volumes of 1cm^3 or less. These systems often exhibit low duty cycles, making standby mode power a key concern. Wakeup timers are one of the few components that must remain on during standby mode. Hence, it is vital to reduce their power consumption while also maintaining accuracy to ensure proper time keeping.

Crystal oscillators are the conventional choice for wake-up timers due to their excellent temperature and frequency stability. However, they require an external component, driving up system volume. Alternatively, a number of relaxation oscillators were recently proposed that can be integrated entirely on-chip. The basic operation of these relaxation oscillators is shown in Fig. 1. A current source (I_{REF}) charges a capacitor (C_{INT}) that is then repeatedly reset when a continuous comparator triggers, thereby generating an output frequency. Even if the charging time ($C_{INT}V_{INT}/I_{REF}$) is perfectly temperature compensated, these methods have the key drawback that temperature dependent comparator and buffer delays (t_d) impact the clock period. A simple way to address this issue is to improve the comparator and clock buffer bandwidth so their delays are negligible relative to the overall period. However, this incurs high power consumption.

In previous works, temperature dependency of charging time has been reduced through a chopper thereby eliminating comparator offset [1],[2]. On the other hand, a feedforward period control technique [3] was proposed to remove comparator and buffer delays. An inverter-based oscillator uses a zero temperature coefficient resistor and tracks threshold voltage variation to maintain both charging time and delay constant [4]. While these approaches achieve high accuracy (38.2 to 104ppm/°C in the kHz range), they consume 120nW to 4.5µW, which remains high relative to standby power in compact wireless sensors. Instead, comparator and buffer delays can be made negligible by slowing the clock frequency to the Hz range, using small gate leakage for I_{REF} [5],[6]. These oscillators consume sub-nW but are highly temperature sensitive (≥375ppm/°C) and offer poor supply stability (>40%/V), which is a critical drawback in battery-powered systems with often poor voltage regulation.

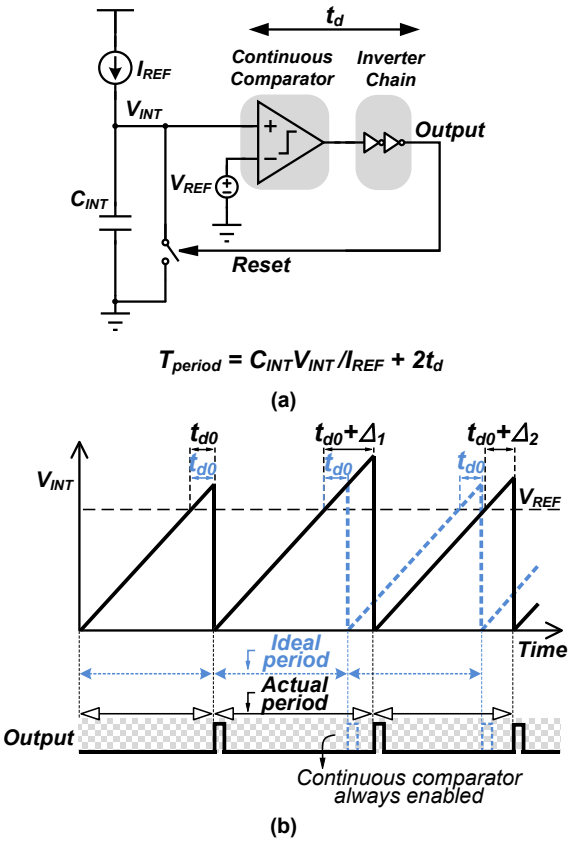

Fig. 1. (a) Basic structure and (b) concept of a conventional relaxation oscillator.

To avoid the fundamental trade-off between temperature-dependent comparator delay and comparator power, we introduce a novel constant charge subtraction scheme that eliminates comparator delay from the clock period.

II. Proposed Low Power Topology

A. Overview of Approach

Fig. 2 shows block diagram of the proposed oscillator and its concept of operation. Instead of the conventional approach of fully discharging the integrating capacitor (C_{INT}), a constant amount of charge (CV_{REF}) is subtracted from C_{INT}

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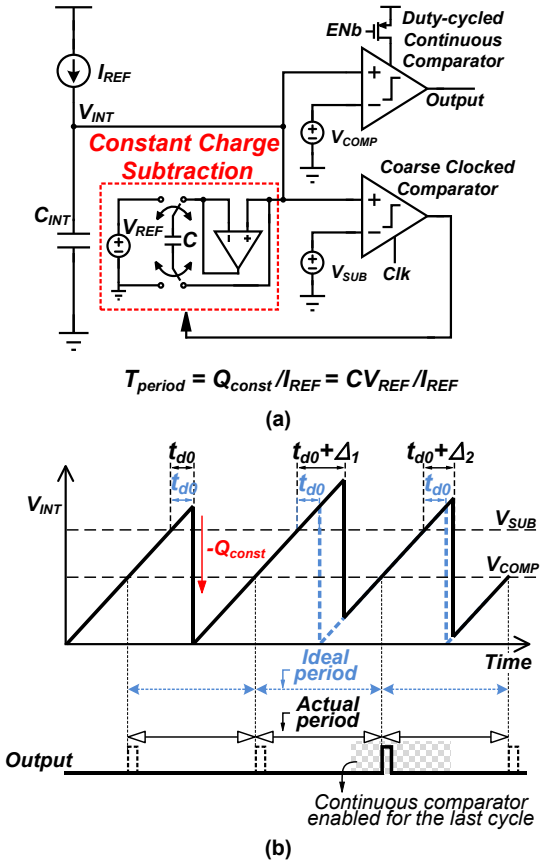

Fig. 2. (a) Basic structure and (b) concept of low power operation using a constant charge subtraction scheme.

through an amplifier. The power-hungry continuous comparator is replaced with a coarse, asynchronously clocked comparator to detect the subtraction point (V_{SUB}). The method leverages the key observation that while the actual subtraction time point varies ($t_{d0}+\Delta_i$), constant charge subtraction creates a sawtooth waveform that always rejoins the ideal sawtooth waveform. Therefore, the exact subtraction time does not impact the sawtooth waveform period and hence the clocked comparator can be slow and inaccurate, allowing its power to be reduced to ~100 pW. While the approach requires an additional amplifier for charge subtraction, its bandwidth can be relaxed to match the frequency of the oscillator and consumes only 2.1nA of tail current. A counter tracks the number of subtraction cycles and triggers an accurate continuous comparator for the last cycle only in order to generate a precise wake-up signal. With this scheme, an accurate wake-up signal is generated while the oscillator operates at ultra-low power for all but the final clock period.

B. Circuit Description

Fig. 3 describes operation of the constant charge subtraction method. Following an initial reset, the scheme cycles through two main phases; charge (Φ_1) and subtraction (Φ_2). In Φ_1, the subtraction capacitor (C_{SUB}) is connected to a voltage reference (V_{REF}) through the charging amplifier. A temperature-independent voltage source [7] charges C_{SUB} to a

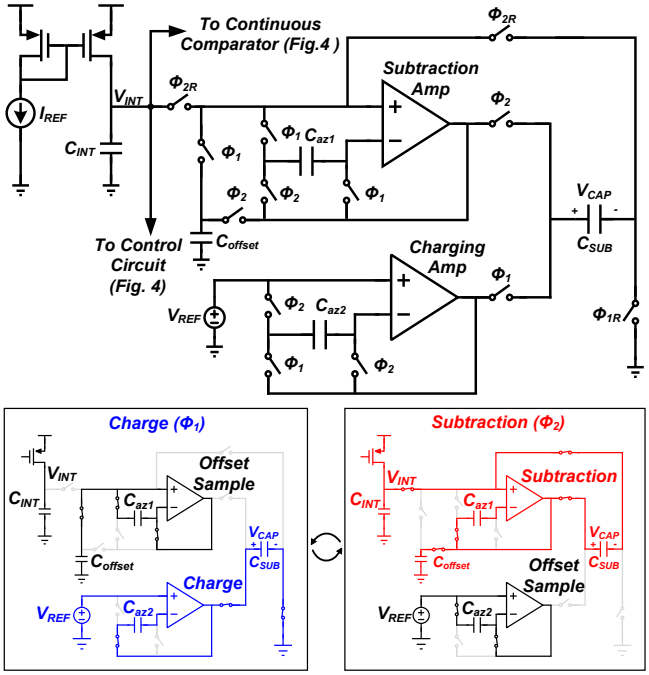

Fig. 3. Detailed structure of proposed constant charge subtraction scheme.

fixed voltage. At the same time, subtraction amplifier offset is stored on C_{az1} to remove offset and $1/f$ noise of the amplifier. The integration capacitor (C_{INT}) is disconnected from the subtraction amplifier to reduce the number of connected off-state switches, reducing leakage by 2.2× and improving timer error by 14ppm/°C in simulation. A temperature-compensated current (I_{REF}) charges up C_{INT} and when V_{INT} exceeds the subtraction voltage (V_{SUB}), the next phase (Φ_2) is triggered. During Φ_2, C_{SUB} is disconnected from the charging amplifier and connected to C_{INT} through the subtraction amplifier. The amplifier therefore subtracts charge in C_{SUB} from C_{INT}. Simultaneously, the offset voltage of the charging amplifier is stored on C_{az2} for the next phase. When V_{INT} reaches the reset voltage (V_{RST}) after subtraction, the phase reverts to Φ_1. Since temperature dependency of amplifier gain can lead to error in the period, both amplifiers are designed for open-loop gain of >78dB with bandwidth of 20kHz in the targeted temperature range, resulting in period error <1ppm/°C. It is important to note that the subtraction delay does not affect the overall period since I_{REF} continues to accumulate charge on C_{INT} during subtraction.

The 4T voltage reference [7] and diode stack generate two reference voltages, V_{SUB} and V_{RST}, for the clocked comparators (Fig. 4, left). The comparator clock is generated with a thyristor-based oscillator in a similar fashion to [8]. Due to high temperature sensitivity of this oscillator its frequency must be set at the lowest operating temperature. To avoid unnecessary power consumption, especially at high temperature, the oscillator is biased with I_{REF} to tolerate temperature dependence. The oscillator consumes 300pW and operates at 700Hz (25°C). While its leakage-based operation makes the comparator clock sensitive to temperature and supply voltage, the overall timer period is not impacted due to

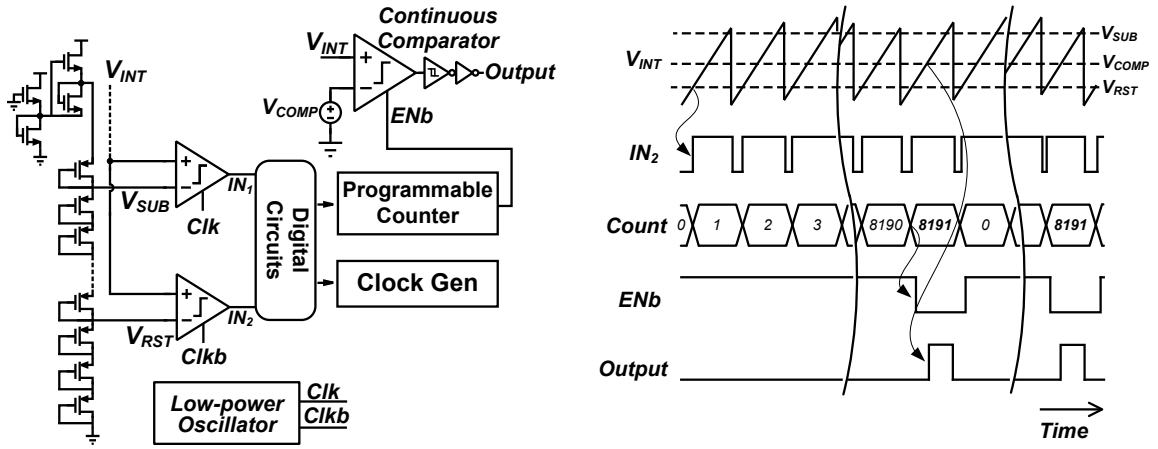

Fig. 4. Detailed schematic of control circuit for generating wake-up signal and clocks (left). . The comparator is activated just before wakeup and disabled after subtraction to prevent output glitching. The timing diagram shows generation of a wake-up signal (ENb) with 13-bit counter configuration (right).

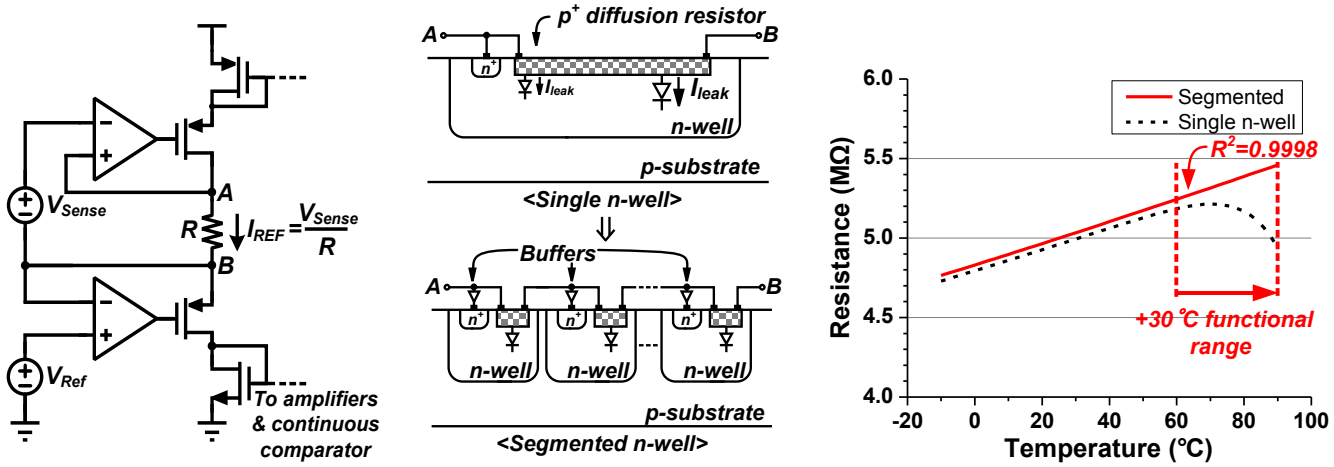

Fig. 5. A reference current (I_{REF}) generator (left) uses a segmented diffusion resistor to generate reference current. Segmenting the resistor incurs 10% area overhead compared to a single n-well resistor, but the reduced junction leakage increases the functional temperature range (right).

the constant charge subtraction scheme. A 2-stage op-amp serves as an accurate continuous comparator for generating a wake-up signal in the last cycle. With 25nA current consumption (5× current of complete oscillator in all previous cycles), comparator delay is <0.1% of the period in the targeted temperature range. Fig. 4 provides a timing diagram of operation. Power gating is controlled by a 16-bit programmable counter to activate the comparator only in the last cycle before wakeup.

The reference current I_{REF} is generated with a temperature-to-voltage sensing element (V_{Sense}) along with a voltage to current (V-I) converter and a resistor [9]. The sensing element is sized to compensate the temperature sensitivity of the resistor and outputs only 10mV, enabling ultra-low power operation. The resistor is a 5MΩ p+ diffusion resistor. In low current applications, junction leakage in the resistor degrades linearity at high temperature. As only 2nA flows through the resistor nominally, the 10× increase in junction leakage from 25°C to 90°C (to 212pA) causes a non-negligible change in total resistor current. We therefore segment the resistor into separate n-wells that are tied to intermediate points to minimize their voltage differences (Fig. 5, middle). Furthermore, segmented n-wells are biased through buffers to isolate n-well to p-substrate leakage. Buffers are designed for 1mV offset (10k Monte Carlo simulations), limiting frequency error below 0.02%. Through this technique the functional temperature range increases from 0-60°C to 0-90°C at a 6.1% area penalty and 500pW additional power from the well biasing buffers.

III. Measurement Results

The proposed wake-up timer is implemented in 0.18µm CMOS. Fig. 6 shows measured stability results against temperature and supply voltage. Operating at 11Hz, temperature stability is measured as 45ppm/°C from -10 to 90°C (±0.25%). Supply sensitivity is 1%/V from 1.2V to 2.2V. Measured Allan deviation demonstrates long-term stability (Fig. 7). As averaging time increases, frequency fluctuations decrease as white noise is averaged out until flicker noise dominates and timer performance saturates (~10mins).

Average power consumption of the timer decreases rapidly as the wakeup interval increases, reaching within 1% of 5.8nW after 50sec. Fig. 8 gives a breakdown of power consumption across the measured temperature range (1.2V supply, 12 min wake-up signals). Due to the proposed approach, continuous comparator power is a negligible portion of total average power consumption (<1%). Amplifiers and continuous comparator show only a small increase in power

with temperature due to current reference (I_{REF}) biasing. Table I compares state-of-art low- power on-chip oscillators, confirming that the proposed timer offers very low power operation with good temperature and voltage insensitivity. Chip photo is shown in Fig. 9.

IV. Conclusion

This work describes a novel wake-up timer that can be used in compact wireless sensors. A constant charge subtraction scheme is introduced to replace a power hungry continuous comparator with low-power clocked comparators. As a result, low-power time tracking is enabled and a precise wake-up signal is generated by triggering the accurate continuous comparator only for the last cycle.

References

[1] A. Paidimarri, *et al.,* "A 120nW 18.5kHz RC Oscillator with Comparator Offset Cancellation for ±0.25% Temperature Stability," *ISSCC Dig. Tech. Papers*, pp. 184-185, Feb. 2013.

[2] K.-J. Hsiao, "A 32.4ppm/°C 3.2-1.6V Self-chopped Relaxation Oscillator with Adaptvie Supply Generation," *Symp. VLSI Circuits,* pp. 14-15, June. 2012.

[3] T. Tokairin, *et al.,* "A 280nW, 100kHz, 1-Cycle Start-up Time, On-chip CMOS Relaxation Oscillator Employing a Feedforward Period Control Scheme," *Symp. VLSI Circuits*, pp. 16-17, June. 2012.

[4] D. Griffith, P. T. Roine, J. Murdock, and R. Smith, "A 190nW 33kHz RC oscillator with ±0.21% Temperature Stability and 4ppm Long-Term Stability," *ISSCC Dig. Tech. Papers*, pp. 300-301, Feb. 2014.

[5] Y. Lee, *et al.,* "A 660pW Multi-Stage Temperature-Compensated Timer for Ultra-Low-Power Wireless Sensor Node Synchronization," *J. Solid-State Circuits*, vol. 48, no. 10, pp. 2511-2521, Oct. 2013.

[6] Y.-S. Lin, D. Sylvester, and D. Blaauw, "A 150pW Program-and-Hold Timer for Ultra-Low-Power Sensor Platforms," *ISSCC Dig. Tech. Papers*, pp. 326-327, Feb. 2009.

[7] M. Seok, G. Kim, D. Blaauw, and D. Sylvester., "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," *J. Solid-State Circuits*, vol. 47, no. 10, pp. 2534-2545, Oct. 2012.

[8] M. Wieckowski, *et al.,* "A Hybrid DC-DC Converter for Sub-Microwatt Sub-1V Implantable Applications," *Symp. VLSI Circuits,* pp. 166-167, June. 2009.

[9] S. Jeong, J.-Y. Sim, D. Blaauw, and D. Sylvester, "A 65nW Temperature Sensor for Ultra-Low Power Microsystems," *Proc. CICC*, Sep. 2013.

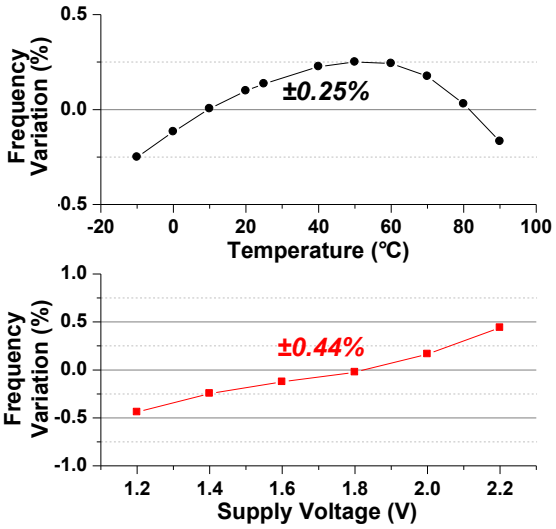

Fig. 6. Measured frequency stability against temperature and supply voltage.

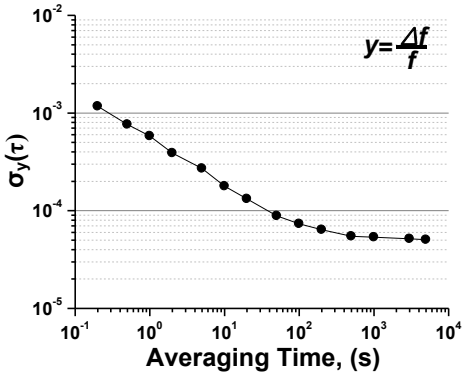

Fig. 7. Measured Allan deviation.

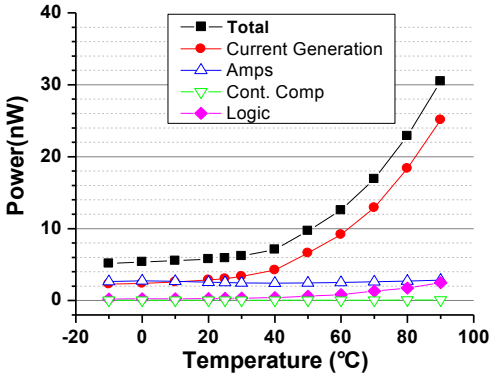

Fig. 8. Power breakdown of the timer.

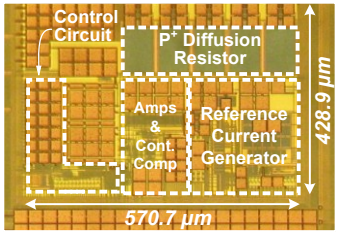

Fig. 9. Die photo of the timer in 0.18µm CMOS.

Table I. Comparison with previous work

Parameters	This Work	[5]	[6]	[1]	[4]
Process	**0.18µm**	0.13µm	0.13µm	65nm	65nm
Area (mm^2)	**0.24**	0.015	0.02	0.032	0.015
Frequency (Hz)	**11**	0.37	11	18500	33000
Temperature Range (°C)	**-10 to 90**	-20 to 60	0 to 90	-40 to 90	-20 to 90
Temperature Coefficient (ppm/°C)	**45**	375[1] (31[2])	490	38.5	38.2
Line Sensitivity (%/V)	**1**	490	40	1	0.09
Power (nW)	**5.8**	0.66[1] (N/A[2])	0.15	120	190

1. Without a temperature sensor.
2. With 10 point calibration using a temperature sensor. Power number with the sensor not available.