A 1.6nJ/bit, 19.9µA Peak Current Fully Integrated 2.5mm² Inductive Transceiver for Volume-Constrained Microsystems

Mohammad Hassan Ghaed, Skylar Skrzyniarz, David Blaauw, Dennis Sylvester
University of Michigan, Ann Arbor, MI 48109

Abstract — A 1.6nJ/bit inductive transceiver targeting volume-constrained microsystems with limited peak current is presented. The transceiver uses a protocol in which the external unit sends the same packet multiple times to shift the power consumption burden to the external TRX unit and relax jitter requirements on the mm-scale receiver. The transceiver receives data from a 2W external unit at 1m distance using a dual-coil LNA design and fast-startup frontend. The 2.5mm² transceiver draws 19.9µA from a 2mm² thin-film battery at 40.7kbps.

I. INTRODUCTION

Short communication range wireless sensor nodes are in great demand for biomedical [1,2] and other emerging applications. A differentiating feature of such nodes is their highly miniaturized form factor [3], often in the mm range. As a result, the substantial work in low power RFID is incompatible with this new class of devices due to the large antennas of RFID card-type devices [4]. Present near-field solutions require large peak currents that are infeasible in such systems [5]. Very small (1-10mm²) thin-film batteries offer the only reliable power source for such systems (Fig. 1). While their 10-50mJ capacities are sufficient for the transmission of several Mb of data between battery recharges (at ~1nJ/bit), their peak output current of 10-50µA is a key challenge for RF blocks (mA range). Therefore, these blocks must operate using a capacitive charge reservoir (nF range) that is recharged between radio transmissions. However, ms-scale recharge times reduce bit rate and place tight requirements on timing reference jitter in order to maintain synchronization throughout the longer communication process. This in turn increases timing reference power (typically integrated on-chip in such systems), which can come to dominate overall power consumption. Further, receiver start-up time/energy becomes critical given the limited charge reservoir.

To address these issues we propose a 2.5mm² near-field transceiver with integrated coils that uses a novel analog front-end and transmission protocol to relax synchronization requirements on the heavily constrained receive side. It uses a 14.3nF charge reservoir and draws 19.9µA peak current. The front-end uses a new fast-startup scheme to minimize start-up overhead and a new dual-coil LNA structure to maximize inductive coupling. The transceiver consumes 42.7nA during the heavily duty cycled monitoring mode and 19.9µA at 40.7kbps during active mode. Energy is drawn from a custom 2mm² 3.6V thin-film battery that is suitable for 3D stacking with the radio die.

II. TRANSCEIVER DESIGN

The proposed CMOS transceiver consists of an asynchronous controller, a receiver front-end and decoder, and an inductive transmitter (Fig. 1). To address the peak output current limitations of highly integrated microsystems, the transceiver uses a new half-duplex protocol that does not require accurate timing to receive data from an external unit (Fig. 2). To initiate data transfer, the external unit sends out a beacon for ~100ms, after which it ceases transmitting and listens for acknowledgement (Fig. 2). The receiver responds (after a delay Twakeup) by sending an acknowledgement via its on-chip transmitter. Next, the external unit begins data transmission by continuously sending a payload packet (header + data) (Fig. 2). After recharging its charge reservoir, the receiver wakes up briefly to capture data. Since the wakeup window will be arbitrarily aligned to the continuously transmitted Manchester-encoded

![Diagram of the proposed transceiver](image-url)
data, the decoder must locate the header to correctly rotate the captured window.

By transmitting the same data many times from the external side, uncertainty in the capture window location becomes acceptable (Fig. 2). This greatly relaxes constraints on clock jitter in the chip at the cost of increased power consumption in the external unit (which is typically not constrained). After receiving a packet, the receiver requests the next packet by sending a signal after a digitally tunable delay, $T_{\text{ack}}$, allowing time for the charge reservoir to recharge. If interference or noise cause the received bitstream to differ from the expected pattern, an acknowledgement is sent with a delay of $2T_{\text{ack}}$, signaling the external unit to retry the same packet. Data reception continues until the on-chip FIFO is full.

Protocol timing is managed by the asynchronous controller (Fig. 1), which is implemented using custom low-leakage high-Vth standard cells to limit total monitoring mode current to 42.7nA.

Fig. 3 shows the receiver front-end block diagram. A fully differential implementation maximizes immunity to interference and supply variation. It consists of a cascode LNA using a 2-coil configuration, two amplifiers, a bandpass filter, two envelope detectors, and a clocked comparator preceded by a source follower. The dummy envelope detector experiences the same interference, supply, and process variation as the main envelope detector, thus improving power-supply rejection and variation immunity. The 10µA source follower attenuates clock kick-back from the comparator to the high-Z envelope detector output by 21dB. When the front-end turns on (power gating released), startup switches short both plates of AC coupling capacitors to their steady-state values during the period shown in Fig. 3 (“Boost Coupling Caps” high). After this, the “Bias Startup” signal

Figure 2. The new transceiver protocol shifts link power and complexity to the external side, which has much less stringent energy constraints.

Figure 3. RF front-end block diagram.
kick-starts the bias circuitry to prevent unnecessary power consumption when front-end voltages stabilize. Finally, all common-mode feedbacks (CMFB) are boosted by injecting additional current into the error amplifiers until floating nodes approach their final values. Since transistors are not yet biased when CMFB boosting is asserted, instabilities caused by extra loop gain in CMFB are avoided. Using these techniques, receiver front-end start up time is reduced from 179µs to 0.45µs, rendering start-up energy less than 3% of total energy consumption for each received packet.

Unlike conventional antenna-driven LNAs, the inductive receiver uses an on-chip coil to couple to the external unit. Introducing a resistive input impedance by inductive degeneration would reduce the quality factor of our critical receive coil, degrading receive distance by 20%. To maximize mutual coupling between the on-chip coil and the external unit, the inductor magnetic moment must be increased. Two options are to increase area and/or the number of turns, however, the correspondingly lower self-resonance-frequency (SRF) would cause the larger inductor to operate as a capacitor at the frequency of interest. Based on 3D EM simulations, 4-turn inductors are the largest possible that still enable 915MHz operation. Therefore we introduce a second 4-turn coil (Fig. 4). This coil couples to the external coil in the same way as the main coil and is connected to the LNA cascode inputs (ke,main and ke,aux in Fig. 4). When the auxiliary coil resonates, this approach provides extra feedback to the input by coupling to the main coil via k_i (≈ 0.6), enabling a 3.6dB frequency-selective gain improvement, which translates to 22% added range (Fig. 4).
transceiver is the first fully integrated radio to achieve 1m range while operating from a battery of mm-scale.

REFERENCES


