Circuits for Ultra-Low Power Millimeter-Scale Sensor Nodes

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***Abstract*—Bell's Law predicts continual scaling of the size of computing systems, and next of these systems is about to emerge: millimeter-scale sensor nodes. These miniature wireless sensors will enable multiple new applications in a wide range of fields, including medical diagnosis, infrastructure monitoring and military surveillance. However, this form factor remains beyond the capabilities of modern integrated circuit design techniques due to extremely small battery size. This paper describes new circuit design techniques for ultra-low power operations that can be applied to digital processors, memory, power management, and a special focus on standby mode operation, which will bring mm^3 sensor nodes into reality.**

I. Introduction

Continuous technology scaling has led to the integration of growing computational capabilities in smaller volumes. As a result, diverse ranges of computing platforms have been developed, ranging from portable handheld devices to building-scale data centers. According to the Bell's Law, approximately every decade, a new class of smaller computers is developed by using fewer components or fractional parts of state-of-the-art chips [1]. Along with the emergence of personal computers in the 1980s and portable handheld devices in the 1990s and 2000s, wireless sensor networks have been recently developed. Considering the trend that the size of these computers is reduced by 2 orders of magnitude every decade, the next new class of miniature computing is poised to emerge: millimeter-scale wireless sensor nodes (Figure 1).

Today's wireless sensors already have a vast range of applications that commonly benefit from longer lifetimes, smaller physical sizes, and cheaper costs [2][3]. However, the state-of-the-art wireless sensors are typically built on printed circuit boards (PCB) with several individually packaged components, resulting in milliwatt-powered systems. Therefore they require bulky batteries to power the system for adequate lifetimes, requiring sensor systems that are centimeters or tens of centimeters per side. Recent advancements in ultra-low power (ULP) circuit design are realizing dramatic reductions in size and cost of future wireless sensors, while maintaining desired lifetimes.

The volume of these ULP sensor nodes, as recently demonstrated in [4], can be as small as cubic-millimeter or smaller. Therefore, a thin-film lithium battery would be used to power the sensor, whose energy density is only 1.5μAh/mm^2. Assuming daily full battery recharge, this allows only a 240nW power budget for the sensor. Unfortunately, simple circuit blocks such as a band-gap reference generator or an oscillator alone can far exceed this power budget. Moreover, the sensor requires measurement data process, retention and transmission which require much more complex circuit blocks such as a microprocessor, memory and radio.

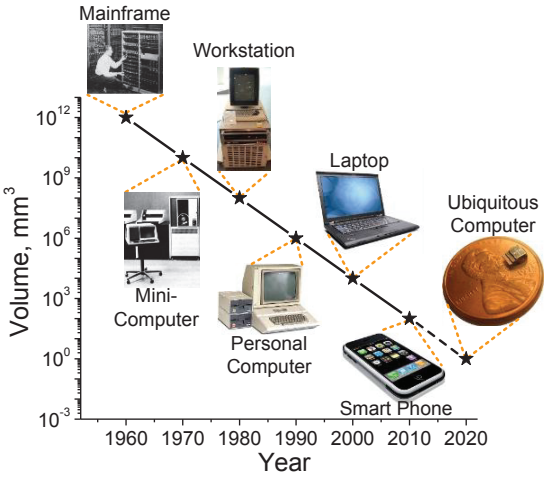


Figure 1. Bell's Law predicts continuous scaling of minimal-sized computing systems.

To meet the stringent power requirements of wireless sensors with these blocks, significant strides have been made in each of wireless sensor components to achieve robust ultra-low power operation. In this paper, recent research findings for a new class of ultra-low power circuits and techniques are presented. Using these techniques, an ULP sensor node with a 1mm^3 volume and lifetime of months to years can be realized.

In Section II, an ultra-low power processor for processing of sensor data managing communication protocols is examined. Section III reviews various types of low-power memories for data storage and Section IV discusses the power electronics aspects of the ultra-low power sensor nodes and the paper concludes in Section V.

II. Processor Design for ULP Millimeter-Scale Sensor Nodes

Sensors can gather large amounts of measurement data, but only a small portion of this data is typically of interest to the user. For example, motion detection sensors in surveillance systems measure audio/visual changes but they only need to report when any changes are detected. Therefore, most of the measurement data that indicate there is no change can be

ignored. Moreover, storing and transmitting raw measurement data requires larger memory and longer power-hungry radio activation time, which can be energy-inefficient. By performing on-chip digital signal processing to extract and compress useful sensor data with a microprocessor, energy consumed for storing and transmitting data can be significantly reduced.

For millimeter-scale sensor nodes, minimizing energy consumption is the critical concern for microprocessors to operate with stringent power budgets. Since dynamic switching energy scales quadratically with supply voltage (V_{DD}), dramatic energy reduction can be achieved by lowering V_{DD}. Therefore, aggressive supply voltage scaling could significantly reduce power consumptions [6][7]. However, voltage scaling also increases the delay of the circuits, especially when V_{DD} is lowered below the threshold voltage (V_{TH}) of the transistors; referred to as the subthreshold region. In this region, leakage power reduces with lower V_{DD}, but leakage energy per cycle rapidly increases due to increased delay. With typical V_{DD} (~1V today), active energy is orders of magnitude higher than leakage energy, but competing trends in dynamic and leakage energy at low voltage results in a voltage (V_{MIN}) where total energy per instruction (E_{MIN}) is minimized (as shown in Figure 2 [8][9]).

Aggressive voltage scaling enables much higher energy efficiency, but it reduces the robustness of circuits at the same time. This is due to the reduced noise margin and increased susceptibility to process variations. Lower supply voltage reduces the on-current to off-current ratio, which degrades the noise margins. Moreover, devices are more sensitive to process variations with low supply voltages. Random dopant fluctuations (RDF) are the dominant source of the V_{TH} variations with such low supply voltages. By removing high fan-in gates, series transmission gates, and dynamic logic, functional robustness can be sufficiently maintained. However, process variation can create up to 300% delay variation with subthreshold operation, leading to a high timing margin requirement. Since RDF is uncorrelated, its effects on critical path delay can be decreased by increasing the logic depth between pipeline stages. This allows more statistical averaging of gate delay variations [10].

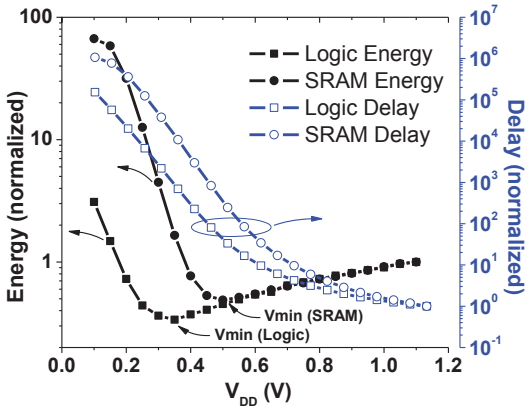


Figure 2. Dynamic energy and leakage power decrease as V_{DD} is scaled down. Latency and leakage energy per cycle increase. The minimum total energy per cycle is achieved at an intermediate voltage (V_{MIN}).

III. Memory Design for ULP Millimeter-scale Sensor Nodes

Memory in a sensor node is used as a temporary storage for the data measured by the sensor until it is collected by the user and can also be used as a scratchpad for complex data processing. Therefore, larger memory allows more infrequent data collection and more complex data processing. In general, denser memory is preferred for a fixed volume, but operating power must meet stringent limitations. For this reason, non-volatile memories such as flash memories are undesirable since they require high voltage charge pumps with very large power. This can quickly dominate sensor power budget, despite the fact that it has near-zero retention power consumption. This section describes two types of CMOS-compatible volatile memories that can be utilized in millimeter-scale sensor nodes: static random access memory (SRAM) and embedded dynamic random access memory (eDRAM).

A. SRAM

Voltage scaling in SRAM not only reduces dynamic power but also leakage power (Figure 2). But with low supply voltages, SRAM becomes more prone to functional failure due to the process variations which lead to destructive read operations and insufficient write margins [11]. Meanwhile, the SRAM bitcell yield must be extremely high for acceptable overall yield, since many sensor systems require large amounts of SRAM, where the vast majority of bitcells must be functional for chip yield.

In the conventional differential 6-transistor (6T) bitcell (Figure 3a), write margin can be improved by increasing the strength of the pass transistors (A_3, A_4) relative to the pull-up devices (A_1, A_2); read stability can be improved by increasing pull-down devices (A_5, A_6) relative to the pass transistors. Therefore, designing the bitcell for higher write margin generally decreases read stability, and vice versa. This creates a fundamental trade-off between write margin and read stability. Device sizing and SRAM assist circuits such as dual-V_{DD} wordline circuits can improve low-voltage SRAM robustness, but they are not sufficient to enable robust near-threshold or subthreshold SRAM [12].

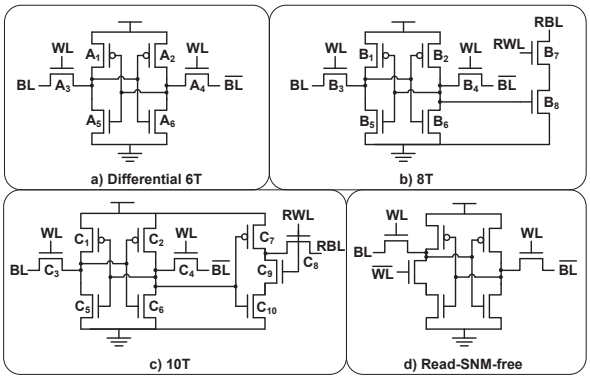


Figure 3. SRAM designs for low-voltage low-power operation.

The 8-transistor (8T) bitcell (Figure 3b) utilizes a separate buffer for read operation (B_7, B_8) [11][13], which allows the cross-coupled inverters and pass-gates to be sized optimally for writes. This makes the bitcell virtually immune to destructive reads, achieving higher low-voltage robustness at the expense of lower density. A 32kb sub-array of 8T SRAM was demonstrated with 295MHz operation at 0.41V [13]. Although the 8T bitcell is robust against the destructive reads, read operations can still fail if the read bitline (RBL) is pulled down to slowly during the read operation and fails to meet timing constraints. It can also fail due to the undesired RBL discharge by the leakage current of unaccessed bitcells. With low V_{DD}, the reduced on-to-off current ratio aggravates this failure mode. The 10T bitcell (Figure 3c) reduces the contention from unaccessed bitcells by lowering a read buffer leakage current with two off NFET devices (C_8, C_9) in series between the read bitline and ground. It also pulls up the RBL during the read of a ONE to prevent undesired discharge [14]. Bitline leakage can be further mitigated through compensation with leaking column headers or footers [15]. The read-SNM-free bitcell (Figure 3d) can also improve read margin by cutting the feedback loop during accesses [16].

B. Embedded DRAM

The 8T and 10T SRAMs achieve higher robustness than differential 6T SRAM at low voltages, but at the cost of a considerably larger area due to the increased device count. The increased bitcell area can limit the sizes of memories in a sensor node, especially when it requires a small form factor. Substantially denser memory can be implemented with embedded DRAMs (eDRAMs) (Figure 4). This implementation only requires 2 or 3 devices per bit and it is fully logic compatible. Traditional DRAMs have a data storage capacitor connected to the read bitline (RBL) with an access transistor. A read operation is performed by sensing the charge redistribution between the storage capacitor and the RBL. To increase the read speeds, gain cell eDRAM uses the trans-conductance of a gain device (M_{GAIN}) [17]. Read speed is further improved in boosted gain cells where the voltage on the data storage node is boosted during a read operation. During a read operation, RWL is pulled down to V_{SS} and this transition couples the charge into the storage node (V_{NODE}) through the gate-source capacitance of M_{GAIN}. The boosting increases the overdrive voltage of the gain device and reduces read latency by 41% [18].

In addition to increased density, eDRAM has lower leakage power than SRAM due to reduced device counts. However, in eDRAM, data is stored as a floating charge which will eventually be discharged through the leakage current. Therefore, data must be periodically refreshed, requiring dynamic power consumption proportional to the refresh frequency. To increase retention time, the subthreshold leakage through the write device (M_{WR}) should be minimized. This subthreshold leakage current is especially large with the cells strong ZERO when the write bitline (WBL) is V_{DD} to write a ONE to an adjacent cell sharing the WBL. A boosted voltage on the write wordline (WWL) can be used to super-cutoff the write

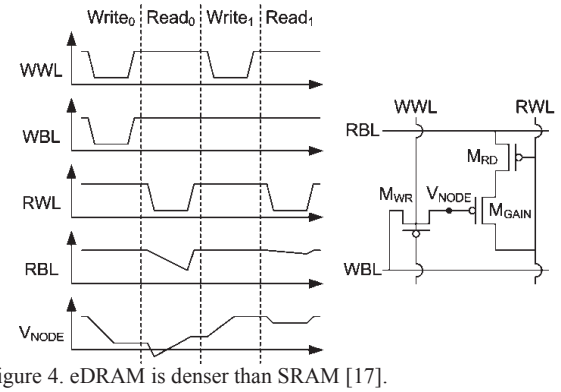


Figure 4. eDRAM is denser than SRAM [17].

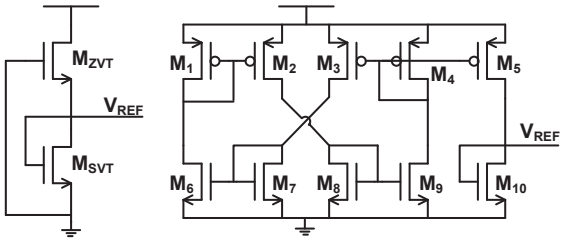
device. This will apply positive gate-source voltages for PMOS, resulting in lower-than-off drain current. However, this requires an additional charge pump or external power supply. Alternatively, a lower WBL voltage can be used for writing a ONE. For example, the steady-state voltage of V_{NODE} can be used to keep unaccessed M_{WR} devices super-cutoff, but it does not increase the off-current during the read of a ONE [17]. Since the subthreshold microprocessors for sensor nodes typically operate at low frequency, the threshold voltage of M_{WR} can be increased to reduce the leakage at the cost of slower write speed [19].

IV. Power Management Design for ULP Millimeter-scale Sensor Nodes

In a sensor node, each circuitry requires a different supply voltage for its energy-optimal or robust operation. For example, microprocessors and other digital circuits run with low supply voltages ranging from 300mV to 600mV since its energy optimal operating point is in subthreshold or near-threshold voltage regime. On the other hand, analog components require higher supply voltages to ensure robust operation with proper headroom and noise margins, which range from 1.2V to 2.5V. Meanwhile, common power sources incorporated in sensor node, such as lithium batteries (3.3-4.2V), alkaline batteries or zinc-air (1.5V) batteries, are limited in their output voltages by their chemistries, and their voltage degrades with use. The output voltages of these batteries do not usually match the desired circuit supply voltages, which also differ from block to block. Therefore, DC-to-DC converting power electronics are necessary in sensor nodes. Conventional power electronics are designed for high output power and are not efficient with low levels of power as low as sub μA, which is needed by sensor nodes. For energy-efficient operation, power electronics must be specifically designed for low power applications.

A. Linear Regulation

A linear regulator is a type of regulator that generates its output voltage by current-amplifying the reference voltage where the amplifier is powered by the higher input supply voltage. Therefore, ideal efficiency of a linear regulator is determined by the ratio of the output to input supply voltage. The actual efficiency is always lower than the ideal efficiency due to the power overhead of the quiescent current of the amplifier. Minimizing this quiescent is desired for high



a) Constant Reference b) CTAT Reference

Figure 5. References for voltage outputs for linear regulators [22][23].

regulating efficiency, but in turn it will reduce the bandwidth of the amplifier, degrading transient response to load current fluctuations. This results in larger output power supply noise, which can increase the latency of the load circuits and decrease SRAM robustness [20]. By dynamically increasing amplifier bias current whenever load power surge is detected, the regulator power can be minimized while maintaining proper bandwidth [21]. The power surges can be detected by dropping the supply voltage across a diode. This diode voltage controls both switches that limit the supply surges and the tail current devices used in the linear regulator.

The linear regulator requires input reference voltage which should be insensitive to supply voltage and temperature variation. Band gap and constant-g_m references are commonly used for its small sensitivity to supply and temperature variations, but they tend to have microamp-level quiescent currents that exceed the power budget of ultra-low-power sensor nodes. A voltage reference with picoamp-level bias current (Figure 5a) can be generated based on the subtraction of threshold voltages [22]. Since the threshold voltage of devices with different V_{TH}s scale together with temperature change, the difference is constant with temperature. Therefore, this voltage can be obtained by connecting a diode-connected nominal-V_{TH} NFET device (M_{SVT}) in series with a super-cutoff zero-V_{TH} NFET device (M_{ZVT}). With properly sized devices, the output voltage will settle to one half of the difference of the V_{TH}s of two devices because of the equal current condition. Since both devices are in the subthreshold region, this voltage reference with 19.4ppm/°C temperature dependency can be realized with only 2.2pW power consumption.

Another voltage reference with low temperature coefficients can be created by combining a complementary to absolute temperature (CTAT) device threshold voltage with a multiple of the proportional to absolute temperature (PTAT) thermal voltage [24]. With these voltage references, a CTAT power supply can be used in subthreshold circuits to keep the frequency of CMOS logic constant with temperature [23]. In this CTAT reference voltage (Figure 5b), a constant current is supplied through a diode-connected device (M_{10}). The temperature-independent current is generated by equating the currents of a high V_{TH} subthreshold device (M_6, M_8) with low V_{TH} saturated devices (M_7, M_9). With increased temperature, the device threshold of M_{10} and the reference voltage decrease. The CTAT power supply balances the effects of temperature on subthreshold logic, which is faster at high temperatures where threshold voltage decreases, resulting in less than 5% frequency variation with temperature.

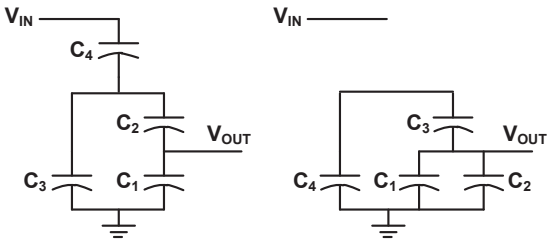


Figure 6. Fibonacci switched capacitor network for DC-DC conversion [26].

B. Switched Capacitor Networks

A linear regulator provides a stable level converted output voltage, but its regulation efficiency is limited to the ratio of the output voltage to the input voltage. Therefore, the efficiency for systems with high conversion ratios can be unacceptable. For example, converting a 3.6V Li-ion battery to subthreshold level can limit its efficiency to less than 20%. In these scenarios, higher power efficiencies can be attained with switched capacitor networks (SCN) or buck converters [7]. SCNs generate output DC voltages by connecting the voltage input and output to capacitors in different configurations. To generate DC voltage at a fixed ratio, SCNs commonly alternate between two configurations of capacitor networks by controlling switches connecting the capacitors. More than two configurations can be used to allow the circuit to convert DC values with several different ratios [25].

A hybrid SCN and linear regulator system can be a good candidate for a voltage regulating system in ultra-low power sensor node. For conversion from 3.6V Li-ion battery to subthreshold voltage levels with 5nA to 500nA load current, 55% conversion efficiency is achieved, which is 4.6× efficiency improvement over ideal linear regulation [26]. A Fibonacci SCN network is used to divide the battery voltage by 5 (Figure 6). Normally, large MOS devices are used for SCNs to reduce conductive losses through switches. However, power overhead for switching the gate capacitances of these switches can be significant when the SCN network is designed for very low power load. Therefore, nearly minimum sized devices are used for switches and low switching frequency of 2kHz is used in this system, whereas typical SCNs are clocked at MHz levels. Due to the switching nature of SCNs, the outputs of SCNs are noisy unless the switching frequency of the network is very high. Since the power budget and low output voltage precludes such high frequency operation, a linear regulator with a low bias current of 5nA is used to eliminate voltage ripples at the output.

C. Buck Converters

Buck converters generate regulated output by alternating between connecting the inductor to the power source to store energy and delivering the stored energy into the load (Figure 7) [27]. The DC-DC conversion ratio of a buck converter is determined by the duty cycle between storing and delivering energy. Therefore, by dynamically adjusting this duty cycle, output voltage can track the minimum energy point (V_{MIN}) to achieve the highest efficiency operation of digital logic components [28]. A buck converter can be an attractive voltage

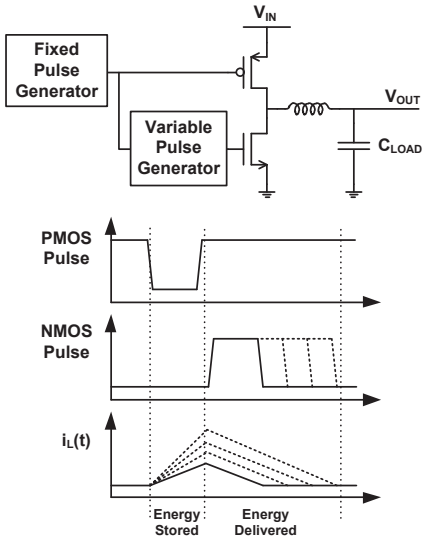


Figure 7. Buck Converter that supplies the energy optimal V_{DD} [28].

regulator where fine tuning for DC-DC conversion ratio is required. However, its efficiency rapidly drops with low load current and it requires large inductor for high efficiency which can occupy significant silicon area of millimeter-scale sensor nodes. Therefore, for supplying power for a sensor node in idle mode, where no precise voltage control is required and load current is very low, SCN is preferred.

V. Conclusion

The emergence of millimeter-scale sensor systems is predicted along with the continuous scaling of computing systems. These miniature sensors with long lifetimes can be realized by reconsidering every circuit element in the sensor system for ultra-low power operation. Recent advances in ultra-low power circuit and system designs make devices for new applications possible, such as intraocular pressure sensing. Such millimeter-scale sensor systems will create numerous new extremely volume-constrained applications, and also replace many of today's bulky, expensive and power hungry wireless sensors in other applications.

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