27.2 A 467nW CMOS Visual Motion Sensor with Temporal Averaging and Pixel Aggregation

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Visual monitoring with CMOS image sensors opens up a variety of new applications for wireless sensor nodes, ranging from military surveillance to in vivo molecular imaging. In particular, the ability to detect motion can enable more intelligent power management through on-demand duty cycling and reduced data-retention requirements. Conventional imager designs focus on achieving higher resolution, frame rate [1], or dynamic range [2], resulting in power consumption levels that are unsuitable for battery-powered wireless sensor nodes [3].

Several in-pixel motion-detection (MD) designs have been proposed [4,5], in which the previous pixel value is stored on an in-pixel capacitor until the end of the next integration cycle for immediate frame differencing. This avoids the need for high-power DSP. However, these designs implement MD in all pixels and still consume mWs of power. In addition, the in-pixel schemes are limited to frame differencing of two consecutive frames, reducing sensitivity to slow-moving objects compared to more sophisticated DSP approaches that operate on multiple frames.

To capitalize on the low-power aspect of in-pixel frame differencing without compromising sensitivity to slow-moving objects, we propose temporal averaging (TA), where multiple pixels are selectively aggregated with a per-cluster offset-canceling scheme ([5,1]). In TA mode, the previous pixel value on CHOLD is buffered through a p-type source follower input device M1, and column line access device M2. A TA cell consists of a TA-SHA pixel, source follower input device M1, and column line access device M2. A 15.6μm2 pMOS parasitic diode is used as the photodiode. The base pixel is used only for regular imaging, and its spare layout area is shared for capacitance tomography (PA), where multiple pixels are selectively aggregated with a per-cluster offset-canceling scheme ([5,1]). In PA mode, the previous pixel value on CHOLD is buffered through an in-pixel capacitor M3-5 and C_HOLD to retain the previous frame’s pixel value. Subthreshold leakage through M3 is the primary leakage source for C_HOLD; hence, the performance is pulled low to ~200μV to super-cutoff M3. The leakage leakage-injected droop of 5mV for 200μs (1% of signal range). C_HOLD for TA unit is 3× larger than in the PA unit, in accordance with the integration period ratio. All explicit capacitors are distributed in the cluster, with a unit capacitance value of 25fF. Of 61 (64 - 3 SHA pixels) available shared slots, 24×2 are used for TA C_HOLD, 3×2 for TA C_TAVG, and 7 for PA C_HOLD. M8-9 connect PA photodiodes to the cluster’s charge sharing network, V_CSN. Up to 4×4 PA-COMM pixels can be selectively aggregated with PA-SHA per cluster. All devices in the array, including capacitors, are thick-oxide I/O devices to minimize gate and subthreshold leakage.

Column readout uses the n-type source follower M1, whose output is sampled by M12 onto C_SMP when COL_EN is high. For columns with MD units (3 per 8), additional column peripheral circuitry including M14-15 is added. During MD mode, the previous pixel value on C_HOLD is buffered through a p-type source follower M4, and the current pixel value is buffered twice through M1 and M15 to provide the same common mode. The resulting two analog signals, V_PREV and V_CUR, feed into the MD comparator to determine the presence of motion. The only mismatch that must be considered between V_PREV and V_CUR arises from process variation between M4 and M15, and is addressed with an offset-cancelation scheme (Fig. 27.2.4). A 9b single-slope ADC is implemented per column to capture regular images, and is only used during imaging mode.

The timing diagram for offset cancellation scheme and MD comparison are shown in Fig. 27.2.4. When one integration period is complete, the MD controller and 250kHz clock are enabled. The source followers of Row [i] are enabled by EN[i] and MD_EN, after which the difference between V_PREV and V_CUR is sampled onto C1 by φ1. When SMP[i] goes high, the previous pixel value is overwritten by the current pixel value, and V_CUVPREV is sampled onto C2. During φ3 the MD comparison occurs, with C1 and C2 in series subtracting out the MD mismatch. Coupling capacitors C1×2 and pulses P1×3 are used to set the motion threshold and latch MD output, as shown in Fig. 27.2.4 (bottom right). The MD output (Motion) triggers if V_CUVPREV is greater than the coupled voltage from C1×2. After marching through 16 rows, φ5 cuts off static power through the MD comparator, and the 250kHz clock is disabled until the subsequent integration finishes. TA and PA units are separately controlled and can operate simultaneously with different frame rates since the column readout structure is independent with its own peripherals.

The proposed design is fabricated in a logic 130nm 8M1P CMOS technology. Figure 27.2.5 shows measured results. In MD mode, the sensor consumes 467nW at 5fps with both TA and PA enabled. In imaging mode, the chip consumes 16μW at 6.4fps. Experiments show that TA cells are effective for motions slower than 70 pixels/s, boosting the detection level by up to 42%. PA cells capture moving objects smaller than 2 pixels wide, providing nearly complete visual coverage despite the use of sub-arrays for detection.

References:
Figure 27.2.1: Temporal averaging (TA) increases sensitivity to slow motions (conceptual diagram at top-left, simulation results at right), while pixel aggregation (PA) reduce blindspots (bottom).

Figure 27.2.2: System block diagram showing pixel placements within a motion detection (MD) cluster.

Figure 27.2.3: Pixel and column schematics. Different pixels have different add-ons to the base 3-T pixel.

Figure 27.2.4: Timing diagram of readout scheme and schematics of offset cancellation and MD thresholding circuit. The example scenario shows motion being detected (bottom right).

Figure 27.2.5: Measurement results. TA pixels are shown to be effective for slow motion (top left). With PA turned off, objects smaller than 7cm at 5m away can escape detection entirely (top right).

Figure 27.2.6: Comparison table and sample images.
Figure 27.2.7: Die micrograph.