Fig. 28.1.2 shows an SSN crosspoint circuit and the priority storage latch. During a request/release cycle channels are indexed using the lower 64 bits from the input bus. Crosspoints send acknowledgement over the upper 64 bits. SSN also features a 4-level message-based QoS arbitration technique that allows only input buses with the highest message priority to arbitrate for the channel (Fig. 28.1.3). A 2-bit message priority is decoded into a 4-bit thermometer code at the crosspoint, which is used to selectively discharge priority bit-lines comprising the QoS priority bus. A multiplexer samples one of those priority bit-lines using its own message priority and the input bus progresses to the LRG arbitration cycle if the monitored priority bit is not discharged. Using separate wires for QoS arbitration incurs 3% area overhead. However, the additional QoS arbitration cycle can be overlapped with the prior routing operation for the output bus, avoiding a latency penalty. The SSN features 8448 word-lines and 8576 bit-lines spread across 4096 crosspoints. The integration of the LRG and QoS control within this fabric with low overhead greatly improves SSN scalability to realize a fabric of large size. In addition, new bi-directional repeaters (Fig. 28.1.3) are used for bit-lines that use a regenerative sensing element to improve delay despite high slew rates on long bit-lines. The regeneration reduces bit-line delay by 32% and allows for a 50% smaller bit-line driver compared to a conventional repeater (Fig. 28.1.4, simulated). Simulated fabric latency shows 1.6× performance benefit from repeated bit-lines (Fig. 28.1.4) and near-linear latency increase with radix size. Fine grain clock gating reduces clock power by 94% at each crosspoint with 2.3% added delay. A crosspoint is clocked only if its connectivity status is ON, a request is asserted, or an LRG priority update occurs. Adjacent input ports are driven from opposite directions, reducing routing congestion and local Ldi/dt drop when repeaters on the 2.5mm long input bus switch.

The SSN achieves 4.57Tb/s at 1.1V with an efficiency of 3.47Tb/s/W (Fig. 28.1.5), which is 3.7× higher than [4] at similar bandwidth. [4] uses an 8×8 mesh topology based on 5×5 routers at each node to connect 64 units whereas SSN uses a 64×64 single stage fabric. SSN is fully functional down to 550mV with a measured peak efficiency of 7.47Tb/s/W at 0.6V. Architectural simulations show that the worst-case cache access latency for conflicting requests improves by 1.8× for an SSN-enabled 64-core system due to the implemented LRG algorithm (Fig. 28.1.6). A routing study shows that only one metal layer in each direction (NS/EW) is needed, requiring 12% of routing tracks in these layers to connect 64 cores and caches with the SSN.

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References

28.1.1: SSN architecture with LRG priority update

28.1.2: Crosspoint circuit and priority storage latch

28.1.3: QoS arbitration technique and bit-line repeater

28.1.4: Simulated SSN delay and efficiency scaling

28.1.5: Measured SSN performance and power and comparison with prior switch fabrics

28.1.6: Architectural evaluation of SSN enabled 64 core system with SPLASH 2 benchmarks