Special Section Briefs

Self-Timed Regenerators for High-Speed and Low-Power On-Chip Global Interconnect

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***Abstract*—In this paper, we propose a new circuit technique called self-timed regenerator (STR) to improve both speed and power for on-chip global interconnects. The proposed circuits are placed along global wires to compensate the loss in resistive wires and to amplify the effect of wire inductance in the wires to enable transmission line like behavior. For different wire widths, the number of STR and sizing of the transistors are optimized to accelerate the signal propagation while consuming minimum power. In 90-nm CMOS technology, STR design achieved a delay improvement of 14% over the conventional repeater design. Furthermore, 20% power reduction is achieved for iso-delay, and 8% delay improvement for iso-power compared with the repeater design. The proposed technique has also been applied to a clock distribution network, reducing clock power by 26%.**

***Index Terms*—Circuit, interconnect, repeaters, signaling.**

I. Introduction

As technology continues to scale, the delay of local wires decreases while the delay of global wires remains the same or even increases. Furthermore, the requirement of high clock frequency leads to careful consideration of inductance of the lines, dispersion, and other transmission line effects. On-chip global interconnects are becoming a major bottleneck for circuit design with respect to overall chip performance and power constraints. Until now, repeaters have been the commonly used method to reduce the quadratic dependence of interconnect delay on wire length. However, as CMOS technology scaling continues, the number of repeaters increases dramatically. Deep submicrometer projections in [1] show that global interconnect distribution (repeaters + wires) will consume ∼40% of the total power in 50-nm technology. Recently, a microprocessor design [2] reported using as many as 12 900 repeaters showing that power and area overhead due to repeaters is becoming a serious concern.

A number of methods to address interconnect issues without using repeaters has been proposed [3]–[5]. The first design uses so-called boosters [3] where extra current is supplied when a transition is detected. However, the fact that it has a stack of two transistors in the charge path limits the speed improvement. In [4], a method is proposed where the receiver biases the voltage at which a transition is detected based on the expected transition direction. Reference [5] proposed a capacitive coupling accelerator, similar to a booster, to reduce resistance–capacitance (*RC*) delay, but the improvement over repeater design was not significant. Reducing the voltage swing has been used [6] to improve power, but is problematic in that another power rail has to be present and the delay tradeoff is not highly favorable. Finally, alternative approaches include modulated signaling [7] and pulsed current-mode signaling [8]. These methods achieved near speed-of-light latency, but they require wide wire topologies with low loss characteristics and the complexity of these designs makes them difficult to adopt in the industry.

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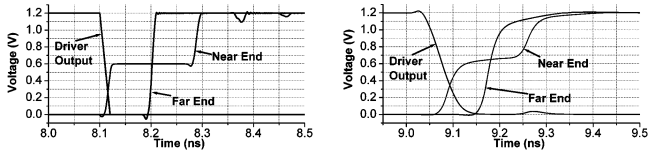


(a) Ideal transmission line (b) Wide interconnect ($40\mu m$)

Fig. 1. Interconnect with transmission line behavior.

In [9], we presented a new circuit technique to achieve high performance, repeater-less propagation for global interconnects. In this paper, we provide a new application study as well as extended results beyond those presented in [9]. The proposed design was implemented and tested for a number of interconnect structures and applied to a clock network design.

The remainder of this paper is organized as follows. Section II describes the operation of the self-timed regenerator (STR) circuit. Experimental results are found in Section III. The application of the proposed circuit in clock distribution network is described in Section IV. This paper is concluded in Section V.

II. STR Design

A. Transmission Line Configuration

We first consider a lossless transmission line where the driver is perfectly matched with the line impedance and the receiver is sufficiently small to present a negligible load. When the driver input transitions, a wave of $V_{\rm DD}/2$ will be propagated along the transmission line, due to the matching of the driver impedance. When the propagated wave reaches the receiver, this voltage will be doubled to the full rail due to the light loading of the receiver, as shown in Fig. 1(a). Note that while a reflected wave is sent back through the transmission line, this reflected wave will be absorbed completely by the driver since it is perfectly matched. This configuration is particularly advantageous for point-to-point signaling in VLSI designs, for instance between the processor and the cache. Taking advantage of reflection at the receiver termination to obtain a full swing signal allows the new design to be easily incorporated in existing design methodologies.

For a sufficiently wide wire, the resistance is insignificant and we obtain behavior similar to that of an ideal transmission line, as shown in Fig. 1(b). However, when the wire becomes thinner, the resistance becomes significant and the signal attenuates as it propagates through the wire. In this case, the signal swing at the receiver may not be sufficient to detect the transition reliably and signal propagation speed is also degraded. To compensate for this signal degradation, our design enhances the transition by properly supplying additional current, while still utilizing the impedance matching and the receiver reflection.

B. Circuit Operation

The STR is designed to quickly detect and accelerate the transition for a certain amount of time with a certain amount of current from the rail. Fig. 2 shows the STR circuit on both sides of the interconnect.

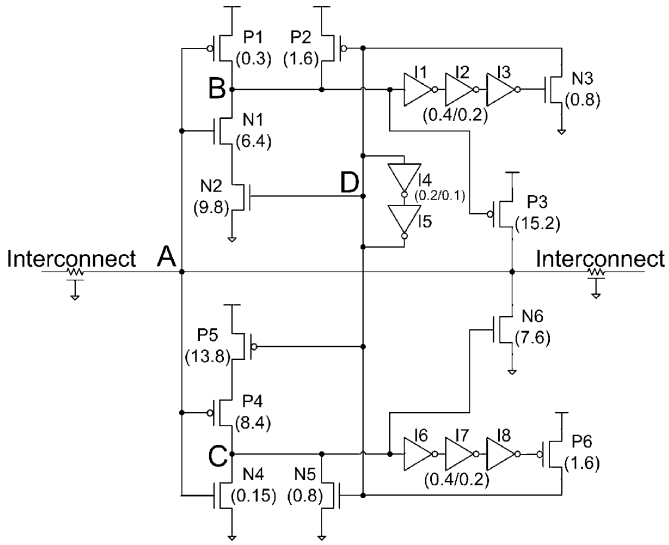
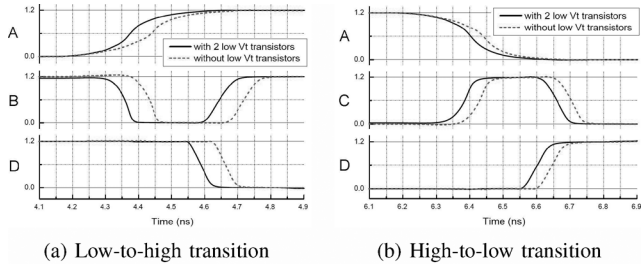


Fig. 2. STR circuit. Optimal sizing (unit: micrometers) for power reduction when five STRs are placed for a 0.45-μm wire is shown.



(a) Low-to-high transition (b) High-to-low transition

Fig. 3. Timing diagrams of STR at rising and falling transition. Speedup due to 2 low V_t transistors is shown.

The upper and lower part accelerates the rising and falling transition, respectively, each one being complementary to the other.

The main idea is to generate a pulse at nodes B and C which would turn on P3 and N6 for a time equal to the width of the pulse. When transistors P3 and N6 are turned on, additional current is supplied from the power rail to the propagating signal to expedite the transition. Transistors N1 and P4 are low threshold transistors which turn on quickly according to the polarity of the signal. P1 and N4 are weak transistors which are present only to establish and maintain initial conditions at nodes B and C. The delay set by the odd-number inverter chain determines the width of the pulse. The number and size of inverters in the chain can be optimized for different wires and constraints. This enables self-timing of the pulse width.

The initial state of the internal nodes of the circuit should be known. When the signal line is at low-voltage steady state, transistor P1 is driving node B to $V_{\rm DD}$. Node D is also set at $V_{\rm DD}$, making the pull-up circuit just ready to detect low-to-high transition while lower circuit remains insensitive to any rising transition. If any noise pulls node D down to GND, P4 and P5 charges node C and after going through a chain of inverters, P6 actively drives node D back to $V_{\rm DD}$, which is the desired initial condition. Similarly, when the signal line is at high-voltage steady state, node C and D is set at GND.

Upon a transition, the circuit works as follows and the timing diagram for each transition is shown at Fig. 3. Note that node A is the interconnect line itself. When the wire is initially at GND, the next transition will be a rising transition. Since transistor P5 is off, the pull-down circuit would be insensitive to this transition. When a rising transition is detected by N1, node B is pulled down to GND immediately as can be seen in Fig. 3(a). P3 turns on and it enhances the transition of the signal. After some delay, N3 turns on and node D is grounded, also shown in Fig. 3(a). P2 charges node B to $V_{\rm DD}$, so P3 turns off. After some time, N3 turns off but node D is maintained at GND by the cross-coupled inverters. Now, the pull-up circuit becomes insensitive to the high-to-low transition as N2 is turned off. In case of a falling transition, the timing waveforms of the internal nodes are shown in Fig. 3(b). Fig. 3 also compares the waveforms between the case when we use low V_t transistors for N1 and P4 and when we do not. Considerable performance improvement is observed by using 2 low V_t transistors in the STR.

A key feature of our design is that transistors (P2, N1, N2) and (P5, P4, N5) are never turned on simultaneously. This eliminates the fight during a transition which degrades the performance improvement and results in additional short circuit current, resulting in power reduction. In addition, the signal line is accelerated by a single transistor between the signal line and the supply rail allowing for a high drive current.

C. Sizing of the Circuit

Sizing of the STR circuit should be done carefully to facilitate the desired operation. An example of optimal sizing of STR is shown in Fig. 2. Transistors N1, N2, and P3, and P4, P5, and N6 are larger transistors than the others. As the number of STRs placed on a wire increases, their sizes get reduced. The size of transistors P3 and N6 determines the amount of current supplied to the signal line. Sizes of N1 and N2, and P4 and P5 determine the response time of the circuit to the propagating wave. The faster these transistors are, the more quickly transistors P3 and N6 get triggered and the better output waveform is at the far end of the wire. The rest of the transistors are not critical in terms of speed and are sized relatively smaller than these six transistors to minimize power consumption. N3 and P6 should be strong enough to switch the state of cross-coupled inverters. Sizes of P2 and N5 determine the slope of the trailing edge of the pulse. The sizing of STR is optimized using HSPICE optimizer and manual sweep for every combination of wire width and number of STRs placed on the line, resulting in different sizing for each situation.

Presence of handful transistors seems to pose STR as a timing critical circuit for sizing. However, other transistors besides the main six transistors are relatively not sensitive to sizing. In addition, depending on the technology, several optimal ratios can be imposed among the six critical transistors (i.e., P3/N6 $= 2$, N2/N1 $=$ P5/P4 $= 1.5$), which accelerates sizing.

D. Effect of STR on Signal Integrity

STRs create discontinuities in the transmission line as additional capacitive and resistive load. This causes the reflection of the original signal at positions where STRs are placed. In narrow wires, the dominant resistance of the line effectively suppresses these reflections. Although the resistance is less in wide wires, STRs are placed further apart, resulting in less reflections. Therefore, the extra inter-symbol interference generated by STRs are largely insignificant.

Another issue which needs to be addressed is inductive coupling. As STR is intended for long wires it increases the current loop thereby resulting in larger inductance, but this is compensated by the reduction in peak current in the STR scheme, which is shown in Section III. Furthermore, global wires or clock nets, which are the applications of STRs, are typically shielded with dedicated wires which provide well-defined return paths, thereby reducing inductive coupling.

III. Experimental Results

The 90-nm technology results are obtained from SPICE simulations for a broad range of wire widths using industrial device models. For

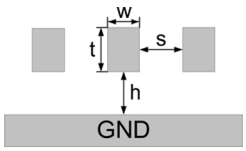


Fig. 4. Structure of global interconnect.

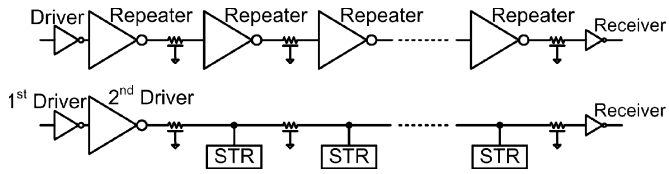


Fig. 5. Repeater/STR implementation scheme.

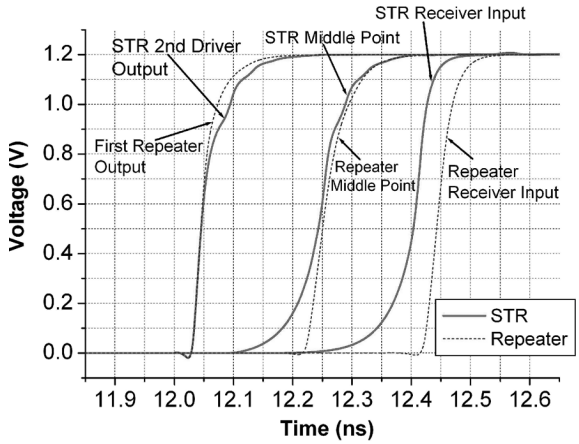


Fig. 6. STR and repeater simulation waveforms of 0.3-μm wide interconnect.

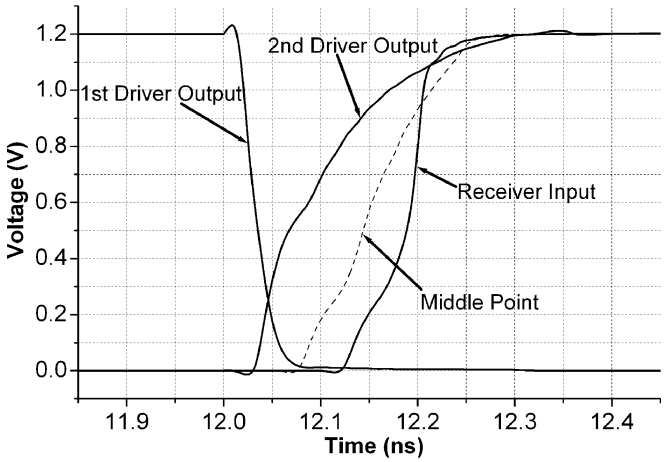


Fig. 7. STR simulation waveform of 4-μm-wide interconnect.

simulation of different wire widths, width w in Fig. 4 is changed and all the other parameters such as spacing, thickness, and distance from the ground plane are fixed. We modeled the interconnect as a top global layer metal with shielding wires on either side. Using a distributed *RLC* pi model, and each 25 μm of the wire is modeled as a lumped *RLC* circuit, and the *RLC* values have been extracted using FastHenry [10] and Predictive Technology Model [11] for a 10-mm line, and the line length is fixed throughout this paper.

We also compared the proposed STR and repeater technique against a traditional booster design [3]. However, the booster design was not able to improve on the performance of the repeater design even after extensive optimization of the transistor sizing of the booster topology. Hence, no comparison of our proposed approach against the booster design is given since the gains will be more than that compared to repeater designs. Previous reported measurements for the booster design were performed by measuring delay from the output of the inverter driving the interconnect to the input of the receiver gate. This method of delay measurement ignores the delay due to the loading of the initial driver and hence might not be accurate.

A. Repeater and STR Design Scheme

The overall scheme for repeater and STR is shown in Fig. 5. To make the comparison fair, we have identical initial drivers both in the repeater and STR scheme. In the repeater scheme, the first repeater is placed after the initial driver. In the STR scheme, the initial driver is followed by a stronger driver, which is sized properly to match the impedance of the line. Adding STR changes the load of the line which affects the impedance, but the difference is not significant. For example, the impedance of 1-μm wide wire when unloaded and loaded with STRs are 46.6 and 44.1 Ω, respectively. As a result, the optimum size of this second driver increases as the wire becomes wider. Throughout the interconnect, repeaters and STRs are inserted regularly. The delay is measured from the initial driver input to the final receiver output.

At each wire width, both the number and size of repeaters are swept to achieve best performance. Among all the combinations, optimal number and size of repeaters which result in the best case delay is chosen, and this serves as the baseline of comparison for the STR designs. Similarly, for a given wire geometry, both the sizing of STR and number of STRs along the interconnect is varied and optimized to achieve better energy and delay compared to the repeater scheme. For simplicity, all repeaters and STRs are sized identically.

Fig. 6 shows the waveform of intermediate nodes of 0.3-μm-wide wire simulation for STRs and repeaters. For this lossy wire, we see significant delay improvement using STRs compared to the repeater design. The waveform of a 4-μm-wide interconnect is shown in Fig. 7. Since the resistance of the wire is now reduced significantly, we start to see the transmission line effects with reflections at the far end. This results in faster transition time at the output of the interconnect than an intermediate point of the wire. The overall power and performance comparison is summarized in Table I.

B. Power, Area, and Peak Current

To measure the amount of power savings we achieve with STRs, the power comparison of the two designs is performed with the same delay. For iso-delay, power reduction up to 19.8% is achieved in the STR design as shown in Table I. This is first due to the fact that smaller numbers of STRs are needed than that of repeaters at the same delay constraint. Also, the short-circuit current is minimized in the STR design because there is no strongly conducting direct path from $V_{\rm DD}$ to GND at any given time. Furthermore, the STR circuit need not be oversized to produce equivalent delay with repeaters. Therefore, the total device width (including drivers, receivers, STRs, and repeaters) is reduced significantly as shown in Table II. In Table I, we observe that power savings of STRs comparing to the repeaters decreases as the wire width increases. This is because the capacitance dominates the interconnect parasitics in wide wires, and therefore sizing down the STR cannot reduce the power dissipated by the capacitance by a large amount.

Peak current is an important metric in interconnect design since it determines the value of decoupling capacitance which suppresses noise and voltage droop. The maximum current is measured in each repeater and STR block for peak current. The results are shown in Table II for iso-delay case, and substantial savings in peak current are achieved.

TABLE I
STR POWER AND PERFORMANCE COMPARISON OPT. REPEATERS: OPTIMAL NUMBER OF REPEATERS, OPT. REGEN: OPTIMAL NUMBER OF STRS

Wire width	Opt. Repeaters	Power reduction (Iso-delay)	Opt. Regen	Delay improvement (Iso-power)	Opt. Regen	Delay improvement (Best case)	Opt. Regen
$0.3\mu m$	10	19.8%	6	7.7%	9	14.0%	13
$0.45\mu m$	8	17.6%	5	6.8%	6	13.8%	12
$1\mu m$	5	16.9%	3	7.4%	5	13.3%	10
$4\mu m$	2	10.9%	1	8.1%	1	11.8%	9

TABLE II
AREA AND PEAK CURRENT COMPARISON (ISO-DELAY)

Wire width	Scheme	Total device width	Peak current
$0.3\mu m$	Repeater	$738\mu m$	$7.1mA$
	STR	$451\mu m$ (-39%)	$3.1mA$ (-56%)
$1\mu m$	Repeater	$543\mu m$	$9.9mA$
	STR	$317\mu m$ (-42%)	$3.9mA$ (-61%)
$4\mu m$	Repeater	$282\mu m$	$12.5mA$
	STR	$130\mu m$ (-54%)	$3.5mA$ (-72%)

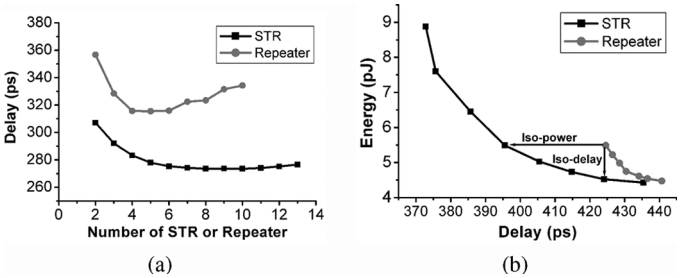


Fig. 8. (a) Delay comparison with different numbers of STRs and repeaters (width: 1 μm). Sizing is optimized for each different number of STR and repeater. (b) Energy versus delay of STR and repeater (width: 0.45 μm).

This is first due to fact that a direct path from $V_{\rm DD}$ and GND does not exist at any given time and secondly the transistor widths in STR are considerably smaller than those in repeater scheme. Also, whenever a transition is detected, the fact that the transition is accelerated for a self-timed window explains almost invariant peak current values across different wire widths.

C. Performance

For performance comparison, the power consumption of both STR and repeater design is set to be the same, and the delay is measured in each case. Across different wire widths, the maximum delay improvement is 8.1% for iso-power. Furthermore, we obtained the maximum performance with the STR design when performance has a higher priority than power consumption. Fig. 8(a) shows that the performance of the STR design dominates that of the repeater design. Performance improvement up to 14% is achieved, and it slightly decreases for wider wires.

Fig. 8(b) shows energy versus delay for STRs and repeaters. The data points in this plot are the minimum energy points obtainable with the given delay for STRs and repeaters. We can see that the STR energy-delay curve exists in the left-bottom side than that of the repeater.

D. Low V_t Repeaters and Leakage Power

Since we are exploiting 2 low V_t transistors in STRs, we also optimized repeaters with low V_t devices to achieve a comprehensive comparison. Fig. 9 shows the leakage power comparison with STR using two low V_t devices, repeaters with high V_t and low V_t. The data points in Fig. 9 for repeaters are the best case delay for each scheme. It is

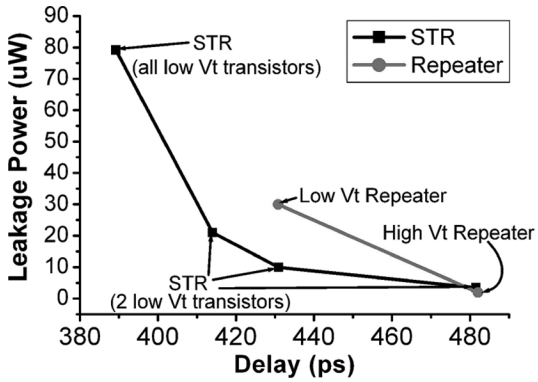


Fig. 9. Leakage power with different $V_{\rm t}$ assignments (width : 0.3 μm).

TABLE III
REPEATER AND STR LEAKAGE COMPARISON (I) : ISO-DELAY WITH LOW $V_{\rm t}$ REPEATER (II) : ISO-DELAY WITH HIGH $V_{\rm t}$ REPEATER.

Wire width (μm)	Repeater	Leakage (μW)	STR	Leakage (μW)
0.45	all lvt	28.01	(I)	11.70
	all hvt	1.86	(II)	4.76
1	all lvt	22.81	(I)	14.37
	all hvt	1.78	(II)	3.92

shown that although low V_t devices are used for all repeaters, it cannot reach the speed of STR, which has only 2 low V_t transistors. In a 0.3-μm-wide wire, the leakage power of STRs is 3$\times$ lower than that of low V_t repeaters for iso-delay. Since the total area in the STR scheme is only 50%$\sim$60% of that in the repeater scheme for iso-delay, leakage power is reduced although there are more transistors in STR comparing to a repeater. Also, these results show that our design has a very specific critical path so that we gain considerable speed improvement by using a few low $V_{\rm t}$ devices without sacrificing leakage power. As the wire becomes wider and the capacitance dominates the interconnect parasitics, leakage power improvement over the repeater design diminishes as shown in Table III.

IV. CLOCK NETWORK APPLICATION

One application of the STR is clock network design. To minimize skew and delay, global clock wires are typically very wide. This results in large wire capacitance and large clock drivers as well, consuming a considerable portion of the entire chip power. To reduce the width of the wires, we propose to place STRs along the clock wire to improve clock delay and clock skew, while meeting the same constraint as in the conventional case with wide wires.

Fig. 10 shows the spine clock distribution network without and with STR. The clock speed is set at 1 GHz, and the objective is to keep the maximum clock skew less than 15 ps between any two nodes out of the eight leaf nodes N0$\sim$N7, the clock delay less than 150 ps, and the clock slope less than 70 ps. The clock delay is defined as the worst

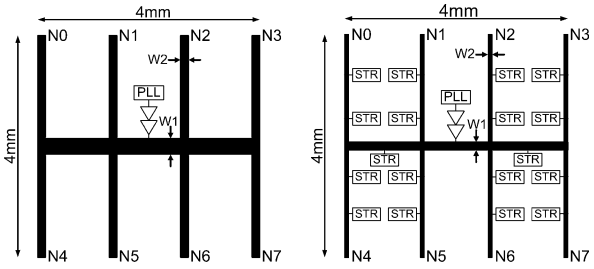


Fig. 10. Spine clock distribution network configuration ($W1/W2 = 2$).

TABLE IV
CLOCK DISTRIBUTION NETWORK COMPARISON ($W1/W2 = 2$)

Scheme	W1	Power	Skew	Delay	Slope
No STR	$8\mu m$	$19.1mW$	$11.8ps$	$130ps$	$51ps$
With STR	$5\mu m$	$14.1mW$	$8.9ps$	$140ps$	$59ps$

delay from the driver input to a leaf node, and the slope is defined as the worst delay between the 20% and 80% point of the clock signal at a leaf node. Without using any STR in the clock network, we had to use 8 μm for W1 and 4 μm for W2 to meet the given constraint. When STRs are added approximately every 0.8 mm along the clock path, the W1 and W2 could be reduced down to 5 and 2.5 μm, respectively, while maintaining similar clock skew, delay, and slope. Considering that the distance of clock net to multiple destinations cannot be perfectly matched, especially in spine clock networks, adding STR per unit length as suggested can compensate for the inherent skew between different nodes. The comparison results of the two clock distribution networks are shown in Table IV. By reducing the clock width substantially, the clock driver need not be sized as much as the conventional case to keep the slope similar, and the capacitance of the clock wires decreased significantly as well. In result, clock power consumption is reduced by 26.2%.

Although the transistor count is more in the STR scheme, under PVT variations, the spread of skew, delay, and slope were found to be actually less than that in the scheme without STR. This would be due to the averaging effect in the presence of more transistors.

V. CONCLUSION

In this paper, we presented a new circuit technique to improve delay and save power for global interconnects. For a 10-mm wire, we could achieve up to 20% power reduction, 2× peak current reduction, and 3× leakage power reduction than the repeaters. Applying STRs in a spine clock distribution network reduces the width of the clock wires considerably while meeting the same skew and delay constraints as in the conventional case, resulting in 26% power reduction.

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A Current-Recycling Technique for Shadow-Match-Line Sensing in Content-Addressable Memories

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***Abstract*—A current-recycling technique for shadow-match-line (SML) sensing in content-addressable memories (CAMs) is presented. In order to minimize energy-overhead, a novel current-recycling voltage detector (CRVD) is devised, whose working current is reused to charge up the match-line (ML) to determine matches or mismatches. Furthermore, with this CRVD, the word circuits realize fast-disable of the charging paths in case of mismatches. Since the majority of CAM words are mismatched, a significant power is reduced with a high search speed. Pre-layout simulation results show the proposed 256-word × 144-bit ternary CAM, based on a 0.13-μm 1.2-V CMOS process, achieves 0.51 fJ/bit/search for the word circuit with less than 900-ps search time. The achievement illustrates a 74.2% energy-delay-product (EDP) reduction as compared with the speed-optimized current-saving scheme. Post-layout simulation results of the word circuits show 0.65 fJ/bit/search energy per search with 1.2-ns search time.**

***Index Terms*—Content-addressable memory (CAM), current- recycling, low power, shadow-match-line (SML) scheme.**

I. INTRODUCTION

Content-addressable memories (CAMs) compare input search data against a table of stored data and return the address of the matching data. CAMs, especially fully parallel ones, have a single clock cycle throughput that makes them faster than other hardware- and software-based search systems. Thus, CAMs are extensively used in many high-

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