Computing the Soft Error Rate of a Combinational Logic Circuit Using Parameterized Descriptors

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Abstract—Soft errors have emerged as an important reliability challenge for nanoscale very large scale integration designs. In this paper, we present a fast and efficient soft error rate (SER) analysis methodology for combinational circuits. We first present a novel parametric waveform model based on the Weibull function to represent particle strikes at individual nodes in the circuit. We then describe the construction of the descriptor object that efficiently captures the correlation between the transient waveforms and their associated rate distribution functions. The proposed algorithm consists of operations to inject, propagate, and merge these descriptors while traversing forward along the gates in a circuit. The parameterized waveforms enable an efficient static approach to calculate the SER of a circuit. We exercise the proposed approach on a wide variety of combinational circuits and observe that our algorithm has linear runtime with the size of the circuit. The runtimes for soft error estimation were observed to be in the order of about 1 s, compared to several minutes or even hours for previously proposed methods.

Index Terms—Error analysis, estimation, simulation, transient propagation.

I. INTRODUCTION

SOFT ERRORS are produced when a radiation particle passes through a strong electric field region in a semiconductor device and generates free electron–hole pairs. If such an event occurs near the depletion region of a reverse-biased p-n junction, the free mobile carriers are efficiently collected by the high electric field present across the p-n junction. Subsequently, a transient noise pulse is generated due to the current flowing through the reverse-biased p-n junction. This single-event transient (SET), if registered by a latch, can cause a functional/data error resulting in a single-event upset (SEU). Errors resulting from such transient upsets are referred to as “soft” errors, as no permanent damage is done to the device, and the rate at which they occur is called the soft error rate (SER). A quantitative metric called failures-in-time (FIT) that measures the number of errors that can occur in one billion device hours is used to provide a calculable estimate for the error rates in industrial logic blocks. In a typical integrated circuit, memory arrays, latch elements, and combinational logic are all susceptible to soft errors.

The continued trend in technology scaling has resulted in soft errors becoming an increasing concern for digital circuits in the nanometer regime. Reduced feature sizes, higher logic densities, shrinking node capacitances, lower operating voltages, and shorter pipeline depths have resulted in a significant increase in the sensitivity of integrated circuits to radiation-induced SEUs. A number of studies examining the impact of technology scaling on the SERs of CMOS circuits have been presented [1]–[6]. Although memory arrays represent a large portion of the chip area that is vulnerable to soft error strikes, a continued reduction in both the critical charge and the collection efficiency has resulted in static RAM SER staying constant over several technology generations. In addition, the use of error-correcting codes enables a high level of soft error protection for memory structures. Similarly, industrial estimates show that the nominal SER of latches is approximately constant from the 130- to 65-nm technologies [2], [7]. The development of radiation-hardened latches [8], [9] with minimal overheads has further lessened the possibility of soft errors occurring in latches. Consequently, for current and future technologies, the impact of soft errors on combinational elements is receiving significant attention. It is predicted that at the 45-nm technology node, a majority of the observed soft failures will be related to SET events that occur in logic blocks [1], [10]. Hence, it is critically important to develop effective techniques to analyze and quantify the impact of soft errors on combinational logic circuits.

At ground level, soft errors are primarily induced due to different types of radiation mechanisms such as [11] ionization by alpha particles, interaction of low-energy thermal neutrons with boron isotopes, and collision of high-energy atmospheric neutrons with the silicon nucleus. The amount of charge collected due to neutrons (10–150 fC/µm) is significantly higher [11] than the charge collected by alpha particles (4–16 fC/µm). Errors caused by alpha particles and thermal neutrons can be minimized using suitable packaging components. However, since atmospheric cosmic neutrons cannot be filtered out using specialized packaging materials, there are no known physical solutions for neutron-induced signal interference.

In this paper, we develop an efficient analysis methodology to compute the SER of combinational logic blocks that are
susceptible to SEUs due to high-energy neutron strikes. We first use a transient current model to describe the gate-level effects of a particle strike on a diffusion region in the circuit [12]. These voltage transients are modeled using the Weibull probability density function that provides accurate waveform representations. The amount of charge collected due to neutron strikes varies over a wide range; the rate distribution corresponding to this set of strikes is modeled using the analytical expressions presented in [13] and [14]. We then describe the construction of the novel SET descriptor object that relates the transient waveform shapes with the corresponding SET rate distribution. The effect of particle strikes on a node is represented in an individual SET descriptor consisting of two simple functions, namely: 1) a waveform shape descriptor described by a parametric Weibull function and 2) a rate function described by a discrete set of error rate numbers. The proposed algorithm proceeds in a bottom-up fashion by injecting SET descriptors at each node and then propagating them along sensitizable paths in the circuit. We employ a merging operation to identify independent strike events with the same waveform shape function and combine the rate functions of the set of such SET descriptors into a single consolidated SET descriptor. The number of waveform shapes corresponding to injected strike events is enormous; however, after propagating through at most three to four gates, they converge into a small subset of waveform shapes. The merging operation efficiently recognizes such instances, thus minimizing the number of distinct waveforms to be propagated along the circuit. Similar to standard static timing analysis (STA), our algorithm requires a single pass through the circuit graph in topological order, and hence, the complexity is linear in the size of the circuit. Our algorithm shows that such an approach based on parameterized waveforms provides accurate and scalable soft error analysis for a variety of combinational circuits.

The remainder of this paper is organized as follows. In Section II, we provide an overview of previous work in this area. In Section III, we present the analytical models for modeling transient pulses and rate functions, and also describe the construction of the SET descriptor. We then detail the methods by which we propagate and merge the different SET descriptors in Section IV. In Section V, we provide algorithm runtimes and present a comparison of our method with SPICE simulations. Finally, we conclude in Section VI.

II. Prior Work

Previous approaches to soft error estimation can be broadly classified into two types, namely: 1) system-level approaches and 2) circuit-level methods. System-level estimation methods seek to compute the probability that a soft error at the gate level is manifested at the system level. An additional objective of these methods is to identify possible cases of errors that could cause the so-called silent data corruption. A detailed overview of an industrial system-level SER estimation method is presented in [15]. The authors in [16] describe the vulnerability factor at the microarchitectural level. In [17], the authors characterize the effects of transient pulses on microprocessor pipelines.

A number of methods have also been proposed in the literature to estimate circuit-level SER. The authors in [18] present a Monte-Carlo-based modeling program called SEMM. A methodology based on the single-event effect state transition model was developed in [19] to quantify the effect of SEUs on complex digital devices. Several methods proposed in the literature are based on models for transient fault injection and propagation [20]–[23]. The authors rely on simple device-level equations to predict the appearance of the transient pulse at the primary output. Other approaches such as those in [24]–[26] analyze the impact of different masking mechanisms on the SER of combinational circuits.

Recently, two new approaches to circuit-level SER estimation have been proposed. The SERA methodology presented in [14] combines various aspects of probability theory, circuit simulation, and fault simulation. The authors develop a path-based approach to inject pulses at individual nodes in the circuit and propagate them to the primary outputs or the latches using probability models. The algorithms presented in [27] and [28] encode particle strikes and fault events at nodes using decision diagrams (i.e., binary decision diagrams (BDDs) and algebraic decision diagrams). The authors then use standard algorithmic approaches to propagate these decision diagrams through the circuit. While these proposed methods are attractive, they are inherently expensive for large combinational circuits. The presence of reconvergence increases the number of paths in a circuit exponentially, thereby limiting the applicability of a path-based algorithm. Similarly, despite the prevalence of circuit partitioning techniques, BDD-based algorithms are inherently limited due to the memory blowup problems associated with them. Furthermore, these methods use overly simplified SPICE models (such as equivalent inverter chains and square pulses) while characterizing the cell library. As we describe in Sections IV-A and IV-B, it is important that the transient waveforms are characterized systematically to accurately capture the effects of various types of masking during the fault propagation operation.

In this paper, we present a static block-based linear-time algorithm to estimate the SERs of arbitrarily large combinational logic circuits. In contrast to previous approaches that use single parameters (such as pulse width or height) to describe the transient waveform, we present a Weibull-function-based model that provides several degrees of freedom and allows a highly accurate fit for various types of transient pulses. Second, we present a unified model called the SET descriptor (explained in Section III-B) that efficiently represents all SET strikes and their rate of occurrence at a victim node. The third key contribution of this paper is the observation that the shape of transient pulses originating at different victim nodes converges after a small number of propagations. This effect allows us to perform an efficient merging operation that leads to linear runtime complexity.

III. SER Analysis Model

In this section, we present an outline of the models used in our algorithm. We first explain our model for a single particle strike. Using this model, we then present a novel parametric
function that captures the effects of the entire range of particle strikes for one instance in a library cell. Finally, we describe the methodology for cell library characterization for SER analysis.

A. Single SET Model

For a given injected charge $Q_0$, the subsequent transient current through the reverse-biased p-n junction is modeled using the current waveform expression presented in [12], i.e.,

$$I(t) = \frac{2Q_0}{\tau \sqrt{\pi}} \sqrt{\frac{t}{\tau}} \exp\left(-\frac{t}{\tau}\right).$$

(1)

Here, $\tau$ is a technology-dependent pulse-shaping parameter. In contrast to other methods such as the double exponential current model [30], this time-dependent current waveform provides a simple yet accurate representation of the current waveform due to an SET. By using this current waveform in conjunction with a library gate, we obtain the output voltage response of the cell to a given amount of injected charge.

Previously, soft error transients have been characterized using pulse width as a single parameter [27] or with simple trapezoidal shapes [22]. Such methods are inherently problematic since they do not accurately capture the range of possible waveforms that can be generated due to a particle strike. The characteristics of the first strike waveform play an important role in determining the impact of electrical masking for propagation through the initial stages of logic. It is indeed accurate to characterize a transient pulse after a few propagations as a trapezoidal waveform. We observe that the Weibull function can be modified slightly to model these pulse shapes as well. This modification is illustrated in Fig. 1(b). We empirically limit the Weibull function to only match the rising and falling edges of the voltage waveform in the range of height between 0 and $V_{dd}$. The values of the Weibull function that are greater than $V_{dd}$ are irrelevant to our analysis. Although it is theoretically possible that a cosmic particle with sufficiently high energy will override the inherent capacitive clamping in a device and produce pulses with large overshoots (or undershoots), based on the given empirical model, we observe that such cases are nonexistent.

B. SET Distribution Model

In the previous subsection, we described the voltage waveform model for a single particle strike. For accurate SER analysis, it is necessary to consider the cumulative effect of the entire spectrum of neutron strikes. The range for the injected charge due to neutron strikes can be determined to be [10 fC, 150 fC] for the 0.13-μm technology [35]. SET strike events causing smaller charge collection occur much more frequently compared to strikes causing large charge collection. Using the empirical model presented in [13], the authors in [14] developed an analytical expression to describe the SET rate distribution, i.e.,

$$R = F \times K \times A \times \left(\frac{1}{Q_s}\right) \times \exp\left(-\frac{Q_0}{Q_s}\right).$$

(3)

Here, $R$ is the rate of SET strikes, $F$ is the neutron flux with energy (> 10 MeV), $A$ is the area of the circuit susceptible.
to neutron strikes (in square centimeters), $K$ is a technology-independent fitting parameter. $Q_0$ is the charge generated by the particle strike, and $Q_s$ is the charge collection slope. We adopt this simple charge-based model to correlate the electric charge injected by a particle strike with the rate of SET occurrence. The collection slope $Q_s$ is a measure of the magnitude of charge generated due to a neutron strike. Among the variables listed in (3), $A$ and $Q$ are dependent on the characteristics of the gate. The area parameter $A$ is set to the area of the n-type or the p-type drain depending on the input state of the gate. In [13], the authors observe that since $Q_s$(NMOS) > $Q_s$(PMOS), the SER due to strikes on NMOS drains is significantly greater (by about 100×) than strikes on PMOS drains. Note that the proposed algorithm is independent of the empirical model used for the rate function. Since we use discrete vectors to describe the rate values, the choice of analytical function used to generate the rate numbers does not influence the performance of the algorithm.

We use the aforementioned three-parameter Weibull function to represent the individual voltage waveforms. For a given cell, as we sweep over the range of charge values (10–150 fC), we observe that a wide set of voltage waveforms are generated. Each waveform in this set can be accorded a unique 3-tuple of Weibull parameters. In order to efficiently identify the entire set of waveforms corresponding to a range of energy levels, we seek to develop a functional relationship among the three parameters. In other words, capturing the relationship among the Weibull parameters using a simple polynomial equation is more efficient compared to identifying each waveform separately in a discrete manner.

If we assume that the three parameters are entirely unconstrained, then it is possible to determine the values of these constants using standard curve fitting techniques. However, such an unconstrained fitting mechanism will result in a one-to-many (aliasing) relationship between the transient waveforms and the Weibull 3-tuples such that one waveform can be represented with nearly equal error by two very different parameter 3-tuples. The existence of a unique one-to-one representation between the Weibull parameters and the voltage waveforms is an important requirement for the merging operation (described later in Section IV-C2) to ensure the optimality of the algorithm. Hence, we place constraints on the values of these parameters such that we obtain unique representations.

First, we categorize the waveforms into three types. (Cat1) First strikes: these correspond to a direct strike at any particular node in the circuit. (Cat2) First propagation: these correspond to the case when a pulse due to a first strike has propagated through exactly one gate. (Cat3) Subsequent propagations: These correspond to cases when the pulse has propagated through two or more gates. We also distinguish between rising and falling transitions in each case, resulting in six total categories. Cat2 is necessary to capture the crossover phase when the nonlinear Cat1 transient waveform is transformed to the standard Cat3 trapezoidal shape. (Note that for some cell/load combinations, Cat3 waveforms may not be entirely trapezoidal and can have shape closer to the Cat2 waveforms.) Using circuit simulations, we have determined that these three categories capture the entire family of waveforms possible in the circuit.

\[
\begin{align*}
\text{C} &= d_0 + d_1b. \\
\end{align*}
\]

Here, $(d_0,d_1)$ are the intercept and slope parameters for this linear equation. This straight line represents the entire set of charge values that can produce a transient pulse at a particular node. Additionally, we also identify the minimum ($b_{\text{min}}$) and maximum ($b_{\text{max}}$) values of $b$ corresponding to that bc line. For $b < b_{\text{min}}$, no transient pulse is generated at the node (electrical masking), and $b > b_{\text{max}}$ can be neglected since the probabilities associated with charge values above 150 fC are negligible.

Fig. 2 illustrates the construction of an individual SET descriptor. The charge values are first discretized so that $Q_i \in \{Q_1, Q_2, \ldots, Q_m\}$. We first determine the rate value $R_i$ corresponding to each $Q_i$ using (3). We then generate voltage pulses corresponding to each $Q_i$ and empirically calculate the

![Fig. 2. Construction of an SET descriptor.](image)
Weibull 3-tuples. While \( a \) is fixed, \( b_i \) and \( c_i \) vary across the range of \( Q_i \). After the set of \( b_i, c_i \) values are generated, we fit a linear equation to determine the pair of parameters \((d_0, d_1)\) that identify this particular set of transient waveforms. It is evident that there exists a one-to-one relationship between \( Q_i \) and \( R_i \) as well as \( Q_i \) and \( b_i \). Since we choose \( b \) as the free variable in our analysis, we store the strike rate information discretely in a pair of vectors. Thus, an individual SET descriptor consists of \( b_{\text{min}}/b_{\text{max}}, d_0, d_1 \) parameters that denote the waveform shapes, and the \( b, R \) vectors describe the strike rate values corresponding to each such transient. Note that the SET descriptor efficiently captures the effects of an entire set of waveforms. This is in contrast to previously proposed SER methodologies [14], [23] that analyze each strike event individually and hence incur larger computational overheads.

### C. Cell Library Characterization

While characterizing a cell library for SER analysis, we quickly recognize that an enormous number of transient waveforms are possible. The factors that influence the character of the transient waveform are the following: cell type, cell size, input state, output load, and the supply voltage \( V_{dd} \). In our analysis, we assume that the supply voltage for each cell is fixed at the nominal value. For every possible permutation among the other factors, a pair of parameters \( d_0 \) and \( d_1 \) represent the resultant transient wave. When the set of all such \((d_0, d_1)\) pairs is examined in the 2-D plane (Fig. 3), we see that a regular pattern exists such that clusters of points in this plane represent nearly-identical transient waves. Consequently, to reduce the sample space of possible transient waveforms, we discretize this 2-D plane by creating artificial grids. The grid sizes on the horizontal and vertical axes are carefully chosen such that all transients within a single grid exhibit nearly-identical behavior when propagated through any cell in the library. We choose a representative waveform candidate for each grid that symbolizes the type of transient for that range of \((d_0, d_1)\) values. We ensure that the chosen representative candidate has the largest number of discretizations so that the transient characteristics of all waveforms in a single grid are fully encapsulated by this single candidate. In this manner, we see that the large sample space of all possible transients can be efficiently represented by a small set of representative candidates. In our analysis, we observed that typically the number of such candidates (equal to the number of grids) is around 8–12.

The candidate waveform set is created in an incremental fashion for the three categories of waves described previously in Section III-B. To characterize the Cat2 waves, we only simulate gates with input transients chosen from the waveform candidates generated for the Cat1 waves. Since the Cat1 waveform candidates efficiently capture all possible types of first strike waves, it is sufficient to characterize for Cat2 first propagation waves using input transients from only this subset. Similarly, Cat3 waves are characterized using Cat2 waveform candidates as the input transients. In our analysis, we observed that a total of about 45 waveforms (inclusive of rising/falling transitions) accurately encompass all possible SETs that can occur from the cells in a given gate library.

Next, we measured the accuracy of the Weibull approach for the 45 candidate waveforms. For each waveform in each category, we computed the percent error between actual \((\text{time, voltage})\) points and the \( V(t) \) corresponding to each \((a, b, c)\) 3-tuple. In Table I, we list the results for rising/falling pulses and the three categories of waveforms.

We observe that falling pulses have lower error percent compared to rising pulses. We also observe that the trapezoidal pulses have larger error compared with the transients that are generated due to particle strikes. The maximum error in the modeling approach is about 20.4%.

### IV. Our Algorithm

In this section, we first examine the various factors that influence the SER of a logic circuit. These factors include the different masking mechanisms and the input states of the gates in the circuit. We then describe the proposed algorithm including the procedures for the propagation and merging of waveforms. Finally, we examine the complexity of the proposed algorithm.

#### A. Masking Mechanism

At any node in a combinational circuit, an SET causes a soft error only if it propagates through the subsequent logic and is observable at an external output, or if it is latched into a memory element of the circuit. There exist three well-known masking mechanisms that prevent an SET in combinational logic from causing a soft error [29].

1) Logical Masking: The propagation of an SET is logically masked if there does not exist a sensitzizable path from the location of the strike node to a primary output.
2) Electrical Masking: An SET can be electrically masked based on the characteristics of the driving cell and the input transient. For instance, given a cell with a large output load, it is possible that a majority of the SETs are attenuated when they propagate through such a gate.

3) Temporal Masking: An SET pulse arriving at a memory element is temporally masked if the clock of the memory element is inactive. In other words, an SET waveform can only cause a failure if it is inside the latching window [25] and corrupts the data bit being written into the memory register element such as a flip-flop or a latch.

Although these masking mechanisms serve as derating factors in reducing the probability of soft errors from occurring, it has been observed that their impact is lessening across technologies. Deeper processor pipelines have allowed higher clock rates that reduce temporal masking. As transistors are continually scaled to smaller feature sizes, the pulse attenuation effect is also decreased significantly so that the possibility of electrical masking is reduced [4].

For accurate SER estimation, it is crucial to account for all three masking mechanisms in the algorithmic framework. Both temporal and electrical masking mechanisms are strong functions of the SET pulse shape, which in turn is a function of the neutron strike characteristics. A brute-force analysis would simulate a large number of neutron strikes for each gate in the circuit and propagate the subsequent SET pulse through all possible paths in the circuit. However, such a method is computationally intractable for even medium-sized circuits. Our algorithm inherently accounts for these masking mechanisms by utilizing the efficient representation of SETs using waveform shape and rate distribution functions.

B. Cell States

An important improvement of the proposed algorithm is the inclusion of state dependence into the SER analysis framework. Previously proposed SEU analysis methods are prone to over-estimating the SER of individual gates since they assume a simplistic block-based model for each cell in the circuit. In these methods, a single equivalent gate (such as an inverter that is possibly sized up) replaces a candidate gate in the original circuit without regard to the possible input states of the candidate gate [14]. We illustrate the importance of considering state dependence in SER analysis by using the two-input NAND gate as an example.

Fig. 4 presents a comparison between the previous SEU analysis method and our method for the four separate input states. Irrespective of the input state, the equivalent gate method assumes that the susceptible node is the output node and the drain area under consideration is the total drain area of the entire cell. This type of generalization is inaccurate both in terms of the rate \( R \) values as well as the type of generated waveform shape for the SETs. For input state 11, the susceptible nodes are the PMOS drains that contribute a significantly lower amount (see Section III-B) to the SERs despite having 5\( \times \) the area of the NMOS transistors. On the other hand, for the input state 10, the susceptible node is the internal node \( I \) in the NAND gate (since the NMOS transistor connected to \( B \) is the one in the OFF state) and not the output node \( Y \). As a result, although the rate values for states 01 and 10 will be identical (proportional to the area of a single NMOS transistor), the range of waveform shapes generated will be different, thereby producing different parameters \((d0, d1)\) for the injected SET descriptor. In addition to first strike waves, it can also be observed that the behavior of a cell while propagating an input transient wave is uniquely determined according to the cell’s input state. Using the library characterization process described in Section III-C, we generate SET descriptors for only the relevant input states of a particular gate in the library. For instance, for the two-input NAND gate, no characterization is necessary for the 00 input state since the presence of two parallel PMOS transistors connected to the power rail significantly reduces the probability of transient pulses being either injected or propagated through such a gate.

C. Structure of the Algorithm

The general structure of our algorithm is similar to a standard STA. In STA, the actual arrival times are propagated forward along the nodes using a single topological pass through the entire circuit. The propagation characteristics for these parameters are dependent on various factors such as cell type, output load, and input slew. In our method, we store SET descriptors at each node in the circuit. For each initial strike condition, the parameters that describe the \( bc \) line and the discrete set of \((b, R)\) points are obtained from a precharacterized cell library. The algorithm traverses the circuit graph in topological order while performing the following two operations at each node \( i \): 1) propagation of each fanin SET descriptor from the driving gate’s input to output of \( i \), and 2) merging of propagated waves and rate functions at \( i \) to compute the total SET strike rate distribution at node \( i \). This total SET strike rate at any node represents the contribution to the strike rate of all the nodes in its fanin cone.

1) Propagation: The algorithm proceeds in a bottom-up fashion (using depth first search) by first injecting SETs at the input gates and proceeding along the nodes in a circuit toward the output. Depending on the input states of the gates, only a fraction of the entire set of gates is susceptible to soft error strikes. Initially, for a first strike waveform, an SET descriptor corresponding to one of the waveform candidates is generated at the injection node. We then propagate this SET descriptor forward through each gate as we traverse through the various sensitizable paths in the circuit. Depending on the
characteristics of the gate (cell size and output load), we use the lookup-table-based transfer function to transform an input SET descriptor to an output SET descriptor of appropriate type. When a waveform is propagated through a gate, the waveform shape (i.e., $d_0, d_1$ and vector $b$) parameters are transformed based on the precharacterized table while the rate values (vector $R$) are propagated as is. Note that since the precharacterized waveform library contains all information related to the input/output waveforms across a given cell, the effects of electrical masking are inherently accounted for by the propagation operation. While performing the transfer function across a gate, we first determine all possible SET descriptors for its inputs and then transfer these SET descriptors using our library of waveform candidates. This is similar to the method used in STA, where arrival times are first generated for all gate inputs, and a subsequent merge operation determines the arrival time at the gate output.

As transient waveforms propagate through the nodes in a circuit, we find that the resultant waves after a few propagations are nearly identical irrespective of the nature of the original first strike wave. This observation is based on the fact that most CMOS gates exhibit a unity transfer function after a few propagations. In other words, even if a large range of waveforms of type Cat1 are injected at various points in the fanin cone of a particular node, after a small number of propagations along the paths that reach that node, the number of type Cat3 waves will be small. As a result, it becomes increasingly important to identify such cases of waveform equivalence during the propagation operation. For instance, it is possible that a gate with two inputs, with each input having a large number of SET descriptors, can have a resultant set of SET descriptors at the output node containing a large set of waves that can possibly be merged. This is in direct contrast to a path-based analysis method that treats each possible SET event as an independent instance and thus incurs a large penalty due to the exponential number of possible paths. The ability to identify such instances of waveform equivalence and efficiently compact the large set of identical waves into a single output wave constitutes a key aspect of our proposed algorithm.

2) Merging: The use of the $(d_0, d_1)$ parameters for waveform identification enables us to quickly identify equivalent waves. At the end of the propagation operation at each gate output, we iterate through the resulting set of waves and compact SET descriptors with identical $(d_0, d_1)$ parameters into a single output SET descriptor. Note that while the vector of $b$ values in the SET descriptor will be identical, the vector of $R$ values may be different because of the difference in the originating SET descriptor. In such cases, we set the vector of $R$ values for the output to be the vector sum of $R$ values of the original two SET descriptors. In this manner, we see that for each node in the circuit, the set of all SET descriptors at that node is the combined effect of considering particle strikes at all possible nodes in the fanin cone of that node.

As an example for the merging operation, consider a circuit that consists of a chain of ten identical inverters [$INV_1, INV_{10}$]. The output of $INV_{10}$ is connected to a capacitive load equivalent to a single inverter. Naturally, ten possible strike locations (at the drain nodes of all inverters) exist. A path-based algorithm would treat each possible strike independently and predict that ten possible waveforms can possibly be generated at the output of $INV_{10}$. However, using our waveform compaction technique, we recognize that only four different types of waveforms are possible at the output of $INV_{10}$. Using the proposed algorithm, we observe that transient waveforms injected at the outputs of $INV_1, INV_7$ manifest themselves as nearly identical waves at the output of $INV_{10}$ since they converge to a single waveform candidate after four propagations. Combining this with three other waves generated at $INV_9$, $INV_6$, and $INV_{10}$, we get only four different classes of waveforms at the output of the inverter chain.

3) Temporal Masking Analysis: At the end of the bottom-up pass through the circuit, a final set of SET descriptors is generated at each output node. (Typically, we observed that each output contained about four to six different types of waveforms, even for large circuits.) Each output node of the circuit is connected to a standard D-flip-flop. Using SPICE measurements, we determined the output response of the flip-flop to the various waveform candidates belonging to three waveform categories. For each candidate, we calculate the temporal probability of that waveform latching into the memory element resulting in a soft error. The temporal probability calculation was performed using the pulse width overlap method [4], which identifies an error event when a transient wave completely overlaps the setup/hold time window ($T_{setup} + T_{hold}$) of the latching flip-flop. Given the clock period $T_C$ and a waveform $k$ with pulse width $T_{pw}$, the temporal probability $z(k)$ can be expressed as

$$z(k) = \begin{cases} 0, & T_{pw} \leq T_{setup} + T_{hold} \\ 1 - \frac{T_{pw} - (T_{setup} + T_{hold})}{T_C}, & T_{pw} \geq (T_{setup} + T_{hold}) \end{cases} \quad (5)$$

Fig. 5 highlights the interface between the SER analysis engine and the temporal masking method presented in the previous section. First, we observe the plot of strike probability values $R$ and the Weibull parameter $b$ corresponding to an individual SER descriptor. Note that each discrete point in this plot corresponds to an individual transient waveform. We then use the $(d_0, d_1)$ parameters of the SET descriptor as indices in a precharacterized lookup table to determine the exact pulse width ($w$) and height corresponding to each transient waveform $k$. It is important to recognize that a one-to-one monotonic relationship exists between parameter $b$, pulse width $w$, and injected charge $Q$ that generated this waveform so that $b_{min} \leftrightarrow w_{min} \leftrightarrow Q_{min}$ and $b_{max} \leftrightarrow w_{max} \leftrightarrow Q_{max}$. For the given transient pulse, we extract the temporal probability $z(k)$ and calculate the scaled strike probability $R_{scale}(b)$ value as $R_{scale}(b) = z(k)R(b)$. We perform this computation for each pulse in the SET descriptor and convert the $(b, R(b))$ plot into a (charge $Q$, $R_{scale}(Q)$) plot, as shown in Fig. 5. The charge values corresponding to parameter $b$ are not required to be stored in the descriptors. The one-to-one relationship ensures that $b_{max}$ corresponds exactly to the injected charge value of $Q = Q_{max} = 150 \text{fC}$. The $Q$ values for the other pulses in the descriptor can be determined by using the step value for charges in the initial discretization and the number of waveforms in the descriptors. (For instance, given a descriptor with 11 waveforms...
and step value of 5 fC for the injected charges, we determine that the smallest \( Q \) value corresponding to these waveforms is \( 150 - (11 - 1) * 5 = 100 \) fC and the largest \( Q \) value is, by definition, 150 fC.

From this analysis, we observe that for all charge values \( Q \) such that \( Q_{min} \leq Q \leq Q_{max} \), a soft error will occur in the logic circuit with a probability value indicated by \( R_{sc} \). The error rate value corresponding to the cumulative effect of all pulses in this SET descriptor \( d \) is determined by calculating the area under this strike probability curve as

\[
\text{SER}(d) = \int_{Q_{min}}^{\infty} R_{sc}(Q) dQ.
\]

For charge value \( Q > Q_{max} \) and, correspondingly, pulse widths \( w > w_{max} \), the strike probability value for the wave \( R(k) \) itself is set to be zero so that the contribution of pulse widths outside the \( [Q_{min}, Q_{max}] \) (and the corresponding \( [w_{min}, w_{max}] \)) range to \( \text{SER}(d) \) is zero. Since we use discrete vectors to describe \( R_{sc} \), we perform numerical integration (in Fig. 5) to calculate \( \text{SER}(d) \). The total circuit \( \text{SER} \) is then an aggregate of the \( \text{SER} \) due to each individual descriptor at each output node in the circuit, i.e.,

\[
\text{SER}_{total} = \sum_{\forall \text{output/\forall descriptor}} \text{SER}(d).
\]

Note that since we disregard the effects of reconvergent paths in our analysis, this value of \( \text{SER}_{total} \) represents an effective upper bound on the actual \( \text{SER} \) value of the circuit. However, it has been observed that the presence of reconvergence does not significantly influence the behavior of transient waveforms [14]. We propose to incorporate more accurate representations of reconvergence in future extensions of this paper.

D. Input Vector Dependence

The input vector dependence can be accounted for in two ways. 1) Compute the circuit \( \text{SER} \) over a large set of typical vectors (possibly obtained by running a set of benchmark programs on the system). For each vector, the logic values are first propagated through the circuit, and the SET descriptor corresponding to each input state is propagated only for the logically unmasked nodes. 2) Compute \( \text{SER} \) by first propagating static state probabilities using the method presented in [36]. For each gate, the rate vectors in the SET descriptors are weighted by the state probabilities and conditional propagation probabilities during the propagate and merge operation. The second method captures the entire input space; however, it is difficult to accurately account for the logic correlation due to path reconvergence. Therefore, for the sake of simplicity, we implemented the first method and calculated the average \( \text{SER} \) numbers.

E. Complexity Analysis

The algorithm proceeds as a single depth-first-search topological pass through the circuit. Beginning at the inputs, the algorithm builds up the SET descriptors at all the nodes as it traverses up the circuit. The merging operation is essential in identifying equivalent waveforms, thereby drastically reducing the number of propagated waves in the subsequent logic stages. For a given input vector, since a single pass through the circuit is sufficient to determine the SET descriptors at all possible outputs, the complexity of the algorithm is \( O(\#\text{Gates} \times \#\text{Waveform\_Candidates}) \). As mentioned previously, the number of waveform candidates is typically a small number (about 40–45). Section V presents a plot confirming that the average runtime of our algorithm over several input vectors is indeed linear in circuit size.

V. RESULTS

We implemented the proposed algorithm using C++. We exercised our algorithm on a Pentium IV machine with a 2.4-GHz processor and 1-GB RAM running Linux. We used a standard IBM 0.13-μm cell library during circuit synthesis. In (1), we set the value of \( \tau \) to be 35 ps [13]. In (3), we set the flux value \( F \) as 56.5 neutrons \( \cdot \) m\(^{-2}\)s\(^{-1}\), corresponding to the rate of neutron flux at sea level [37], and the fitting parameter \( K \) as \( 2.2 \times 10^{-5} \) [13]. Based on the technology-dependent estimates in [13] for the collection slope, we use \( Q_s(\text{NMOS}) = 17.3 \) fC and \( Q_s(\text{PMOS}) = 6.5 \) fC. We characterized the gates and generated the candidate waveforms as described in Section III-C. Note that this characterization process is a one-time effort that needs to be performed only once for a given library.

We first present the error rate and runtime results associated with our algorithm. Table II presents the runtime and error rate values obtained by running our algorithm on various
TABLE II
LIST OF CIRCUITS, SER VALUES, AND RUNTIES

<table>
<thead>
<tr>
<th>Circuit</th>
<th># Gates</th>
<th># Inputs</th>
<th># Outputs</th>
<th>Avg # Descriptors per Node</th>
<th>SER (# FIT)</th>
<th>R/t (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>i1</td>
<td>59</td>
<td>25</td>
<td>13</td>
<td>1.39</td>
<td>1.78E-05</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>i2</td>
<td>222</td>
<td>201</td>
<td>1</td>
<td>1.21</td>
<td>5.17E-05</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>i3</td>
<td>132</td>
<td>132</td>
<td>6</td>
<td>1.44</td>
<td>1.83E-06</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>i4</td>
<td>236</td>
<td>192</td>
<td>6</td>
<td>1.72</td>
<td>5.80E-06</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>i5</td>
<td>204</td>
<td>133</td>
<td>66</td>
<td>1.55</td>
<td>2.36E-05</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>i6</td>
<td>735</td>
<td>138</td>
<td>67</td>
<td>2.26</td>
<td>1.32E-04</td>
<td>0.01</td>
</tr>
<tr>
<td>i7</td>
<td>937</td>
<td>199</td>
<td>67</td>
<td>2.42</td>
<td>2.86E-04</td>
<td>0.01</td>
</tr>
<tr>
<td>i8</td>
<td>1609</td>
<td>133</td>
<td>81</td>
<td>2.08</td>
<td>2.98E-04</td>
<td>0.02</td>
</tr>
<tr>
<td>i9</td>
<td>1018</td>
<td>88</td>
<td>63</td>
<td>2.56</td>
<td>3.58E-04</td>
<td>0.01</td>
</tr>
<tr>
<td>i10</td>
<td>3379</td>
<td>257</td>
<td>244</td>
<td>2.36</td>
<td>4.33E-04</td>
<td>0.04</td>
</tr>
<tr>
<td>c17</td>
<td>7</td>
<td>5</td>
<td>2</td>
<td>1.26</td>
<td>6.95E-06</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>c432</td>
<td>246</td>
<td>36</td>
<td>7</td>
<td>1.69</td>
<td>1.82E-05</td>
<td>&lt;0.01</td>
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<tr>
<td>c499</td>
<td>750</td>
<td>41</td>
<td>32</td>
<td>1.89</td>
<td>6.23E-05</td>
<td>0.01</td>
</tr>
<tr>
<td>c880</td>
<td>591</td>
<td>60</td>
<td>26</td>
<td>1.96</td>
<td>6.55E-05</td>
<td>0.01</td>
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<tr>
<td>c1355</td>
<td>748</td>
<td>41</td>
<td>32</td>
<td>2.00</td>
<td>8.36E-05</td>
<td>0.01</td>
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<tr>
<td>c1908</td>
<td>760</td>
<td>33</td>
<td>25</td>
<td>1.87</td>
<td>8.32E-05</td>
<td>0.01</td>
</tr>
<tr>
<td>c3540</td>
<td>1951</td>
<td>50</td>
<td>22</td>
<td>2.49</td>
<td>9.16E-05</td>
<td>0.03</td>
</tr>
<tr>
<td>c6288</td>
<td>4836</td>
<td>32</td>
<td>32</td>
<td>2.34</td>
<td>4.53E-04</td>
<td>0.06</td>
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<tr>
<td>mul4x4</td>
<td>241</td>
<td>8</td>
<td>8</td>
<td>1.94</td>
<td>2.98E-05</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>mul8x8</td>
<td>1320</td>
<td>16</td>
<td>16</td>
<td>2.33</td>
<td>6.74E-05</td>
<td>0.02</td>
</tr>
<tr>
<td>mul16x16</td>
<td>6175</td>
<td>32</td>
<td>32</td>
<td>2.25</td>
<td>1.62E-04</td>
<td>0.07</td>
</tr>
<tr>
<td>mul24x24</td>
<td>15678</td>
<td>48</td>
<td>48</td>
<td>1.68</td>
<td>1.78E-04</td>
<td>0.13</td>
</tr>
<tr>
<td>mul32x32</td>
<td>25618</td>
<td>64</td>
<td>64</td>
<td>1.92</td>
<td>5.70E-04</td>
<td>0.20</td>
</tr>
</tbody>
</table>

Table II. Although the circuits differ by 2.6× in circuit size, with the smaller circuit having 3× more output nodes, the SER value of i6 is about 3.5× larger than the SER value of c3540.

Fig. 6. Runtime versus circuit size.

Fig. 7. Histogram showing the number of nodes having a specific size value for the descriptor set for circuits i6, c499, c1355, and c1908.

benchmarks such as the MCNC-91 suite [38], the ISCAS-85 benchmarks [39], and standard multiplier circuits. We list the number of gates and input/output counts for each circuit. For benchmarks c17, mul4 × 4, and mul8 × 8, we applied the entire sample space of 2N vectors, where N is the input count. For all other benchmarks, we applied 500 000 input vectors and extracted the average SER value and runtime from those runs. From this table, we see that for circuits with less than 250 gates, the runtime is less than 0.01 s. Fig. 6 plots the runtime of our algorithm versus circuit size and demonstrates the linear complexity of the proposed approach.

Unlike circuit parameters such as area and power dissipation that are mainly a function of the circuit size, the number of outputs plays a significant role in determining the error rate of a circuit. Naturally, a larger number of outputs will increase the observability of possible transient pulses. We observed that a small circuit with a large number of outputs can have a higher error rate than a large circuit with a small number of outputs. This can be seen by comparing circuit i6 with circuit c3540 in

$$\text{SER} = \frac{\text{Number of Descriptors}}{\text{Total Number of Nodes}}$$
System-level SER estimation methods such as those in [16] and [17] assume a single average value for the SER per output bit while considering different logic circuits that constitute architectural pipelines. However, using the more accurate circuit-level SER estimation approach presented in this paper, we recognize that a simple model using average SER values for the output bits can incur a large error in SER computation. Fig. 8 plots the relative magnitudes of the SER values across the output bits of circuit $i5$. We normalize the $y$-axis such that the minimum SER value across the different output bits is equal to 1.0 and the $x$-axis corresponds to the output bit number (for the sake of clarity, we sort the SER values across the output bits). This plot shows that SER values across output bits can differ by as much as 100×. This observation is similar to the SER peaking phenomenon noted in [14] for multiplier circuits. Note that our analysis method calculates the SER value for each internal node as well as output bit separately. Such a fine-grained computation is important from the perspective of SER optimization since it allows circuit designers to target high susceptibility nodes using radiation hardening and node reengineering techniques [40], [41]. Furthermore, the large disparity in SER values among the output bits allows for flip-flop-directed optimization methods to leverage the effects of temporal masking [42].

The proposed algorithm expresses the SER value of the circuit in terms of the number of FITs. The FIT metric has proven to be an effective quantitative measure in the semiconductor industry to measure circuit reliability. The correlation between FITs and mean time between failures (MTBF) is given by the equation MTBF (in hours) = $10^9$/FIT so that the MTBF of 1000 years corresponds to approximately 114 FITs. Previously proposed algorithms such as those in [27], [40], and [43] predict the circuit SER in terms of normalized error rates given in arbitrary units. In contrast to these approaches, since the proposed algorithm provides a measure for the number of FIT, we believe that our algorithm is more suitable for use in an industrial SER estimation framework to quantify system failure distributions.

Finally, to verify the accuracy of the proposed method, we compared the SER results from our algorithm with those obtained from SPICE simulations. To perform a full comparison with SPICE for a given circuit, we first pick a sample input vector and simulate strikes node-by-node for that circuit. For about 30 discrete values of charge in the range 10–150 fC, this experiment would involve about $(30 \times \text{#Gates})$ simulations per circuit per input vector. Since the time required for such a simulation was prohibitively large, we chose a subset of circuits that span the range of sizes in the fuller benchmark set for the purpose of SPICE comparison. Table III lists the SER values of our algorithm against SPICE for a fixed input vector. We see that the error is usually within 20%, with an average error of 16.1%. Note that computation error on the order of 20% is relatively insignificant since the SER value typically varies by several orders of magnitude across different circuits on the chip.

VI. CONCLUSION

In this paper, we presented a static linear-time SER analysis algorithm. We developed parametric waveforms to represent the effect of soft error strikes on the susceptible nodes in a circuit. We used an efficient merging mechanism to prune the number of distinct waveforms to be propagated in the circuit. Experimental results show that our algorithm has linear runtime complexity in the number of nodes in the circuit and SER results are, on average, within 16.1% of SPICE simulations. In addition to predicting the presence of a transient pulse at the output, we also produce an actual SER number for any given circuit. Such a rate number is useful for the system-level designer to budget extra resources for radiation hardening.

REFERENCES


<table>
<thead>
<tr>
<th>Circuit</th>
<th>Algorithm SER (# FIT)</th>
<th>SPICE SER (# FIT)</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>i1</td>
<td>1.99E-05</td>
<td>2.31E-05</td>
<td>16.1</td>
</tr>
<tr>
<td>i2</td>
<td>1.13E-06</td>
<td>9.71E-07</td>
<td>14.1</td>
</tr>
<tr>
<td>i5</td>
<td>1.03E-04</td>
<td>1.22E-04</td>
<td>18.1</td>
</tr>
<tr>
<td>i8</td>
<td>3.45E-04</td>
<td>3.98E-04</td>
<td>15.5</td>
</tr>
<tr>
<td>c432</td>
<td>2.01E-05</td>
<td>2.42E-05</td>
<td>20.5</td>
</tr>
<tr>
<td>c880</td>
<td>4.73E-05</td>
<td>4.01E-05</td>
<td>15.3</td>
</tr>
<tr>
<td>c6288</td>
<td>3.68E-04</td>
<td>4.40E-04</td>
<td>19.6</td>
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<td>2.19E-05</td>
<td>2.49E-05</td>
<td>13.6</td>
</tr>
<tr>
<td>mul8x8</td>
<td>7.33E-05</td>
<td>8.23E-05</td>
<td>12.3</td>
</tr>
</tbody>
</table>

Average 16.1


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