Inductance: Implications and Solutions for High-Speed Digital Circuits

SE1 Inductance Extraction and Modeling

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With operating frequencies entering the multi-gigahertz range, inductance is becoming an increasingly important consideration in design and analysis of on-chip interconnects. An overview is given of the extraction and analysis issues related to on-chip inductance effects, starting with a brief overview of Maxwell’s equations.

The quasi-static assumption and its implications for analysis of VLSI interconnects are discussed. It is then shown how interconnects can be represented using partial element equivalent circuit (PEEC) models. The complexity of current flow in VLSI circuits is then examined and the PEEC-based model required to represent it is presented. The importance is shown of constructing a comprehensive model that includes substantial portions of the power and ground grid surrounding the signal net to model the distributed current return paths. The importance is shown of modeling the power grid decoupling capacitance, power grid supply pads, signal net coupling capacitance, and local power and ground connections of the driver and receiver gates.

Methods are explained for simulating the constructed model and techniques that can be used to speed-up the simulation of large PEEC models. Simplified approaches are discussed that use so-called loop inductance models, or use RL circuit formulations and are compared with more detailed PEEC models. Results show the trade-off between the accuracy and efficiency of the different methods. The applicability of each method at different stages of the design is discussed. Experimental results are based on simulations of industrial circuits, including a global clock net structure of a large multi-gigahertz processor.
Frequency Dependence

- As frequency increases:
  - \( R \) increases due to proximity and skin effect
  - \( L \) reduces due to proximity effect

\[ Z = R + j \omega L \]

- Signal response increasingly characterized by inductance...

Inductive Effects

Electromagnetic Field Equations (Maxwell)

Relation between electric field & charges (Gauss' law)
- Electric field starts and ends on charges

\[ \nabla \cdot D = \rho \]

Source free nature of magnetic field
- Magnetic field forms closed loops

\[ \nabla \times B = 0 \]

Maxwell's Equations (con't)

- Electromagnetic induction law (Faraday's law)
  - Change in magnetic field induces electric field

\[ \nabla \times E = -\frac{\partial B}{\partial t} \]

Magnetic field induced by:
- Current in conductors (Amperes' law)
- Change in electric field (Displacement current)

\[ \nabla \times H = J + \frac{\partial D}{\partial t} \]

Solving Maxwell's eqns: full-wave simulation

- Methods
  - Finite Difference Method
  - Finite Element Method (FEM)
  - Boundary Element Method (BEM)
  - Method of moments (MOM)

- Transmission line models
**Common Simplifying Assumptions**

- Electro-static assumption:
  - No current and magnetic field
  - Used for capacitance extraction
- DC assumption:
  - Fixed current
  - Electric and magnetic field are independent
  - Current changes slow magnetic induced voltage small compared with resistance drop
  - Used for RC interconnect simulations

**Quasi-static Assumption**

- Magnetic field change creates significant electric field
- Assume:
  - Displacement current is small
- Electric field change does not create significant magnetic field
  - No electromagnetic wave propagation without displacement current
  - Interaction between pairs of elements becomes instantaneous (no retardation)
  - Valid if:
    - Displacement current is small compared to current density \( J \) (sufficiently low frequency)
    - Characteristic size is smaller than wavelength (10GHz wavelength is 30nm)

**Inductance Definition Using Flux**

- Traditional definition of inductance in terms of magnetic flux:
  \[ \Phi_j = \int B \cdot dl \]
- Inductance \( M \) is ratio of flux \( \Phi_j \) over current in loop \( j \)
  \[ \Phi_j = M_j I_j \]
- Flux definition not well suited for on-chip interconnects:
  - System consists of many intersecting loops (no individual loops evident)
  - Wire thickness significant compared to loop area (area integral not easily defined)

**Partial Inductance**

- Each wire segment is assigned partial self and mutual inductance
  - Split wires into segments
  - Partial inductance \( M \) between wire segments \( i \) reflects voltage induced in \( i \) due to current in \( j \)
- Analytical solution for partial inductance for parallel filaments with uniform current distribution:
  \[ M_i = \frac{N_i}{N} \int_{V} B \cdot dl \]
**PEEC Model Approach - Issues**

- **Fully-dense L matrix**
  - Computation of all mutual inductances is expensive
  - Large simulation time $\Rightarrow$ needs acceleration

**Sparsification - Implicit**

- Fast Multipole (FastHenry)  
  [Kamon IEEE-MIT '94]
  - Lump the effect of a bunch of distant conductors into a single mutual inductance

**Sparsification Issue**

- Simply dropping small entries from the Partial Inductance Matrix, can lead to a non-positive definite matrix.

**Sparsification - Explicit**

- Block diagonal sparsification  
  [Gala DAC '00]
  - Guaranteed passive
  - Loss of accuracy

- Shift-and-truncate  
  [Krauter ICCAD '95]
  - Remove couplings between wires with large separation
  - Better accuracy, guaranteed passive

**Acceleration - PRIMA**

- Passive Reduced-Order Interconnect Macromodeling Algorithm
  - [Odabasioglu - ICCAD '97]
  - Guaranteed passivity of reduced order model

1. Define ports

2. Compute multi-port reduced order model for the linear (RLC) circuit
Acceleration - PRIMA

- Passive Reduced-Order Interconnect Macromodeling Algorithm
  - [Odabasioglu - ICCAD '97]
  - Guaranteed passivity of reduced order model

3. Combine with non-linear devices, power supply

4. Simulate the reduced system in SPICE

Loop Inductance Approach

Use RL PEEC model and solve in frequency domain:

Step 1: Define grid, signal topology

Step 2: Define port at the driver end and short the receiver end of the signal.

Step 3: Compute loop impedance

Step 4: Construct a lumped circuit model using the loop resistance and inductance with interconnect and load capacitance.

Can be extended to a distributed model
On-chip inductance is important for higher frequencies. Longer wires can cause additional complications, and the return paths are frequency-dependent, making modeling complex. Detailed models using PEEC can be slow due to run-time issues, hence the need for sparsification and acceleration. Loop inductance models are fast but may suffer from accuracy issues, which is why specific topologies are used.

### PEEC vs. Loop Inductance

#### Clock Net 1

<table>
<thead>
<tr>
<th>ELEMENTS</th>
<th>DELAY (US)</th>
<th>SKEW (US)</th>
<th>RUN-TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$R$ $C$ $L$ $M$</td>
<td>PREC</td>
<td>$131p$</td>
</tr>
<tr>
<td>RC</td>
<td>3k 6k - -</td>
<td>$560p$ (-4.5us)</td>
<td>$5p$ (-10ps)</td>
</tr>
<tr>
<td>LOOP</td>
<td>3k 6k 2k -</td>
<td>1.1us (1.1us)</td>
<td>1.2ns (-1ns)</td>
</tr>
</tbody>
</table>

#### Clock Net 2

<table>
<thead>
<tr>
<th>ELEMENTS</th>
<th>DELAY (US)</th>
<th>RUN-TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$R$ $C$ $L$ $M$</td>
<td>PREC</td>
</tr>
<tr>
<td>RC</td>
<td>34k 72k 34k 40k</td>
<td>4.4us (-4.4us)</td>
</tr>
<tr>
<td>LOOP</td>
<td>480 800 400</td>
<td>660ps (-660ps)</td>
</tr>
</tbody>
</table>

### Summary
- On-chip inductance is important
- Higher frequencies
- Longer wires
- Modeling of inductance is difficult
- Return paths complicated, frequency dependent
- Detailed model using PEEC
  - Complex
  - Run-time issues => Sparsification/Acceleration
- Simplified models using loop inductance
  - Fast
  - Accuracy issues => Use for specific topologies

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