

CURRICULUM VITAE

David T. Blaauw

December 2016

I Personal Data

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II Employment History

A. Education

Doctor of Philosophy in Computer Science, University of Illinois, Urbana-Champaign, January 1992.
Thesis: “Functional Abstraction in Switch-Level Simulation.”
Advisor: Professor Jacob A. Abraham

Master of Science in Computer Science, University of Illinois, Urbana-Champaign, May 1989.
Thesis: “Automatic Generation of Behavioral Models.”
Advisor: Professor Jacob A. Abraham

Bachelor of Science in Physics with a second major in Computer Science, Duke University, May 1986.

B. Present Position

Professor of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.

C. Employment History

- September 2007 - Present: Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan
- August 2001 - September 2007: Associate Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan.
- September 1994 - August 2001: Engineering Manager, Advanced Design Technology, Motorola, Inc., Austin, Texas.
- August 1993 - September 1994: Staff engineer, Semiconductor Systems Design Technology Group, Motorola, Inc., Austin, Texas.
- August 1992 - August 1993: Development Staff Member, IBM Corporation, Endicott, New York.

D. Honors and Awards

- 2016 SIA-SRC University Researcher Award, established by the semiconductor industry association to recognize lifetime research contributions to the U.S. semiconductor industry by university faculty.
- 2016 IEEE Micro Top Picks special issue "MBus: The Missing Interconnect that Enables the Modular Millimeter-Scale Computing Class and Connects the World's Smallest Computer,"
- Best Paper Award, "Racetrack Converter: A Low Power and Compact Data Converter Using Racetrack Spintronic Devices," IEEE International Symposium on Circuits and Systems (ISCAS), May 2015
- 2014 John von Neumann Student Research Award for Excellence in Systems Research – SONIC Annual Review Meeting
- Recognized as top 50 innovator over the last 50 years graduating from the University of Illinois EECS department in 2014
- College of Engineering Innovation Excellence Award for 2013-2014
- Design Automation Conference (DAC) 50th Anniversary award for being the top 10 most cited DAC authors in DAC's 50 year history, June 2013
- Design Automation Conference (DAC) 50th Anniversary award for publishing the most papers in the fifth decade of DAC's history, June 2013
- 2013 University of Michigan Electrical Engineering and Computer Science (EECS) Department Outstanding Achievement Award for innovative research in variation-tolerant and energy efficient integrated circuit design, and exceptional mentoring and teaching in the area of VLSI circuits
- International Solid-State Circuits Conference (ISSCC) 60th Anniversary Special Recognition top 10 contributing author over the last 10 years, February 2013
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD) Ten Year Retrospective Most Influential Paper Award, "Combined Dynamic Voltage Scaling and Adaptive Body biasing for Lower Power Microprocessors under Dynamic Workloads," ICCAD 2002 Conference, November 2012
- Second Prize in the 18th Samsung Human-Tech Thesis Competition for research on millimeter sensor design, February 2012
- IEEE Fellow status, January 2012

- Winner MuSyC Research Consortium annual best poster award, “A Modular 1mm³ Die-Stacked Sensing Platform,” Nov 2011
- Winner 11th International VLSI-Symposium Low Power Design Contest, “SWIFT: A 2.1 Tb/s 32x32 Self-Arbitrating Manycore Interconnect Fabric,” IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011
- Winner Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC) Design contest, “Design and Implementation of Centip3De, a 7-layer Many-Core System,” Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC), Feb/June 2011
- Best Paper Award, “Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs),” ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2009
- 2008 Ted Kennedy Family Team Excellence Award (award shared with Todd Austin, Scott Mahlke, Trevor Mudge, Marios Papaefthymiou). The Ted Kennedy Family Team Excellence Award is an annual award given by the University of Michigan, College of Engineering that recognizes the production of an extraordinary and significant piece of work from current or recent collaboration in teaching or research to the College of Engineering.
- 2008 Richard Newton GSRC Industrial Impact Award for “development of the Razor technology” (award shared with Professor Todd Austin). The Richard Newton GSRC Industrial Impact Award is an annual award given by the GSRC DARPA/MARCO center that recognizes research that is “at least five years old and has had a significant industrial impact.”
- University of Michigan College of Engineering Research Excellence Award for 2007-2008, January 2008
- Best Paper Nomination, “Energy Efficient Near-threshold Chip Multi-processing,” ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2007
- Best Paper Nomination, “Self-timed Regenerators for High-speed and Low-power Interconnect,” ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2007
- Microprocessor Review Analysts’ Choice Award in Innovation for “Introducing Speculation on Correctness as a Method for Allowing Circuit Operation Beyond Worst-Case Design,” Microprocessor Review, February 2007
- 2004 IEEE Micro Top Picks special issue on the most industry relevant and significant papers of the year in computer architecture, “Razor: Circuit-Level Correction of Timing Errors for Low-Power Operation”
- University of Michigan Henry Russel Award for “Exceptional Scholarship and Conspicuous Ability as a Teacher,” November 2004
- Best Paper Nomination, “Parametric Yield Estimation Considering Leakage Variability,” ACM/IEEE Design Automation Conference (DAC), June 2004
- Best Paper Award, “Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation,” ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2003
- Best Regular Paper Award, “Noise Analysis Methodology for Partially Depleted SOI Circuits,” IEEE Custom Integrated Circuits Conference (CICC), September 2003
- IBM Faculty Award, IBM Center for Advanced Studies, June 2003
- Best Paper Award, “Statistical Delay Computation Considering Spatial Correlations,” ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2003

- IBM Faculty Award, IBM Center for Advanced Studies, June 2002
- Best Paper Nomination, “Pre-route Noise Estimation in Deep Submicron Integrated Circuits,” ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2002
- Best Paper Nomination, “Driver Modeling and Alignment for Worst-Case Delay Noise,” ACM/IEEE Design Automation Conference (DAC), June 2001
- Best Paper Award, “On-Chip Inductance Modeling and Analysis,” ACM/IEEE Design Automation Conference (DAC), June 2000
- Motorola Innovation Award, 1997
- Motorola High Impact Technology Award, 1996

III Research Experience

A. Research Interests

My research interests focus on high-performance and low-power VLSI circuits, particularly addressing nano-meter design issues pertaining to power, performance and robustness. My aim is to develop novel circuit design techniques for effective VLSI design in the nano-meter era, in conjunction with efficient and accurate analysis and optimization methods for large, multi-million transistor designs.

B. Doctoral Students Supervised

| <u>Student</u> | <u>Thesis Title/Topic</u> | <u>Graduation Date</u> |
|--------------------|--|------------------------|
| Ziyun Li | | In Progress |
| Yu Zeng | | In Progress |
| Dongkwun Kim | | In Progress |
| Li-Xuan Chuo | | In Progress |
| Xiao Wu | | In Progress |
| Wootae Lim | | In Progress |
| Yao Shi | | In Progress |
| Taekwang Jang | | In Progress |
| Wanyeong Jung | | In Progress |
| Supreet Jeloka | | In Progress |
| Yejoong Kim | Robust Circuit Design for Low-Voltage VLSI | May 2015 |
| Nathaniel Pinckney | Near-Threshold design | In Progress |
| Dongmin Yoon | Low power timer references | In Progress |
| Inhee Lee | Power management for ultra-low power sensors systems | October 2014 |
| Gyouho Kim | Ultra-low power visual monitoring | August 2014 |

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|-----------------------|---|---------------|
| Bharan Giridhar | Adaptive Computing | December 2013 |
| Zhi Yoong Foo | Low power processor design techniques | August 2013 |
| Sudhir Satpathy | Fast and low power inconnect fabrics | Dec 2012 |
| David Fick | Adaptive Low-power design | August 2012 |
| Yoonmyung Lee | Ultra Low-Power Memory Design | April 2012 |
| Prashant Singh | Reliability analysis and wear-out detection | April 2010 |
| Nurrachman Liu | Automatic tuning of VLSI circuits | April 2010 |
| Brian Cline | Process variation modeling for advance semiconductor circuits | Feb 2010 |
| Cheng Zhuo | VLSI wearout modeling | Dec 2010 |
| Ravikishore Gandikota | Crosstalk-Noise analysis for nanometer VLSI circuits | Aug 2009 |
| Carlos Tokunaga | Circuits and architectures for secure processing | Sep 2008 |
| Shidhartha Das | Razor: circuit speculation for power and performance efficient design | Oct 2008 |
| Kaviraj Chopra | Statistical timing analysis including spatial correlations | Apr 2008 |
| Eric Karl | Reliable computing on unpredictable silicon | Mar 2008 |
| Sanjay Pant | Power grid analysis and design | Dec 2007 |
| Mini Nanua | Leakage and noise analysis in nano-scale technologies | Apr 2007 |
| Bo Zhai | Dynamic voltage scaling for embedded processor designs | Mar 2007 |
| Rajeev Rao | Modeling and design of low-power VLSI systems under for multiple sources of uncertainty | Jul 2006 |
| Dongwoo Lee | Analysis and minimization of leakage current | May 2005 |

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| Aseem Agarwal | Statistical timing analysis for VLSI circuits | Mar 2005 |
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C. Masters Students Supervised

| <u>Student</u> | <u>Thesis Title/Topic</u> | <u>Graduation Date</u> |
|-------------------|---|------------------------|
| Skyler Skrzyniarz | Low Power Correlation Architectures for GPS | June 2015 |
| Junhua Gu | Low Power Circuits for Analog to digital interfaces | May 2015 |
| Ruochen Xie | Energy Reduction of FeRAM Memories for Millimeter Sensors | May 2015 |
| Allen Wang | Low Power Level Conversion | May 2014 |
| Naveen Akesh | Low Power Audio Device for Developing World | May 2014 |
| Zhe Yu | RF Communication for Millimeter Scale Sensors | May 2014 |
| Hsi-Shou Wu | Low Power Word-Spotting | April 2014 |
| Siddharth Saxena | Low power correlation circuits | May 2013 |
| Karan Jain | Low power synchronization using ambient RF signals | April 2012 |
| Jordan LeNoach | pH sensor for millimeter sensors | Dec 2011 |
| Jeffrey Yeh | Chip design for the developing world | April 2011 |
| Nate Robert | Low power LDO | Dec 2010 |

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| Vikas Vinay | Low power Class-D amplifier for developing world applications | Dec 2010 |
| Abhishek Madhavan | Low power chip design | Dec 2010 |
| Junsun Park | Intra-cellular chip design | May 2010 |
| Jou-ching (George) Sung | Low power ADC design | August 2009 |
| Mao-Ter Chen | Low power sensor node design | Dec 2008 |
| Sudharsen Kalaiselvan | Razor-3: A circuit speculation and SEU tolerant circuit technique | May 2007 |
| Deepesh John | Low power design through typical-case optimization | May 2006 |
| Yueh-Chuan Tzeng | Encryption processor for side channel attack avoidance | May 2006 |
| Meghna Singhal | Low power design using subthreshold operation | May 2006 |
| Amir Borna | Analysis of lithographic variations for chip performance | Aug 2005 |
| Amit Jain | Delay modeling for non-ramp input transitions | Nov 2004 |
| Toan Pham | Clock skew reduction using Razor flip-flops | Dec 2003 |
| Bhavana Thudi | Non-iterative switching window computation for delay noise | May 2003 |
| Wesley Kwong | Efficient circuit-level analysis of gate-oxide tunneling current in VLSI designs | May 2003 |

D. Research Grants

- DSTL/MoD, “Architectural Design Study for M3 MM Scale Computing GPS Logger,” \$400,000 with 175,000 to PI David Blaauw, 8/15/2013-3/14/2014
- NSF, “SHF: Small: Minimally Invasive Error Detection/Correction for Runtime Margin Elimination,” \$450,000 with \$252,750 to PI: David Blaauw, 7/2012-6/2015

- BAE Systems/United States Army, “Center for Objective Microelectronics and Biomimetic Adaptive Technology (COM-BAT),” \$400,000 with \$135,000 to Co-PI David Blaauw, PI:Kamal Sarabandi, Co-PI: David Blaauw, 9/2013 – 8/2016
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$5,000,000 total, with approx. \$1,600,000 to Co-PI David Blaauw, PI: Trevor Mudge, 5/2010 - 5/2015
- Advanced Energy Consortium, “An Autonomous Microsystem Test-Bed for Extreme Environments: Integrating Sensor Elements, Electronics, and Packaging,” \$950,000 with \$226,625 to Co-PI David Blaauw, PI: Yogesh Gianchandani , 6/2012-12/2014
- Semiconductor Research Corporation (SRC), “Fast Power Supply Boosting for Energy-Efficient, High-Performance Processors,” \$360,000 total with \$180,000 to PI David Blaauw, 8/2012 - 7/2015
- DARPA, “Systems on Nanoscale Information Fabrics (SONIC) Center,” \$7,008,335, PI: Naresh Shanbhag with \$1,401,667 to Co-PI David Blaauw, 1/2013-10/2017
- DARPA, “The TerraSwarm Research Center,” \$6,887,500, with \$ 1,100,000 to Co-PI David Blaauw, PI: Edward Lee, 1/2013-10/2017
- DSTL, “MM scale computing for GPS logger,” \$400,000, with \$175,000 to PI: David Blaauw
- Isocline Engineering LLC, “Power Efficient Software Define Radio (SDR) Mobile Architecture Technology for Handheld Devices,” \$220,093 to PI: David Blaauw
- Isocline Engineering LLC, “ Programmable Microchip for Accelerating Neuromorphic Object Recognition,” \$45,715 to PI: David Blaauw
- QUALCOMM, “Near Threshold Computing,” \$100,000, gift, 8/2011-8/2013
- Oracle, “High Performance Razor Architecture ” \$80,000, gift, 8/2013-8/2014
- AMD, “*In Situ* Wearout Detection and Mitigation,” \$100,000, gift, with \$50,000 to David Blaauw, 11/2011
- Food and Drug Administration, “Smart Rapid Palatal Expander for Pediatric Cleft and Palate Patients,” \$312,000 total with \$136,000 to Blaauw, PI: Jeanne Nervina, University of Michigan, 9/2011- 8/2013
- National Science Foundation (NSF), “Integrating Circuits, Sensing, and Software to Realize the Cubic-mm Computing Class,” \$2,533,000 total with \$519,265 to Blaauw, PI: David Wentzloff, University of Michigan, 08/2011 - 7/2016
- Qualcomm, “Near-Threshold Computing,” \$50,000, gift, PI: David Blaauw, University of Michigan, 05/2011
- Department of Energy, “Hardware-Software Co-Design for Non-Volatile Memory in Exascale Systems,” \$525,000 total with \$202,747 to Blaauw, PI: Trevor Mudge, University of Michigan, 01/2011 - 12/2013
- Intel Corporation, “A Confidence-Driven Model for Predictable Computing in Future Technologies,” \$249,000 total with \$65,916 to Blaauw, PI: Prof. Zhengya Zhang, Co-PIs: Prof. David Blaauw, and Prof. Dennis Sylvester, University of Michigan, 01/2010 - 10/2010
- QUALCOMM, “Adaptive Design Solutions for VLSI Circuits,” \$50,000, gift, 09/01/09
- National Science Foundation (NSF), “Reclaiming Moore’s Law through Ultra Energy Efficient Computing,” \$2,778,507 total with \$643,700 to Blaauw, PI: Prof. David Blaauw, Co-PIs: Prof. Trevor Mudge, Prof. Dennis Sylvester, University of Michigan, Prof. Chaitali Chakrabarti, Arizona State University, Prof. David Money Harris, Harvey Mudd University, 09/2009 - 08/2014
- National Science Foundation (NSF), “Probabilistic Wearout in Nanoscale,” \$300,000 with \$150,000 to Blaauw, PI: Dennis Sylvester, Co-PI: David Blaauw, 08/2008 - 07/2011

- IBM Corporation/Defense Advanced Research Projects Agency (DARPA), “Strained Si/SiGe/Ge Heterojunction Tunneling Transistor (HETT) e with Steep Subthreshold Slope for Extremely Low Power Electronics,” \$17,971,252 with \$600,000 to Blaauw, PI: Steve Koester, Co-PI: David Blaauw, 01/2008 - 12/2009
- BAE Systems/United States Army, “Center for Objective Microelectronics and Biomimetic Adaptive Technology (COM-BAT),” \$8,962,200 with \$700,000 to Blaauw, PI: Kamal Sarabandi, Co-PI: David Blaauw, 5/2008 - 5/2013
- Intel Corporation, “Adaptive Digital Design in the Nanometer Regime,” \$100,000, gift, 3/2008 - 3/2010
- Sun Microsystems, “Robust Low Voltage SRAM Design,” \$150,000, gift, 9/2007 - 9/2010
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design,” \$40,000, gift, 7/2007
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), “Elastic: An Adaptive Self-Healing Architecture for Unpredictable Silicon,” \$600,000 total, PI: David Blaauw, 9/2006 - 9/2009
- Semiconductor Research Corporation (SRC), “A Design Optimization Framework for Process Variation Tolerance,” \$390,000 total with \$195,000 to Blaauw, PI: Dennis Sylvester, Co-PI: David Blaauw, University of Michigan, 9/2006 - 8/2009
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design” \$40,000, gift, 7/2006
- Semiconductor Research Corporation (SRC), “CAD Solutions for Parametric Yield Optimization,” \$321,000 total with \$160,000 to Blaauw, PI Dennis Sylvester, Co-PI: David Blaauw, University of Michigan, 9/2005 - 7/2008
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design” \$40,000, gift, 7/2005
- NSF Engineering Research Center (ERC) for Wireless Integrated Micro Systems (WIMS), “Subthreshold Processor Design,” PI: Kenneth Wise, University of Michigan, \$60,000 to Blaauw, 5/2005 - 5/2010
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$5,000,000 total, with approx. \$1,600,000 to Blaauw, PI: Trevor Mudge, University of Michigan, Co-PIs: David Blaauw, Scott Mahlke, University of Michigan, 5/2005 - 5/2010
- Semiconductor Research Corporation (SRC), “Optimization of Lithographic Induced Variability for Improved Circuit Performance,” \$161,029, PI: David Blaauw, 9/2004 - 8/2007
- Intel Corporation, “Power Grid Integrity Analysis,” \$50,000, gift, 7/2004
- Photronics, Inc. \$75,000, gift, 6/2004 - 5/2005
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$240,000 total with \$60,000 to Blaauw, PI: Trevor Mudge, University of Michigan, Co-PIs: David Blaauw, Scott Mahlke and Todd Austin, University of Michigan, 5/2004 - 5/2005
- National Science Foundation (NSF), Information Technology Research (ITR), “Collaborative Research ITR: Mobile Supercomputing,” \$1,900,000 total with \$320,603 to Blaauw, PI: Prof. Trevor Mudge, Co-PIs: Prof. David Blaauw, Prof. Todd Austin, Prof. Scott Mahlke, University of Michigan, Prof. Wayne Wolf, Princeton University, Prof. Chaitali Chakrabarti, Arizona State University, 11/2003 - 11/2007

- Intel Corporation, “VLSI Design Curriculum,” \$247,292 total with \$61,823 to Blaauw, PI: Richard Brown, Co-PIs: Prof. David Blaauw, Prof. Michael Flynn, and Prof. Dennis Sylvester, University of Michigan, 10/2003 - 10/2004
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), “Power Aware Systems,” \$600,000 total, PI: David Blaauw, 9/2003 - 9/2006
- IBM Corporation, Center for Advanced Studies, “Static Performance Analysis under Process and Environment Variations,” \$40,000, Faculty Award, 9/2003
- Intel Corporation, “Power Grid Integrity Analysis,” \$50,000, gift, 7/2003
- Semiconductor Research Corporation (SRC), “Analysis and Reduction of Simultaneous Gate-Oxide Tunneling and Subthreshold Leakage Current,” \$360,000 total with \$160,000 to Blaauw, PI: David Blaauw, Co-PI: Dennis Sylvester, University of Michigan, 7/2003 - 7/2006
- National Science Foundation (NSF), “Performance Analysis and Optimization for Nanometer Design,” \$375,000, PI: David Blaauw, 6/2003 - 6/2006
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$240,000 total with \$60,000 to Blaauw, PI: Trevor Mudge, University of Michigan, Co-PIs: David Blaauw and Scott Mahlke, University of Michigan, 5/2003 - 5/2004
- IBM Corporation, Center for Advanced Studies, “Leakage Characterization and Analysis,” \$40,000, Faculty Award, 9/2002
- National Science Foundation (NSF), Information Technology Research (ITR), “Methodologies for Robust Design of Information Systems under Multiple Sources of Uncertainty”, \$1,800,00 total with \$450,000 to Blaauw, PI: David Blaauw, Co-PIs: Prof. Dennis Sylvester, University of Michigan, Prof. Sachin Sapatnekar, University of Minnesota, Prof. Sarma Vrudhula, University of Arizona, 8/2002 - 8/2006
- Intel Corporation, “Power Grid Integrity Analysis,” \$50,000, gift, 7/2002
- MARCO/DARPA - Giga-Scale Research Center (GSRC), “Power Management for Nanometer design,” \$197,000, PI: David Blaauw, 10/2001 - 8/2003
- Semiconductor Research Corporation (SRC), “Variability in Chip-Level Performance and Signal Integrity Verification,” \$257,000, PI: David Blaauw, 10/2001 - 10/2004

IV Teaching Experience

| <u>Semester</u> | <u>Class</u> | <u>Course Number</u> | <u>Size</u> | <u>Rating (out of 5) Course/Instructor</u> |
|-----------------|-------------------------------------|----------------------|-------------|--|
| Fall 2016 | VLSI Design I | EECS 427 | | |
| Fall 2015 | Digital Integrated Circuits | EECS 312 | 35 | 4.58/4.81 |
| Fall 2014 | Advanced VLSI Design II | EECS 628 | 26 | 4.86/4.90 |
| Winter 2014 | Advanced VLSI Design | EECS 627 | 38 | 4.77/4.77 |
| Fall 2013 | VLSI Design I | EECS 427 | 39 | 4.74/4.78 |
| Winter 2013 | Introduction to Electronic Circuits | EECS 215 | 120 | 3.56/4.09 |
| Winter 2012 | Advanced VLSI Design | EECS 627 | 37 | 4.87/4.87 |
| Fall 2011 | VLSI Design I (Section 2) | EECS 427 | 18 | 4.79/4.79 |
| Fall 2011 | VLSI Design I (Section 1) | EECS 427 | 35 | 4.83/4.83 |
| Winter 2011 | Advanced VLSI Design | EECS 427 | 9 | 4.88/4.88 |
| Fall 2010 | Advanced VLSI Design II | EECS 628 | 19 | 4.81/5.00 |
| Winter 2010 | Advanced VLSI Design | EECS 627 | 19 | 4.85/4.96 |
| Winter 2009 | Advanced VLSI Design | EECS 627 | 23 | 4.75/4.75 |
| Fall 2008 | VLSI Design I | EECS 427 | 28 | 4.67/4.56 |
| Winter 2007 | Advanced VLSI Design | EECS 627 | 20 | 4.79 |
| Fall 2006 | VLSI Design I | EECS 427 | 31 | 4.89 |
| Winter 2006 | Advanced VLSI Design | EECS 627 | 22 | 4.55 |
| Fall 2005 | Topics in VLSI Design | EECS 598 | 12 | 4.25 |
| Winter 2005 | Advanced VLSI Design | EECS 627 | 20 | 4.79 |
| Winter 2004 | Advanced VLSI Design | EECS 627 | 35 | 4.59 |
| Fall 2003 | Introduction to Logic Design | EECS 270 | 87 | 4.77 |
| Winter 2003 | Advanced VLSI Design | EECS 627 | 36 | 4.61 |

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| Fall 2002 | Introduction to Logic Design | EECS 270 | 109 | 4.77 |
| Winter 2002 | Advanced VLSI Design | EECS 627 | 40 | 4.31 |
| Fall 2001 | Issues in High-Performance Deep-Submicron Design | EECS 598 | 11 | 4.75 |

V Publications

A. Books

1. Ashish Srivastava, Dennis Sylvester and David Blaauw, *Statistical Analysis and Optimization for VLSI: Timing and Power*, Kluwer Academic Publishers, 2005

B. Book Chapters

1. Sechang Oh, Wanyeong Jung, Hyunsoo Ha, Jae-Yoon Sim, David Blaauw, “Energy-Efficient CDCs for Millimeter Sensor Nodes,” Chapter in *Advances in Analog Circuit Design*, Kofi Makinwa, Andrea Baschirott, and Pieter Harpe, editors, Springer Publishing Company, 2015
2. Shidhartha Das, David Roberts, David Blaauw, David Bull, Trevor Mudge, “Architectural Techniques for Adaptive Computing,” Chapter in *Adaptive Techniques for Dynamic Processor Optimization: Theory and Practice*, Alice Wang and Sam Naffziger, editors, Springer Publishing Company, 2008
3. David Blaauw, Sanjay Pant, Rajat Chaudhry and Rajendran Panda, “Design and Analysis of Power Supply Networks,” Chapter in *Electronic Design Automation for Integrated Circuits Handbook*, Louise Sheffer, Luciano Lavagno and Grant Martin, editors, CRC Press, 2005
4. Sarvesh Kulkarni, Ashish Srivastava, Dennis Sylvester, David Blaauw, “Power Optimization Techniques using Multiple Supply Voltages,” Chapter in *Closing the Power Gap between ASIC and Custom*, David Chinnery and Kurt Keutzer, editors, Kluwer Academic Publishers, 2005
5. Dongwoo Lee, Bo Zhai, David Blaauw, Dennis Sylvester, “Static Leakage Reduction through Simultaneous $V_{T_{ox}}$ and State Assignment,” Chapter in *Ultra Low-Power Electronics and Design*, Enrico Macii, editor, Kluwer Academic Publishers, 2004
6. David Blaauw, Abhijit Dharchoudhury, Rajendran Panda, “Design and Analysis of Power Distribution Networks for Processor Design,” Chapter in *IEEE Design of High Performance Microprocessors Circuits*, Anantha Chandrakasan, William Bowhill, and Frank Fox, editors, IEEE Press, 2000
7. Abhijit Dharchoudhury, Shantanu Ganguly, David Blaauw, “Timing and Signal Integrity Analysis,” Chapter in *Handbook for VLSI Design*, Wai Kai Chen, editor, IEEE Press, 2000

C. Invited Articles

1. Taekwang Jang, Myungjoon Choi, Yao Shi, Inhee Lee, Dennis Sylvester and David Blaauw, “Millimeter-Scale Computing Platform for Next Generation of Internet of Things,” IEEE International Conference on RFID (RFID), May 2016
2. Taekwang Jang, Seokhyeon Jeong, Myungjoon Choi, Wanyeong Jung, Gyouho Kim, Yen-Po Chen, Yejoong Kim, Wootae Lim, Dennis Sylvester, David Blaauw, “Key Building Blocks and Integration Strategy of a Miniaturized Wireless Sensor Node,” IEEE European Solid-State Circuits Conference (ESSCIRC), September 2015
3. Nathaniel Pinckney, David Blaauw, Dennis Sylvester, “Low Power Near-Threshold Design,” IEEE Solid-State Circuits Magazine, June 2015
4. Inhee Lee, Yejoong Kim, Suyoung Bang, Gyouho Kim, Hyunsoo Ha, Yen-Po Chen, Dongsuk Jeon, Seokhyun Jeong, Wanyeong Jung, Mohammad Hassan Ghaed, Zhiyoong Foo, Yoonmyung Lee, Jae-Yoon Sim, Dennis Sylvester, and David Blaauw, “Circuit Techniques for Miniaturized Bio-medical Sensors,” IEEE Custom Integrated Circuits Conference (CICC), September 2014
5. David Blaauw, Dennis Sylvester, Prabal Dutta, Yoonmyung Lee, Inhee Lee, Sechang Bang, Yejoong Kim, Gyouho Kim, Pat Pannuto, Ye-Shang Kuo, Dongmin Yoon, Wanyeong Jung,

- ZhiYoong Foo, Yen-Po Chen, Seok Hyeon Jeong, Myungjoon Choi, "IoT Design Space Challenges: Circuits and Systems" 2014 IEEE Symposium on VLSI Technology, June 2014
6. Yoonmyung Lee, Dennis Sylvester, David Blaauw, "Circuits for Ultra-Low Power Millimeter-Scale Sensor Nodes," 2012 Asilomar Conference on Signals, Systems and Computers (Asilomar), November 2012
 7. David Blaauw, Dennis Sylvester, Yoonmyung Lee, Inhee Lee, Suyoung Bang, Yejoong Kim, Gyouho Kim, Hassan Ghaed, "From Digital Processors to Analog Building Blocks: Enabling New Applications through Ultra-Low Voltage Design," Invited paper to the IEEE Subthreshold Microelectronics Conference (SubVt), Plenary Keynote, October 2012
 8. Nathaniel Pinckney, Korey Sewell, Ronald Dreslinski, Dave Fick, David Blaauw, Dennis Sylvester, Trevor Mudge, "Assessing the Performance of Parallelized Near-Threshold Computing," ACM/IEEE Design Automation Conference (DAC), June 2012
 9. Yoonmyung Lee, YeJoong Kim, Dongmin Yoon, David Blaauw, Dennis Sylvester, "Circuit and System Design Guidelines for Ultra-Low Power Sensor Nodes," ACM/IEEE Design Automation conference (DAC), June 2012
 10. Yoonmyung Lee, Dennis Sylvester, David Blaauw, "Synchronization of Ultra-Low Power Wireless Sensor Nodes", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2011
 11. Gregory Chen, Scott Hanson, David Blaauw, Dennis Sylvester, "Circuit Design Advances for Wireless Sensing Applications," Proceedings of the IEEE, Special Issue on Wireless Sensor Networks, Vol. 98, No. 11, November 2010, pg. 1808 - 1827
 12. Prashant Singh, Dennis Sylvester, David Blaauw, "Adaptive Sensing and Design for Reliability," IEEE International Reliability Physics Symposium, May 2010
 13. Ronald G. Dreslinski, Michael Wieckowski, David Blaauw, Dennis Sylvester, Trevor Mudge, "Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits," Proceedings of the IEEE, Special Issue on Ultra-Low Power Circuit Technology, Vol. 98, No. 2, February 2010, pg. 253 - 266
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54. Myungjoon Choi, Inhee Lee, Tae-Kwang Jang, David Blaauw, Dennis Sylvester "A 23pW, 780ppm/°C Resistor-less Current Reference Using Subthreshold MOSFETs," (ESSCIRC) September 2014
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61. Supriya Rao, Reetuparna Das, Supreet Jeloka, David Blaauw, Ronald G. Dreslinski, Trevor Mudge, "VIX: Virtual Input Crossbars for Efficient Switch Allocation," ACM/IEEE Design Automation Conference (DAC), June 2014
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74. Seokheon Jeong, Jae-yoon Sim, David Blaauw, Dennis Sylvester, "65nW CMOS Temperature Sensor for Ultra-Low Power Microsystems," IEEE Custom Integrated Circuits Conference (CICC), September 2013
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81. Dong-Woo Jee, Dennis Sylvester, David Blaauw, Jae-Yoon Sim, "A 0.45V, 423 nW, 3.2 MHz Multiplying DLL with Leakage-Based Oscillator for Ultra-Low-Power Sensor Platforms," IEEE International Solid-State Circuits Conference (ISSCC), February 2013
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90. Ronald Dreslinski, David Fick, Bharan Giridhar, Gyouho Kim, Sangwon Seo, Matthew Fojtik, Sudhir Satpathy, Yoonmyung Lee, Daeyeon Kim, Nurrachman Liu, Michael Wiecekowski, Gregory Chen, Trevor Mudge, Dennis Sylvester, David Blaauw, "Centip3De: A 64-Core, 3D Stacked, Near-Threshold System", HotChips-24, August 2012
91. Ronald Dreslinski, Korey Sewell, Thomas Manville, Sudhir Satpathy, Nathaniel Pinckney, Geoff Blake, Michael Cieslak, Reetuparna Das, Thomas Wensch, Dennis Sylvester, David Blaauw, Trevor Mudge, "Swizzle Switch: A Self-Arbitrating High-Radix Crossbar for NoC Systems," HotChips-24, August 2012
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93. Sudhir Satpathy, Dennis Sylvester, David Blaauw, "A Standard Cell Compatible Bidirectional Repeater with Thyristor Assist," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2012
94. Yen-Po Chen, Matt Fijtk, David Blaauw, Dennis Sylvester, "A 2.98nW Bandgap Voltage Reference Using a Self-Tuning Low Leakage Sample and Hold," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2012
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100. Sudhir Satpathy, Korey Sewell, Thomas Manville, Yen-Po Chen, Ronald Dreslinski, Dennis Sylvester, Trevor Mudge, David Blaauw, "A 4.5Tb/s 3.4Tb/sW 64 x 64 Switch Fabric With Self-Updating Least-Recently-Granted Priority and Quality-of-Service Arbitration in 45nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), February 2012
101. Yoonmyung Lee, Gyouho Kim, Suyoung Bang, Yejoong Kim, Inhee Lee, Prababl Dutta, Dennis Sylvester, David Blaauw, "A Modular 1mm³ Die-Stacked Sensing Platform with Optical Communication and Multi-Modal Energy Harvesting," IEEE International Solid-State Circuits Conference (ISSCC) *Invited Paper* to the IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC, February 2012
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112. Nurrachman Liu, Nathaniel Pinckney, Scott Hanson, Dennis Sylvester, David Blaauw, "A True Random Number Generator using Time-Dependent Dielectric Breakdown," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011
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117. Mark Woh, Sudhir Satpathy, Ronald G. Dreslinski, Daniel Kershaw, Dennis Sylvester, David Blaauw, Trevor Mudge, "Low Power Interconnects for SIMD Computers," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2011
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119. Gregory Chen, Hassan Ghaed, Razi-Ul Haque, Michael Wieckowski, Yejoong Kim, Gyouho Kim, David Fick, Daeyeon Kim, Mingoo Seok, Kensall Wise, David Blaauw, Dennis Sylvester, "A 1 Cubic Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor," IEEE International Solid-State Circuits Conference (ISSCC), February 2011
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124. Vineeth Veetil, Dennis Sylvester, David Blaauw, "A Lower Bound Computation Method for Evaluation of Statistical Design Techniques," ICCAD 2010, November 2010
125. Vivek Joshi, Kanak Agarwal, Dennis Sylvester, David Blaauw, "Analysis and Optimization of SRAM Robustness for Double Patterning Lithography," ICCAD 2010, November 2010
126. Cheng Zhuo, Kanak Agarwal, Dennis Sylvester, David Blaauw, "Active Learning Framework for Post-Silicon Variation Extraction and Test Cost Reduction," ICCAD 2010, November 2010
127. Prashant Singh, Eric Karl, Dennis Sylvester, David Blaauw, "Dynamic NBTI Management Using a 45nm Multi-Degradation Sensor," IEEE Custom Integrated Circuits Conference (CICC), September 2010, *Invited Paper to the Special Issue on CICC, IEEE Transactions on Circuits and Systems I: Analog and Digital Signal Processing (T-CAS)*
128. Vivek Joshi, Michael Wieckowski, Gregory Chen, David Blaauw, Dennis Sylvester, "Analyzing the Impact of Double Patterning Lithography on SRAM Variability in 45nm CMOS," IEEE Custom Integrated Circuits Conference (CICC), September 2010
129. Mingoo Seok, Gyouho Kim, David Blaauw, Dennis Sylvester, "Variability Analysis of a Digitally Trimmable Ultra-Low Power Voltage Reference," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2010
130. Greg Chen, Michael Wieckowski, David Blaauw, Dennis Sylvester, "Crosshairs SRAM - An Adaptive Memory for Mitigating Parametric Failures," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2010
131. Mingoo Seok, David Blaauw, Dennis Sylvester, "Clock Network Design for Ultra-Low Power Applications," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August, 2010
132. Nurrachman Liu, Scott Hanson, Dennis Sylvester, David Blaauw, "OxID: On-Chip One-Time Random ID Generation using Oxide Breakdown," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2010
133. Sudhir Satpathy, Zhiyoong Foo, Bharan Giridhar, Dennis Sylvester, Trevor Mudge, David Blaauw, "A 1.07 Tbit/s 128x128 Swizzle Network for SIMD Processors," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2010
134. Vineeth Veetil, Yung-Hsu Chang, Dennis Sylvester, David Blaauw, "Efficient Smart Monte Carlo based SSTA on Graphics Processing Units with Improved Resource Utilization," ACM/IEEE Design Automation Conference (DAC), June 2010
135. Vivek Joshi, "Closed-Form Modeling of Layout-Dependent Mechanical Stress," ACM/IEEE Design Automation Conference (DAC), June 2010
136. Mingoo Seok, Scott Hanson, Michael Wieckowski, Gregory K. Chen, Yu-Shiang Lin, David Blaauw, Dennis Sylvester, "Circuit Design Advances to Enable Ubiquitous Sensing Environments," IEEE International Symposium on Circuits and Systems (ISCAS), May 2010
137. Cheng Zhuo, David Blaauw, Dennis Sylvester, "Process Variation and Temperature Aware Reliability Management," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2010
138. Michael Wieckowski, Dennis Sylvester, David Blaauw, "A Black Box Method for Stability Analysis of Arbitrary SRAM Cell Structures," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2010

139. David Bull, Shidhartha Das, Karthik Shivashankar, Ganesh Dasika, Krisztian Flautner, David Blaauw, "A Power-efficient 32bit ARM ISA Processor using Timing-error Detection and Correction for Transient-error Tolerance and Adaptation to PVT Variation," IEEE International Solid-State Circuits Conference (ISSCC), February 2010, **Invited Paper to the IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC**
140. Prashant Singh, Zhiyoong Foo, Michael Wieckowski, Scott Hanson, Matt Fojtik, David Blaauw, Dennis Sylvester, "Early Detection of Oxide Breakdown Through In Situ Degradation Sensing," IEEE International Solid-State Circuits Conference (ISSCC), February 2010
141. Jae-sun Seo, Ron Ho, Jon Lexau, Michael Dayringer, Dennis Sylvester, David Blaauw, "High Bandwidth and Low Energy On-Chip Signaling with Adaptive Pre-Emphasis in 90nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), February 2010
142. Gregory Chen, Matthew Fojtik, Daeyeon Kim, David Fick, Junsun Park, Mingoo Seok, Mao-Ter Chen, Zhiyoong Foo, Dennis Sylvester, David Blaauw, "A Millimeter-Scale Nearly-Perpetual Sensor System with Stacked Battery and Solar Cells," IEEE International Solid-State Circuits Conference (ISSCC), February 2010
143. David Fick, Nurrachman Liu, Zhiyoong Foo, Matthew Fojtik, David Blaauw, Dennis Sylvester, "In Situ Delay Slack Monitor for High-Performance Processors using an All-Digital, Self-Calibrating 5ps Resolution Time-to-Digital Converter," IEEE International Solid-State Circuits Conference (ISSCC), February 2010
144. Cheng Zhuo, Yung-Hsu Chang, Dennis Sylvester, David Blaauw, "Design Time Body Bias Selection for Parametric Yield Improvement," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2010
145. Vivek Joshi, Kanak Agarwal, Dennis Sylvester, David Blaauw, "Analyzing Electrical Effects of RTA-driven Local Anneal Temperature Variation," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2010
146. Cheng Zhuo, David Blaauw, Dennis Sylvester, "Post-Fabrication Measurement-Driven Oxide Breakdown Reliability Prediction and Management," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2009
147. Ravikishore Gandikota, David Blaauw, Dennis Sylvester, "Interconnect Performance Corners considering Crosstalk Noise," IEEE International Conference on Computer Design (ICCD), October 2009
148. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "Near-Field Communications using Phase-Locking and Pulse Signalling for Millimeter-Scale Systems," IEEE Custom Integrated Circuits Conference (CICC), September 2009
149. Mingoo Seok, Gyouho Kim, Dennis Sylvester, David Blaauw, "A 0.5V 3.6ppm/0C 2.2pW 2-Transistor Voltage Reference," IEEE Custom Integrated Circuits Conference (CICC), September 2009
150. Daeyeon Kim, Yoonmyung Lee, Jin Cai, Leland Chang, Steven J. Koester, Dennis Sylvester, David Blaauw, "Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs)," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2009, **Best Paper Award**
151. Ronald G. Dreslinski, David Fick, David Blaauw, Dennis Sylvester, Trevor Mudge, "Reconfigurable Multicore Server Processors for Low Power Operation," International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS), July 2009
Vineeth Veetil, Dennis Sylvester, David Blaauw, Saumil Shah, Steffen Rochel, "Efficient Smart Sampling based Full-Chip Leakage Analysis for Intra-Die Variation Considering State Dependence," ACM/IEEE Design Automation Conference (DAC), July 2009

152. Ravikishore Gandikota, Li Ding, Peivand Tehrani, David Blaauw, "Worst-Case Aggressor-Victim Alignment with Current-Source Driver Models," ACM/IEEE Design Automation Conference (DAC), July 2009
153. David Fick, Andrew DeOrio, Jin Hu, David Blaauw, Dennis Sylvester, Valeria Bertacco, "Vicis: A Reliable Network for Unreliable Silicon," ACM/IEEE Design Automation Conference (DAC), July 2009
154. Jae-Sun Seo, Dennis Sylvester, David Blaauw, "Crosstalk-Aware PWM-Based On-Chip Global Signaling in 65nm CMOS," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2009
155. Mike Wieckowski, Gregory K. Chen, Mingoo Seok, David Blaauw, Dennis Sylvester, "A hybrid DC-DC Converter for Sub-Microwatt Sub-IV Implantable Applications," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2009
156. David Fick, Andrew DeOrio, Gregory Chen, Valeria Bertacco, Dennis Sylvester, David Blaauw, "A Highly Resilient Routing Algorithm for Fault-Tolerant NoCs," ACM/IEEE Design Automation and Test in Europe Conference (DATE), April 2009
157. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "A 150pW Program-and-Hold Timer for Ultra-Low Power Sensor Platforms," IEEE International Solid-State Circuits Conference (ISSCC), February 2009
158. Carlos Tokunaga, David Blaauw, "Secure AES engine with a local switched capacitor current equalizer," IEEE International Solid-State Circuits Conference (ISSCC), February 2009, *Invited Paper to the IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC*
159. Ronald Dreslinski, Greg Chen, Trevor Mudge, David Blaauw, Dennis Sylvester, Krisztian Flautner, "Reconfigurable Energy Efficient Near Threshold Cache Architectures," ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2008
160. Brian Cline, Vivek Joshi, Dennis Sylvester, David Blaauw, "Stress-Enhanced Standard Cell Library Design," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2008
161. Jae-Sun Seo, Igor Markov, Dennis Sylvester, David Blaauw, "On the Decreasing Significance of Large Standard Cells in Technology Mapping," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2008
162. Kaviraj Chopra, Cheng Zhuo, David Blaauw, Dennis Sylvester, Vladimir Zolotov, "A Statistical Approach for Full-Chip Gate-Oxide Reliability Analysis," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2008
163. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "An Ultra Low Power 1V, 220nW Temperature Sensor for Passive Wireless Applications," IEEE Custom Integrated Circuits Conference (CICC), September 2008
164. Mingoo Seok, Scott Hanson, Jae-Sun Seo, Dennis Sylvester, David Blaauw, "Robust Ultra-Low Voltage ROM Design," IEEE Custom Integrated Circuits Conference (CICC), September 2008
165. Michael Wieckowski, Young Min Park, Carlos Tokunaga, Dong Woon Kim, Zhiyoong Food, Dennis Sylvester, David Blaauw, "Timing Yield Enhancement Through Soft Edge Flip-Flop Based Design," IEEE Custom Integrated Circuits Conference (CICC), September 2008
166. Sanjay Pant, David Blaauw, "Circuit Techniques for Suppression and Measurement of On-chip Inductive Supply Noise," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2008

167. Yoonmyung Lee, Mingoo Seok, Scott Hanson, David Blaauw, Dennis Sylvester, "Standby Power Reduction Techniques for Ultra-Low Power Processors," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2008
168. Cheng Zhuo, David Blaauw, Dennis Sylvester, "Variation-Aware Gate Sizing and Clustering for Post-Silicon Optimized Circuits," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2008
169. Mingoo Seok, Dennis Sylvester, David Blaauw, "Optimal Technology Selection for Minimizing Energy and Variability in Low Voltage Applications," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2008
170. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "Sensor Data Retrieval Using Alignment Independent Capacitive Signaling," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2008, *Invited Paper to the IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI Circuits*
171. Mingoo Seok, Scott Hanson, Yu-Shiang Lin, Zhiyoong Foo, Dayeon Kim, Yoonmyung Lee, Nurachman Liu, Dennis Sylvester, David Blaauw, "The Phoenix Processor: A 30pW Platform for Sensor Applications," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2008, *Invited Paper to the IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI Circuits*
172. Ravikishore Gandikota, David Blaauw, Dennis Sylvester, "Modeling Crosstalk in Statistical Static Timing Analysis", ACM/IEEE Design Automation Conference (DAC), June 2008
173. Vivek Joshi, Brian Cline, Dennis Sylvester, David Blaauw, Kanak Agarwal, "Leakage Power Reduction Using Stress-Enhanced Layouts," ACM/IEEE Design Automation Conference (DAC), June 2008
174. Vineeth Veetil, Dennis Sylvester, David Blaauw, "Efficient Monte Carlo based Incremental Statistical Timing Analysis," ACM/IEEE Design Automation Conference (DAC), June 2008
175. Yu-Shiang Lin, Scott Hanson, Fabio Albano, Carlos Tokunaga, Razi-UI Haque, Kensall Wise, Ann Marie Sastry, David Blaauw, Dennis Sylvester, "Low-Voltage Circuit Design for Widespread Sensing Applications," IEEE International Symposium on Circuits and Systems (ISCAS), May 2008
176. Vivek Joshi, Brian Cline, Dennis Sylvester, David Blaauw, Kanak Agarwal, "Stress Aware Layout Optimization", ACM/IEEE International Symposium on Physical Design (ISPD), April 2008
177. Eric Karl, David Blaauw, Dennis Sylvester, "Analysis of System-Level Reliability Factors and Implications on Real-time Monitoring Methods for Oxide Breakdown Device Failures," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2008
178. Brian Cline, Kaviraj Chopra, David Blaauw, Andres Torres, Savithri Sundareswaran, "Transistor-Specific Delay Modeling for SSTA," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2008
179. Eric Karl, Prashant Singh, David Blaauw, Dennis Sylvester, "Compact in situ Sensors for Monitoring NBTI and Oxide Degradation," IEEE International Solid-State Circuits Conference (ISSCC), February 2008
180. David Blaauw, Sudharsan Kalaiselvan, Kevin Lai, Wei-Hsiang Ma, Sanjay Pant, Carlos Tokunaga, Shidhartha Das, David Bull, "RazorII: In-Situ Error Detection and Correction for PVT and SER tolerance," IEEE International Solid-State Circuits Conference (ISSCC), February 2008, *Invited Paper to the IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC*
181. Sanjay Pant, David Blaauw, "A Charge-Injection Based Active Decoupling Technique for Inductive Supply Noise Suppression," IEEE International Solid-State Circuits Conference (ISSCC), February 2008

182. Gregory Chen, David Blaauw, Nam Sung Kim, Trevor Mudge, Dennis Sylvester, "Yield-driven Near-threshold SRAM Design," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2007
183. Ravikishore Gandikota, Kaviraj Chopra, David Blaauw, Murat Becer, "Victim Alignment in Cross-talk Aware Timing Analysis," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2007
184. Vivek Joshi, David Blaauw, Dennis Sylvester, "Soft-edge Flip-flops for Improved Timing Yield: Design and Optimization," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2007
185. Ronald G. Dreslinski, Bo Zhai, Trevor Mudge, David Blaauw, Dennis Sylvester, "An Energy Efficient Parallel Architecture Using Near Threshold Operation," Parallel Architectures and Compilation Techniques (PACT), September 2007
186. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "A sub-pW timer using gate leakage for ultra low power sub-Hz monitoring systems," IEEE Custom Integrated Circuits Conference (CICC), September 2007
187. Jae-sun Seo, Dennis Sylvester, David Blaauw, Himanshu Kaul, Ram Krishnamurthy, "A Robust Edge Encoding Technique for Energy-Efficient Multi-Cycle Interconnect," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2007
188. Bo Zhai, Ronald G. Dreslinski, Trevor Mudge, David Blaauw, Dennis Sylvester, "Energy Efficient Near-threshold Chip Multi-processing," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2007, **Best Paper Nomination**
189. Scott Hanson, Bo Zhai, Mingoo Seok, Brian Cline, Kevin Zhou, Meghna Singhal, Michael Minuth, Javin Olson, Leyla Nazhandali, Todd Austin, Dennis Sylvester, David Blaauw, "Performance and variability optimization strategies in a sub-200mV, 3.5pJ/inst, 11nW subthreshold processor," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2007, *Invited Paper to the IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI Circuits*
190. Mingoo Seok, Scott Hanson, Dennis Sylvester, David Blaauw, "Analysis and Optimization of Sleep modes in Subthreshold Circuit Design," ACM/Design Automation Conference (DAC), June 2007
191. Ravikishore Gandikota, Kaviraj Chopra, David Blaauw, Dennis Sylvester, Murat Becer, "Top-k Aggressors Sets in Delay Noise Analysis," ACM/IEEE Design Automation Conference (DAC), June 2007
192. Scott Hanson, Mingoo Seok, Dennis Sylvester, David Blaauw, "Nanometer Device Scaling in Sub-threshold Circuits," ACM/Design Automation Conference (DAC), June 2007
193. Mini Nanua, David Blaauw, "Investigating Crosstalk in Sub-Threshold Circuits," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2007
194. Jae-Sun Seo, Prashant Singh, Dennis Sylvester, David Blaauw, "Self-timed Regenerators for High-speed and Low-power Interconnect," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2007, **Best Paper Nomination**
195. Bo Zhai, David Blaauw, Dennis Sylvester, Scott Hanson, "A sub-200mV 6T SRAM in 130nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), February 2007, *Invited Paper to the Special Issue on the 2008 Compound Semi-Conductor Integrated Circuit Symposium (CSICS'08)*

196. Carlos Tokunaga, David Blaauw, Trevor Mudge, "A True Random Number Generator with a Metastability-Based Quality Control," IEEE International Solid-State Circuits Conference (ISSCC), February 2007, *Invited Paper to the Special Issue on the 2007 IEEE International Solid-State Circuits Conference (ISSCC)*
197. Brian Cline, Kaviraj Chopra, David Blaauw and Yu Cao, "Analysis and Modeling of CD Variation for Statistical Static Timing," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2006
198. Sarvesh Kulkarni, Dennis Sylvester and David Blaauw "A Statistical Approach to Body Bias Clustering for Post-Silicon Tuning," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2006
199. Rajeev Rao, David Blaauw and Dennis Sylvester, "Soft Error Reduction in Combinational Logic Using Gate Resizing and Flip-flop Selection," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2006
200. Kaviraj Chopra, Bo Zhai, David Blaauw and Dennis Sylvester, "A New Statistical Max Operation for Propagating Skewness Statistical Timing Analysis," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2006
201. Sanjay Pant, David Blaauw, "An Active Decoupling Capacitance Circuit for Inductive Noise Suppression in Power Supply Networks," IEEE International Conference on Computer Design (ICCD), October 2006
202. Scott Hanson, Dennis Sylvester, David Blaauw, "A New Technique for Jointly Optimization Gate Sizing and Supply Voltage in Ultra-Low Energy Circuits," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), September 2006
203. Eric Karl, David Blaauw, Dennis Sylvester, Trevor Mudge, "Reliability Modeling and Management in Dynamic Microprocessor-Based Systems," ACM/IEEE Design Automation Conference (DAC), July 2006
204. Bo Zhai, Leyla Nazhandali, Javin Olson, Anna Reeves, Michael Minuth, Ryan Helfand, Sanjay Pant, David Blaauw, Todd Austin, "A 2.60pJ/Inst. Subthreshold Sensor Processor for Optimal Energy Efficiency," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2006
205. Vivek Joshi, Rajeev Rao, Dennis Sylvester, David Blaauw, "Logic SER Reduction through Flip-flop Redesign," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2006
206. Rajeev Rao, Kaviraj Chopra, David Blaauw, Dennis Sylvester, "An Efficient Static Algorithm for Soft Error Rate Analysis of Combinational Circuits," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2006
207. Sanjay Pant, David Blaauw, "Timing-Aware Decoupling Capacitance Allocation in Power Distribution Networks," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2006
208. Saumil Shah, Ashish Srivastava, Dushyant Sharma, Dennis Sylvester, David Blaauw, Vladimir Zolotov, "Discrete Vt Assignment and Gate Sizing Using a Self-Snapping Continuous Formulation," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2005
209. Kavi Chopra, Saumil Shah, Ashish Srivastava, David Blaauw Dennis Sylvester, "Parametric Yield Maximization using Gate Sizing based on Efficient Statistical Power and Delay Gradient Computation," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2005

210. Amit Jain, Vladimir Zolotov, David Blaauw, "Accurate Delay Computation for Noisy Waveform Shapes," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2005
211. Sanjay Pant, David Blaauw, "Static Timing Analysis Considering Power Supply Variations," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2005
212. Leyla Nazhandali, Michael Minuth, Bo Zhai, Javin Olson, Scott Hanson, Todd Austin, David Blaauw, "A Second-Generation Sensor Network Processor with Application-Driven Memory Optimizations and Out-of-Order Execution," ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), September 2005.
213. Bo Zhai, Scott Hanson, David Blaauw, Dennis Sylvester, "Analysis and Mitigation of Variability in Subthreshold Design," ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 2005
214. Shidhartha Das, Sanjay Pant, David Roberts, Seokwoo Lee, David Blaauw, Todd Austin, Trevor Mudge, Krisztián Flautner, "A Self-Tuning DVS Processor Using Delay-Error Detection and Correction," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2005, *Invited Paper to the Special Issue on the 2005 Symposium on VLSI Circuits*
215. Leyla Nazhandali, Anna Reeves, Michael Minuth, Ryan Helfand, Javin Olson, Bo Zhai, Sanjay Pant, Todd Austin, David Blaauw, "Energy Optimization of Subthreshold Voltage Sensor Processors," International Symposium on Computer Architecture (ISCA), June 2005
216. Ashish Agarwal, Saulim Shah, Dennis Sylvester, David Blaauw, "Accurate and Efficient Gate-Level Parametric Yield Estimation Considering Power/Performance Correlation", ACM/IEEE Design Automation Conference (DAC), June 2005
217. Aseem Agarwal, Kaviraj Chopra, Vladimir Zolotov, David Blaauw, "Circuit Optimization using Statistical Static Timing Analysis," ACM/IEEE Design Automation Conference (DAC), June 2005
218. David Blaauw, Kaviraj Chopra, "CAD Tools for Variation Tolerance," ACM/IEEE Design Automation Conference (DAC), June 2005
219. Eric Karl, Dennis Sylvester, David Blaauw, "Timing Error Correction Techniques for Voltage-Scalable On-Chip Memories," IEEE International Symposium on Circuits and Systems (ISCAS), May 2005
220. Amit Jain, David Blaauw, "Slack Borrowing in Flip-Flop Based Sequential Circuits," ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI), April 2005
221. Rajeev Rao, David Blaauw, Dennis Sylvester, Charles Alpert, Sani Nassif, "An Efficient Surface-Based Low-Power Buffer Insertion Algorithm," ACM/IEEE International Symposium on Physical Design (ISPD), April 2005
222. Aseem Agarwal, Kaviraj Chopra, Vladimir Zolotov, David Blaauw, "Statistical Timing Based Optimization Using Gate Sizing," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2005
223. Himanshu Kaul, Dennis Sylvester, David Blaauw, Trevor Mudge, Todd Austin, "DVS for On-Chip Designs Based on Timing Error Correction," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2005
224. Harmander Deogun, Dennis Sylvester, David Blaauw, "Gate-Level Mitigation Techniques for Neutron-Induced Soft Error Rate," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2005

225. David Roberts, Todd Austin, David Blaauw, Krisztián Flautner, Trevor Mudge, "Error Analysis for the Support of Robust Voltage Scaling," International Symposium on Quality Electronic Design (ISQED) March 2005
226. Mini Nanua, David Blaauw, Chanhee Oh, "Leakage Current Modeling in PD SOI Circuits," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2005
227. Dongwoo Lee, David Blaauw, Dennis Sylvester, "Runtime Leakage Minimization through Probability-Aware Dual-Vt or Dual-Tox Assignment," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2005, pg. 399-404
228. Kanak Agarwal, Dennis Sylvester, David Blaauw, Anirudh Devgan, "Achieving Continuous Vt Performance in a Dual Vt Process," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2005, pg. 393-398
229. Mridul Agarwal, Kanak Agarwal, Dennis Sylvester, David Blaauw, "Statistical Modeling of Cross-Coupling Effects in VLSI Interconnects," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2005, pg 503-506
230. Seokwoo Lee, Todd Austin, Trevor Mudge, David Blaauw, "Reducing Pipeline Energy Demands with Local DVS and Dynamic Retiming," ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 2004, pg. 319-324
231. Nam Sung Kim, Krisztián Flautner, David Blaauw, Trevor Mudge, "Single-Vdd and Single-Vt Super-Drowsy Techniques for low-leakage high-performance instruction caches," ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 2004, pg. 54-57
232. Richard Brown, Dennis Sylvester, David Blaauw, Michael Flynn, Gordon Carichner, Catharine June, "VLSI Design Curriculum," ASEE Annual Conference & Exposition, June 2004
233. Aseem Agarwal, Florin Dartu, David Blaauw, "Statistical Gate Delay Model Considering Multiple Input Switching," ACM/IEEE Design Automation Conference (DAC), June 2004, pg. 658-663
234. Seokwoo Lee, Shiddhartha Des, Valeria Bertacco, Todd Austin, David Blaauw, Trevor Mudge, "Circuit-Aware Architectural Simulation," ACM/IEEE Design Automation Conference (DAC), June 2004, pg. 305-310
235. Rajeev Rao, Anirudh Devgan, David Blaauw, Dennis Sylvester, "Parametric Yield Estimation Considering Leakage Variability," ACM/IEEE Design Automation Conference (DAC), June 2004, pg. 442-447, **Best Paper Nomination**
236. Harmander Deogun, Rajeev Rao, Dennis Sylvester, David Blaauw, "Crosstalk- and Leakage-Aware Bus Encoding for Total Power Reduction," ACM/IEEE Design Automation Conference (DAC), June 2004, pg. 779-782
237. Ashish Srivastava, Dennis Sylvester, David Blaauw, "Power Minimization Using Simultaneous Gate Sizing, Dual-Vdd, and Dual-Vth Assignment," ACM/IEEE Design Automation Conference (DAC), June 2004, pg 783-787
238. Ashish Srivastava, Dennis Sylvester, David Blaauw, Aseem Agarwal, "Statistical optimization of leakage power considering process variations using dual-Vth and sizing," ACM/IEEE Design Automation Conference (DAC), June 2004, pg. 773-778
239. Bo Zhai, David Blaauw, Dennis Sylvester, Krisztián Flautner, "Theoretical and Practical Limits of Dynamic Voltage Scaling," ACM/IEEE Design Automation Conference (DAC), June 2004, pg. 868-873
240. Dongwoo Lee, Vladimir Zolotov, David Blaauw, "Static Timing Analysis using Backward Signal Propagation," ACM/IEEE Design Automation Conference (DAC), June 2004, pg. 664-669

241. Kanak Agarwal, Dennis Sylvester, David Blaauw, Frank Liu, and Sarma Vrudhula, "Variational Delay Metrics for Interconnect Timing Analysis," ACM/IEEE Design Automation Conference (DAC), June 2004, pg. 381-384
242. Sanjay Pant, David Blaauw, Vladimir Zolotov, Savithri Sundareswaran, "A Stochastic Approach to Power Grid Analysis," ACM/IEEE Design Automation Conference (DAC), June 2004, pg. 171-176
243. Woo Hyung Lee, Sanjay Pant, David Blaauw, "Analysis and reduction of on-chip inductance effects in power supply grids," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2004, pg. 131-136
244. Ashish Srivastava, Dennis Sylvester, David Blaauw, "Concurrent Sizing, Vdd and Vth Assignment for Low-Power Design," ACM/IEEE Design Automation and Test in Europe Conference (DATE), Vol. 1, February 2004, pg. 718-719
245. Dongwoo Lee, Harmander Deogun, David Blaauw, Dennis Sylvester, "Simultaneous State, Vt and Tox Assignment for Total Standby Power Minimization," ACM/IEEE Design Automation and Test in Europe Conference (DATE), Vol. 1, February 2004, pg. 494-499
246. Kanak Agarwal, Dennis Sylvester, David Blaauw, "A Simplified Transmission-Line Based Crosstalk Noise Model for On-Chip RLC Wiring," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2004, pg. 859-865
247. Dan Ernst, Nam Sung Kim, Shidhartha Das, Sanjay Pant, Toan Pham, Rajeev Rao, Conrad Ziesler, David Blaauw, Todd Austin, Trevor Mudge, "Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation," ACM/IEEE International Symposium on Microarchitecture (MICRO), December 2003, pg. 7-18 **Best Paper Award**
248. Kanak Agarwal, Dennis Sylvester, David Blaauw, "Dynamic Clamping: On-Chip Dynamic Shielding and Termination for High-Speed RLC Buses," IEEE International Symposium on System-on-Chip, November 2003, pg. 97-100
249. Aseem Agarwal, David Blaauw, Vladimir Zolotov, "Statistical Clock Skew Analysis Considering Intra-Die Process Variations," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2003, pg. 914-921
250. Aseem Agarwal, David Blaauw, Vladimir Zolotov, "Statistical Timing Analysis for Intra-Die Process Variations with Spatial Correlations," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2003, pg. 900-907
251. Sanjay Pant, David Blaauw, Vladimir Zolotov, Savithri Sundareswaran, Rajendran Panda, "Vectorless Analysis of Supply Noise Induced Delay Variation," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2003, pg. 184-191
252. Dmitry Nadezhin, Sergey Gavrilov, Alexey Glebov, Yury Egorov, Vladimir Zolotov, David Blaauw, Rajendran Panda, Murat Becer, Alexandre Ardelea, Ajay Patel, "SOI Transistor Model for Fast Transient Simulation," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2003, pg. 120-127
253. Sarvesh Bhardwaj, Sarma Vrudhula, David Blaauw, "□AU: Timing Analysis Under Uncertainty," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2003, pg. 615-620
254. Nam Sung Kim, David Blaauw, Trevor Mudge, "Leakage Power Optimization Techniques for Ultra Deep Sub-Micron Multi-Level Caches," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2003, pg. 627-632

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256. Mini Nanua, David Blaauw, "Noise Analysis Methodology for Partially Depleted SOI Circuits," IEEE Custom Integrated Circuits Conference (CICC), September 2003, pg. 719-722 **Best Paper Award, Invited Paper to the Special Issue on the 2003 Custom Integrated Circuits Conference (CICC 2003)**
257. Himanshu Kaul, Dennis Sylvester, David Blaauw, "Clock Net Optimization Using Active Shielding," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2003, pg. 265-268
258. Rajeev Roa, Ashish Srivastava, David Blaauw, Dennis Sylvester, "Statistical Estimation of Leakage Current Considering Inter- and Intra-Die Process Variation," ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 2003, pg. 84-89
259. Dongwoo Lee, David Blaauw, "Static Leakage Reduction through Simultaneous Threshold Voltage and State Assignment," ACM/IEEE Design Automation Conference (DAC), June 2003, pg. 191-194
260. Dongwoo Lee, Wesley Kwong, David Blaauw, Dennis Sylvester, "Analysis and Minimization Techniques for Total Leakage Considering Gate Oxide Leakage," ACM/IEEE Design Automation Conference (DAC), June 2003, pg. 175-180
261. Murat R. Becer, David Blaauw, Ilan Algor, Rajendran Panda, Chanhee Oh, Vladimir Zolotov, Ibrahim Hajj, "Post-Route Gate Sizing for Crosstalk Noise Reduction," ACM/IEEE Design Automation Conference (DAC), June 2003, pg. 954-957
262. Kanak Agarwal, Dennis Sylvester, David Blaauw, "Simple Metrics for Slew Rate of RC Circuits Based on Two Circuit Moments," ACM/IEEE Design Automation Conference (DAC), June 2003, pg. 950-953
263. Kanak Agarwal, Dennis Sylvester, David Blaauw, "An Effective Capacitance Based Driver Output Model for On-Chip RLC Interconnects," ACM/IEEE Design Automation Conference (DAC), June 2003, pg. 376-381
264. Aseem Agarwal, David Blaauw, Vladimir Zolotov, "Computation and Refinement of Statistical Bounds on Circuit Delay," ACM/IEEE Design Automation Conference (DAC), June 2003, pg. 348-353
265. Bhavana Thudi, David Blaauw, "Non-Iterative Timing Window Computation for Delay Noise," ACM/IEEE Design Automation Conference (DAC), June 2003, pg. 390-395
266. Haitian Hu, Vladimir Zolotov, Min Zhao, Rajendran Panda, David Blaauw, Sachin Sapatnekar, "Table Look-up Based Compact Modeling for On-Chip Interconnect Timing and Noise Analysis," IEEE International Symposium on Circuits and Systems (ISCAS), May 2003, pg. 668-671
267. Aseem Agarwal, Vladimir Zolotov, David Blaauw, "Statistical Timing Analysis Using Bounds," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2003, pg. 62-67
268. Dongwoo Lee, Wesley Kwong, David Blaauw, Dennis Sylvester, "Simultaneous Subthreshold and Gate-Oxide Tunneling Leakage Current in Nanometer CMOS Design," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2003, pg. 287-292
269. David Blaauw, Vladimir Zolotov, Chanhee Oh, Murat Becer, Rajendran Panda, "Static Electromigration Analysis for Signal Interconnects," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2003, pg. 377-382

270. Murat R. Becer, David Blaauw, Ilan Algor, Rajendran Panda, Chanhee Oh, Vladimir Zolotov, Ibrahim Hajj, "Post-Route Gate Sizing for Crosstalk Noise Reduction," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2003, pg. 171-176
271. Robert Bai, Sarvesh Kulkarni, Wesley Kwong, Ashish Srivastava, Dennis Sylvester, David Blaauw, "An Implementation of a 32-bit ARM Processor Using Dual Power Supplies and Dual Threshold Voltages," IEEE Computer Society Annual Symposium on VLSI, February 2003, pg. 149-154
272. Aseem Agarwal, David Blaauw, Vladimir Zolotov, Savithri Sundareswaran, Min Zhou, Kaushik Gala, Rajendran Panda, "Statistical Delay Computation Considering Spatial Correlations," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2003, pg. 271-276, **Best Paper Award**
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VI Scholarly Addresses

A. Conference Keynote Addresses and Invited Presentations

1. Invited presentation, “Low-Power Circuit Techniques for IoT Energy Harvesting,” International Symposium on Quality Electronic Design (ISQED), March 2016
2. Plenary Keynote Address, “From Digital Processors to Analog Building Blocks: Enabling New Applications through Ultra-Low Voltage Design,” IEEE Subthreshold Microelectronics Conference (SubVt), October 2012
3. Invited presentation, “Adaptive Sensing and Design for Reliability,” IEEE International Reliability Physics Symposium, May 2010
2. Invited presentation, “Architectural Techniques for Self-Adaptive Computing,” IEEE International Solid-State Circuits Conference (ISSCC), February 2007
3. Invited presentation, “Energy Optimality and Variability in Subthreshold Design,” ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), September 2006
4. Invited presentation, “Energy Efficient Design for Subthreshold Supply Voltage Operation,” IEEE International Symposium on Circuits and Systems (ISCAS), May 2006
5. Invited presentation, “Extended Dynamic Voltage Scaling for Low Power Design,” IEEE International SOC Conference, September 2004
6. Invited presentation, “Signal Integrity Issues in High Performance Design,” IEEE International Workshop-Power And Timing Modeling, Optimization and Simulation (Patmos), Switzerland, September 2001
7. Invited presentation, “Inductance 101: Analysis and Design,” ACM/IEEE Design Automation Conference, June 2001
8. Invited presentation, “Inductance Extraction and Modeling,” ACM/IEEE Great Lakes Symposium on VLSI Design (GLSVLSI), March 2000
9. Keynote address, “Power Management Issues in High Performance Processor Design,” IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), Italy, March 1999
10. Keynote address, “Industrial Perspectives on Emerging CAD Tools for Low Power Processor Design,” ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 1998

B. Conference Tutorials

1. “Managing Variations Through Adaptive Design Techniques,” half-day tutorial, IEEE International Solid-State Circuits Conference (ISSCC), February 2009
2. “Circuit and CAD Techniques for Low Power Design,” full day tutorial with co-presenter Anantha Chandrakasan, ACM/IEEE Design Automation Conference (DAC), June 2007
3. “Future Trends and Issues in DVS,” full day tutorial with co-presenters Barry Pangrle, David Flynn, David Tamura, ACM/IEEE Design Automation Conference (DAC), June 2005
4. “Leakage Issues in IC Design: Trends, Estimation, Avoidance,” embedded tutorial with co-presenter Anirudh Devgan, ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2005
5. “Low Power Robust Computing,” full day tutorial with co-presenters Todd Austin, Krisztián Flautner, Nam Sung Kim, Trevor Mudge, Dennis Sylvester, ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2004

6. "Standby Leakage Analysis and Optimization Methods for VLSI Design," full day tutorial with co-presenters Anirudh Devgan, Siva Narendra, Farid Najm, ACM/IEEE International Conference on Computer Aided Design (ICCAD), November 2003
7. "Design for Manufacturing in the Sub-100nm Era," full day tutorial with co-presenters Louis Scheffer, Sani Nassif, Andrzej Strojwas, ACM/IEEE Design Automation Conference (DAC), June 2003
8. "Inductance Extraction and Modeling," half-day tutorial with co-presenters Shannon Morton, Philip Restle, Claude Gauthier, IEEE International Solid-State Circuits Conference (ISSCC), February 2002
9. "On-Chip and Package Inductance Issues," half day tutorial with co-presenter Rajendran Panda, ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2001
10. "Signal Integrity Analysis in High Performance Design," full day tutorial with co-presenters Anirudh Devgan, Abhijit Dharchoudhury, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 1999
11. "Interconnect-Driven Performance Optimization for Deep Submicron Layout Systems," full day tutorial with co-presenters Jason Cong, Ren-Song Tsay, ACM/IEEE Design Automation Conference (DAC), June 1997

C. University Lectures and Seminars Presentations

1. "Razor: Power and Reliability Trade-Offs in DVS," Invited Presentation, India Institute of Technology (IIT) Mumbai, India, December 2004
2. "Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation," Invited Seminar, University of Delft, Netherlands, August 2004
3. "Dynamic Voltage Scaling Based on Timing Speculation," Invited Presentation, University of Arizona, October 2003
4. "Statistical Analysis of Circuit Performance," Distinguished Lecture Series, University of Toronto, April 2003
5. "Signal Integrity in High Performance Design," Center for Low Power Electronic Seminar Series, University of Arizona, February 2001
6. "Deep Submicron Issues in High Performance Designs," Microsystems Technology Laboratories Seminar Series, Massachusetts Institute of Technology, October, 2000
7. "CAD Challenges for High-Performance and Low-Power Processor Designs," Electrical and Computer Engineering Graduate Seminar, University of Illinois, Urbana-Champaign, February 1999
8. "Emerging Deep Submicron Issues in Industrial Designs," Electrical and Computer Engineering Graduate Seminar, Purdue University, February 1999

D. Industrial Invited Presentations

1. "Low Voltage Circuits for Ultra Low Energy Consumption," Qualcomm Corporation, San Diego, CA, May, 2007
2. "Energy Efficient Computation using Low Voltage Operation," Sun Microsystems, Santa Clara, CA, May, 2007
3. "Ultra Low Power Sensor Design using Extreme Voltage Scaling," Philips Research Laboratory, Eindhoven, Netherlands, August, 2006
4. "Low Power Sensor Design," Totoya Research Center, Detroit, MI, April, 2006

5. "Subthreshold Processor Design," Freescale Semiconductor, Austin, TX, January 2006
6. "Computer-Aided Design Methods for Nano-meter VLSI Designs," Intel Corporation, Strategic CAD Laboratory, Portland, OR, January 2006
7. "Advanced Circuit Design Techniques for Low-Power Design," Intel Corporation, Circuits Research Laboratory, Portland, OR, January 2006
8. "Subthreshold Design for Low Power Sensor Processors," ARM Ltd, Cambridge, England, December 2005.
9. "Razor: Low Power and Robust Design using DVS," Nvidia Design Corporation, San Jose, CA, November 2005
10. "Statistical Timing Analysis: Basic Principles and State-of-the-Art," CLK Design Automation, Boston, MA, October 2005
11. "Razor: Low Power and Robust Design using DVS," Freescale Semiconductor, Austin, TX, October 2005
12. "Statistical Performance Analysis and Optimization," Synopsys Inc, San Jose, CA, February 2005
13. "Circuit Analysis and Optimization Method for High-Performance Design," Intel Strategic Computer-Aided Design Laboratory, Portland, OR, December 2004
14. "Energy efficient computation using subthreshold operation," Intel Circuits Research Laboratory, Portland, Oregon, December 2004
15. "Razor Prototype Chip Results," ARM Ltd, Cambridge England, September 2004
16. "Subliminal Systems, the Final Computing Frontier," ARM Ltd, Cambridge England, September 2004
17. "Statistical Timing Analysis," LSI Logic Corporation, May 2004
18. "Analysis and Minimization Techniques for Subthreshold and Gate Oxide Leakage Current," Intel Circuits Research Laboratory, Portland, Oregon, January 2004
19. "Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation," Intel Circuits Research Laboratory, Portland, Oregon, January 2004
20. "Razor: Dynamic Voltage Scaling Based on Timing Speculation," IBM Austin Research Laboratory, Austin, Texas, October 2003
21. "Statistical Performance Analysis," Intel Timing Verification Seminar, Portland Oregon, June 2003
22. "Leakage Analysis for High-Speed Circuits," Intel Circuits Research Laboratory, Portland, Oregon, May 2003
23. "Statistical Timing Analysis," Magma Design Automation, December 2003
24. "Performance Analysis of Power-Supply Noise on High-Speed Circuits," Intel Strategic Computer-Aided Design Laboratory, Portland, Oregon, May 2003
25. "Leakage and Power Analysis for Deep-Submicron VLSI," Texas Instruments Corp., Dallas, Texas, April 2003
26. "Performance and Power Analysis in High-Performance VLSI Designs," Motorola Advanced Design Technology Group, Austin, Texas, February 2003
27. "Leakage Analysis and Reduction Methods," IBM Austin Research Laboratory, Austin, Texas, February 2003
28. "Statistical Timing Analysis for VLSI Design," IBM Design Automation Professional Interest Seminar, IBM T. J. Watson Research Center, York Town, New York, September 2002

29. "Variability in Chip-Level Performance Analysis," Intel Performance Verification Seminar, Intel Inc., Haifa, Israel, May 2002
30. "Signal Integrity Methods for Deep Submicron Design," Cadence Deep-Submicron Design Seminar, Cadence Berkeley Labs, Berkeley, California, December 2001
31. "Signal Integrity Issues in High-Performance Design," Motorola Internal Conference on Signal Integrity, Austin, Texas, October 2000
32. "Circuit Analysis Techniques," Motorola Timing Meeting, Motorola, Inc., Tel Aviv, Israel, April 2000

VII Professional Activities

A. Professional Societies

- Senior Member of the Institute of Electrical and Electronics Engineers (IEEE).
- Member of the Association of Computing Machinery (ACM).

B. Editor, Co-Editor, and Associate Editor Positions

- Associate editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, December 2003 - January 2006
- Co-guest editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, special issue on the Design Automation Conference, 2002
- Co-guest editor, *IEEE Design and Test of Computers*, special issue on the Design Automation Conference, 2002
- Co-guest editor, *IEEE Transactions on Very Large Scale Integration Systems (T-VLSI)*, special issue on Low Power Electronics, 1999

C. Conference and Workshop Chair Positions

- Panel Chair, ACM/IEEE Design Automation Conference (DAC), 2003
- Co-Chair, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2002
- Co-Chair, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2001
- General Co-Chair, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2000
- Tutorial Chair, ACM/IEEE Design Automation Conference (DAC), 2000
- Co-Chair, technical program committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 1999

D. Consulting & Advisory Boards

- **Technical Consulting and Advisory boards**
 - Member of University of Illinois at Urbana – Champaign Advisory Panel 2013 – current
 - Gear Inc. 2013 – 2015
 - Apache Design Automation – member of advisory board
 - Nascentric, Technical Consulting, 2008
 - CLK Design Automation (CLK-DA), Technical Consulting, 2005 – 2008
- **Legal Consulting**
 - Parkins Coie LLP, 2014 – 2015
 - WilmerHale, 2012 – 2013
 - Alston & Bird, 2010 – 2011
 - Weil, Gotshal & Manges, 2008 – 2010
 - WilmerHale, 2007

- **Conference Organization**

- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2009
- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2008
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2007
- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2007
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2006
- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2006
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2006
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2005
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2005
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2005
- Member, executive committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2005
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2004
- Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2004
- Member, technical program committee, ACM Workshop on Power-Aware Computer Systems (PACS), 2004
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2004
- Member, technical program committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2004
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2003
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2003
- Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2003
- Member, technical program committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2003
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2003

- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2002
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2002
- Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2002
- Member, technical program committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2002
- Member, technical program committee, ACM/IEEE Design Automation and Test in Europe Conference (DATE), 2002
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2001
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2001
- Member, technical program committee, IEEE International Conference on Computer Design (ICCD), 2001
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2000
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2000
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2000
- Member, technical program committee, IEEE International Conference on Computer Design (ICCD), 2000
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- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 1998
- Member, technical program committee, IEEE International Conference on Computer Design (ICCD), 1998
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 1998
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 1997

F. Refereeing and Reviewing

- NSF, SRC, Natural Science and Engineering Research Council of Canada (NSERC)

- IEEE , IEEE T-VLSI, ACM TODAES, IEEE D&T
- DAC, ICCAD, ISLPED, ICCD, ISPD, TAU, DATE, ISCAS, ISQED, PACS