CURRICULUM VITAE

David T. Blaauw

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I Personal Data

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II Employment History

A. Education

Doctor of Philosophy in Computer Science, University of Illinois, Urbana-Champaign, January 1992.
Thesis: "Functional Abstraction in Switch-Level Simulation."
Advisor: Professor Jacob A. Abraham

Master of Science in Computer Science, University of Illinois, Urbana-Champaign, May 1989.
Thesis: "Automatic Generation of Behavioral Models."
Advisor: Professor Jacob A. Abraham

Bachelor of Science in Physics with a second major in Computer Science, Duke University, May 1986.

B. Present Position

Professor of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.

C. Employment History

• September 2007 - Present:	Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan
• August 2001 - September 2007:	Associate Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan.
• September 1994 - August 2001:	Engineering Manager, Advanced Design Technology, Motorola, Inc., Austin, Texas.
• August 1993 - September 1994:	Staff engineer, Semiconductor Systems Design Technology Group, Motorola, Inc., Austin, Texas.
• August 1992 - August 1993:	Development Staff Member, IBM Corporation, Endicott, New York.

D. Honors and Awards

- 15 year retrospective most influential paper in ISCA 2002 award for groundbreaking research in power-efficient computing, ACM/IEEE International Conference on Computer Architecture (ISCA), 2017
- Member of University of Illinois Engineering Advisory Panel. 2015 through current.
- Ranked as the top publishing author at IEEE VLSI Circuits Symposium over the last 30 years of the conference with 38 publications. June, 2017
- 2016 SIA-SRC University Researcher Award, established by the semiconductor industry association to recognize lifetime research contributions to the U.S. semiconductor industry by university faculty.
- 2016 IEEE Micro Top Picks special issue "MBus: The Missing Interconnect that Enables the Modular Millimeter-Scale Computing Class and Connects the World's Smallest Computer,"
- Best Paper Award, "Racetrack Converter: A Low Power and Compact Data Converter Using Racetrack Spintronic Devices," IEEE International Symposium on Circuits and Systems (ISCAS), May 2015
- 2014 John von Neumann Student Research Award for Excellence in Systems Research – SONIC Annual Review Meeting
- Recognized as top 50 innovator over the last 50 years graduating from the University of Illinois EECS department in 2014
- College of Engineering Innovation Excellence Award for 2013-2014
- Design Automation Conference (DAC) 50th Anniversary award for being the top 10 most cited DAC authors in DAC's 50 year history, June 2013
- Design Automation Conference (DAC) 50th Anniversary award for publishing the most papers in the fifth decade of DAC's history, June 2013
- 2013 University of Michigan Electrical Engineering and Computer Science (EECS) Department Outstanding Achievement Award for innovative research in variation-tolerant and energy efficient integrated circuit design, and exceptional mentoring and teaching in the area of VLSI circuits
- International Solid-State Circuits Conference (ISSCC) 60th Anniversary Special Recognition top 10 contributing author over the last 10 years, February 2013

- IEEE/ACM International Conference on Computer-Aided Design (ICCAD) Ten Year Retrospective Most Influential Paper Award, "Combined Dynamic Voltage Scaling and Adaptive Body biasing for Lower Power Microprocessors under Dynamic Workloads," ICCAD 2002 Conference, November 2012
- Second Prize in the 18th Samsung Human-Tech Thesis Competition for research on millimeter sensor design, February 2012
- IEEE Fellow status, January 2012
- Winner MuSyC Research Consortium annual best poster award, "A Modular 1mm^3 Die-Stacked Sensing Platform," Nov 2011
- Winner 11th International VLSI-Symposium Low Power Design Contest, "SWIFT: A 2.1Tb/s 32x32 Self-Arbitrating Manycore Interconnect Fabric," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011
- Winner Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC) Design contest, "Design and Implementation of Centip3De, a 7-layer Many-Core System," Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC), Feb/June 2011
- Best Paper Award, "Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs)," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2009
- 2008 Ted Kennedy Family Team Excellence Award (award shared with Todd Austin, Scott Mahlke, Trevor Mudge, Marios Papaefthymiou). The Ted Kennedy Family Team Excellence Award is an annual award given by the University of Michigan, College of Engineering that recognizes the production of an extraordinary and significant piece of work from current or recent collaboration in teaching or research to the College of Engineering.
- 2008 Richard Newton GSRC Industrial Impact Award for "development of the Razor technology" (award shared with Professor Todd Austin). The Richard Newton GSRC Industrial Impact Award is an annual award given by the GSRC DARPA/MARCO center that recognizes research that is "at least five years old and has had a significant industrial impact."
- University of Michigan College of Engineering Research Excellence Award for 2007-2008, January 2008
- Best Paper Nomination, "Energy Efficient Near-threshold Chip Multi-processing," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2007
- Best Paper Nomination, "Self-timed Regenerators for High-speed and Low-power Interconnect," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2007
- Microprocessor Review Analysts' Choice Award in Innovation for "Introducing Speculation on Correctness as a Method for Allowing Circuit Operation Beyond Worst-Case Design," Microprocessor Review, February 2007
- 2004 IEEE Micro Top Picks special issue on the most industry relevant and significant papers of the year in computer architecture, "Razor: Circuit-Level Correction of Timing Errors for Low-Power Operation"
- University of Michigan Henry Russel Award for "Exceptional Scholarship and Conspicuous Ability as a Teacher," November 2004
- Best Paper Nomination, "Parametric Yield Estimation Considering Leakage Variability," ACM/IEEE Design Automation Conference (DAC), June 2004

- Best Paper Award, "Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation," ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2003
- Best Regular Paper Award, "Noise Analysis Methodology for Partially Depleted SOI Circuits," IEEE Custom Integrated Circuits Conference (CICC), September 2003
- IBM Faculty Award, IBM Center for Advanced Studies, June 2003
- Best Paper Award, "Statistical Delay Computation Considering Spatial Correlations," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2003
- IBM Faculty Award, IBM Center for Advanced Studies, June 2002
- Best Paper Nomination, "Pre-route Noise Estimation in Deep Submicron Integrated Circuits," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2002
- Best Paper Nomination, "Driver Modeling and Alignment for Worst-Case Delay Noise," ACM/IEEE Design Automation Conference (DAC), June 2001
- Best Paper Award, "On-Chip Inductance Modeling and Analysis," ACM/IEEE Design Automation Conference (DAC), June 2000
- Motorola Innovation Award, 1997
- Motorola High Impact Technology Award, 1996

III Research Experience

A. Research Interests

My research interests focus on high-performance and low-power VLSI circuits, particularly addressing nano-meter design issues pertaining to power, performance and robustness. My aim is to develop novel circuit design techniques for effective VLSI design in the nano-meter era, in conjunction with efficient and accurate analysis and optimization methods for large, multi-million transistor designs.

B. Doctoral Students Supervised

Student	Thesis Title/Topic	Graduation Date
Taewook Kang		In Progress
Zhehong Wang		In Progress
Kyojin Choo		In Progress
Ziyun Li		In Progress
Yu Zeng		In Progress
Dongkwun Kim		In Progress
Li-Xuan Chuo		In Progress
Xiao Wu		In Progress
Wootaek Lim		In Progress
Yao Shi		In Progress
Taekwang Jang		In Progress
Wanyeong Jung	Low-Power Energy Efficient Circuit Techniques for Small IoT Systems	April 2017
Supreet Jeloka	Cross-point Circuits for Computation, Interconnects, Security and Storage	January 2017

Yejoong Kim	Robust Circuit Design for Low-Voltage VLSI	May 2015
Nathaniel Pinckney	Near-Threshold design	July 2015
Dongmin Yoon	Low power timer references	January 2015
Inhee Lee	Power management for ultra-low power sensors systems	October 2014
Gyouho Kim	Ultra-low power visual monitoring	August 2014
Bharan Giridhar	Adaptive Computing	December 2013
Zhi Yoong Foo	Low power processor design techniques	August 2013
Sudhir Satpathy	Fast and low power inconnect fabrics	December 2012
David Fick	Adaptive Low-power design	August 2012
Yoonmyung Lee	Ultra Low-Power Memory Design	April 2012
Prashant Singh	Reliability analysis and wear-out detection	April 2010
Nurrachman Liu	Automatic tuning of VLSI circuits	April 2010
Brian Cline	Process variation modeling for advance semiconductor circuits	Feb 2010
Cheng Zhuo	VLSI wearout modeling	Dec 2010
Ravikishore Gandikota	Crosstalk-Noise analysis for nanometer VLSI circuits	Aug 2009
Carlos Tokunaga	Circuits and architectures for secure processing	Sep 2008
Shidhartha Das	Razor: circuit speculation for power and performance efficient design	Oct 2008
Kaviraj Chopra	Statistical timing analysis including spatial correlations	Apr 2008

Eric Karl	Reliable computing on unpredictable silicon	Mar 2008
Sanjay Pant	Power grid analysis and design	Dec 2007
Mini Nanua	Leakage and noise analysis in nano-scale technologies	Apr 2007
Bo Zhai	Dynamic voltage scaling for embedded processor designs	Mar 2007
Rajeev Rao	Modeling and design of low-power VLSI systems under for multiple sources of uncertainty	Jul 2006
Dongwoo Lee	Analysis and minimization of leakage current	May 2005
Aseem Agarwal	Statistical timing analysis for VLSI circuits	Mar 2005

C. Masters Students Supervised

Student	Thesis Title/Topic	Graduation Date
Hyungjoo Seo		In Progress
Skyler Skrzyniarz	Low Power Correlation Architectures for GPS	June 2015
Junhua Gu	Low Power Circuits for Analog to digital interfaces	May 2015
Ruochen Xie	Energy Reduction of FeRAM Memories for Millimeter Sensors	May 2015
Allen Wang	Low Power Level Conversion	May 2014
Naveen Akesh	Low Power Audio Device for Developing World	May 2014
Zhe Yu	RF Communication for Millimeter Scale Sensors	May 2014

Hsi-Shou Wu	Low Power Word-Spotting	April 2014
Siddharth Saxena	Low power correlation circuits	May 2013
Karan Jain	Low power synchronization using ambient RF signals	April 2012
Jordan LeNoach	pH sensor for millimeter sensors	Dec 2011
Jeffrey Yeh	Chip design for the developing world	April 2011
Nate Robert	Low power LDO	Dec 2010
Vikas Vinay	Low power Class-D amplifier for developing world applications	Dec 2010
Abhishek Madhaven	Low power chip design	Dec 2010
Junsun Park	Intra-cellular chip design	May 2010
Jou-ching (George) Sung	Low power ADC design	August 2009
Mao-Ter Chen	Low power sensor node design	Dec 2008
Sudherssen Kalaiselvan	Razor-3: A circuit speculation and SEU tolerant circuit technique	May 2007
Deepesh John	Low power design through typical-case optimization	May 2006
Yueh-Chuan Tzeng	Encryption processor for side channel attack avoidance	May 2006
Meghna Singhal	Low power design using subthreshold operation	May 2006
Amir Borna	Analysis of lithographic variations for chip performance	Aug 2005
Amit Jain	Delay modeling for non-ramp input transitions	Nov 2004
Toan Pham	Clock skew reduction using Razor flip-flops	Dec 2003

Bhavana Thudi	Non-iterative switching window computation for delay noise	May 2003
Wesley Kwong	Efficient circuit-level analysis of gate-oxide tunneling current in VLSI designs	May 2003

D. Research Grants (partial)

- DSTL/MoD, "Architectural Design Study for M3 MM Scale Computing GPS Logger," $400,000 with 175,000 to PI David Blaauw, 8/15/2013-3/14/2014
- NSF, "SHF: Small: Minimally Invasive Error Detection/Correction for Runtime Margin Elimination," $450,000 with $252,750 to PI: David Blaauw, 7/2012-6/2015
- BAE Systems/United States Army, "Center for Objective Microelectronics and Biomimetic Adaptive Technology (COM-BAT)," $400,000 with $135,000 to Co-PI David Blaauw, PI:Kamal Sarabandi, Co-PI: David Blaauw, 9/2013 – 8/2016
- ARM, Ltd, "Low Power Computing for Embedded Applications," $5,000,000 total, with approx. $1,600,000 to Co-PI David Blaauw, PI: Trevor Mudge, 5/2010 - 5/2015
- Advanced Energy Consortium, "An Autonomous Microsystem Test-Bed for Extreme Environments: Integrating Sensor Elements, Electronics, and Packaging," $950,000 with $226,625 to Co-PI David Blaauw, PI: Yogesh Gianchandani , 6/2012-12/2014
- Semiconductor Research Corporation (SRC), "Fast Power Supply Boosting for Energy-Efficient, High-Performance Processors," $360,000 total with $180,000 to PI David Blaauw, 8/2012 - 7/2015
- DARPA, "Systems on Nanoscale Information Fabrics (SONIC) Center," $7,008,335, PI: Naresh Shanbhag with $1,401,667 to Co-PI David Blaauw, 1/2013-10/2017
- DARPA, "The TerraSwarm Research Center," $6,887,500, with $ 1,100,000 to Co-PI David Blaauw, PI: Edward Lee, 1/2013-10/2017
- DSTL, "MM scale computing for GPS logger," $400,000, with $175,000 to PI: David Blaauw
- Isocline Engineering LLC, "Power Efficient Software Define Radio (SDR) Mobile Architecture Technology for Handheld Devices," $220,093 to PI: David Blaauw
- Isocline Engineering LLC, " Programmable Microchip for Accelerating Neuromorphic Object Recognition," $45,715 to PI: David Blaauw
- QUALCOMM, "Near Threshold Computing," $100,000, gift, 8/2011-8/2013
- Oracle, "High Performance Razor Architecture " $80,000, gift, 8/2013-8/2014
- AMD, "*In Situ* Wearout Detection and Mitigation," $100,000, gift, with $50,000 to David Blaauw, 11/2011
- Food and Drug Administration, "Smart Rapid Palatal Expander for Pediatric Cleft and Palate Patients," $312,000 total with $136,000 to Blaauw, PI: Jeanne Nervina, University of Michigan, 9/2011- 8/2013
- National Science Foundation (NSF), "Integrating Circuits, Sensing, and Software to Realize the Cubic-mm Computing Class," $2,533,000 total with $519,265 to Blaauw, PI: David Wentzloff, University of Michigan, 08/2011 - 7/2016
- Qualcomm, "Near-Threshold Computing," $50,000, gift, PI: David Blaauw, University of Michigan, 05/2011

- Department of Energy, “Hardware-Software Co-Design for Non-Volatile Memory in Exascale Systems,” $525,000 total with $202,747 to Blaauw, PI: Trevor Mudge, University of Michigan, 01/2011 - 12/2013
- Intel Corporation, “A Confidence-Driven Model for Predictable Computing in Future Technologies,” $249,000 total with $65,916 to Blaauw, PI: Prof. Zhengya Zhang, Co-PIs: Prof. David Blaauw, and Prof. Dennis Sylvester, University of Michigan, 01/2010 - 10/2010
- QUALCOMM, “Adaptive Design Solutions for VLSI Circuits,” $50,000, gift, 09/01/09
- National Science Foundation (NSF), “Reclaiming Moore’s Law through Ultra Energy Efficient Computing,” $2,778,507 total with $643,700 to Blaauw, PI: Prof. David Blaauw, Co-PIs: Prof. Trevor Mudge, Prof. Dennis Sylvester, University of Michigan, Prof. Chaitali Chakrabarti, Arizona State University, Prof. David Money Harris, Harvey Mudd University, 09/2009 - 08/2014
- National Science Foundation (NSF), “Probabilistic Wearout in Nanoscale,” $300,000 with $150,000 to Blaauw, PI: Dennis Sylvester, Co-PI: David Blaauw, 08/2008 - 07/2011
- IBM Corporation/Defense Advanced Research Projects Agency (DARPA), “Strained Si/SiGe/Ge HEterojunction Tunneling Transistor (HETT) e with Steep Subthreshold Slope for Extremely Low Power Electronics,” $17,971,252 with $600,000 to Blaauw, PI: Steve Koester, Co-PI: David Blaauw, 01/2008 - 12/2009
- BAE Systems/United States Army, “Center for Objective Microelectronics and Biomimetic Adaptive Technology (COM-BAT),” $8,962,200 with $700,000 to Blaauw, PI:Kamal Sarabandi, Co-PI: David Blaauw, 5/2008 - 5/2013
- Intel Corporation, “Adaptive Digital Design in the Nanometer Regime,” $100,000, gift, 3/2008 - 3/2010
- Sun Microsystems, “Robust Low Voltage SRAM Design,” $150,000, gift, 9/2007 - 9/2010
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design,” $40,000, gift, 7/2007
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), “Elastic: An Adaptive Self-Healing Architecture for Unpredictable Silicon,” $600,000 total, PI: David Blaauw, 9/2006 - 9/2009
- Semiconductor Research Corporation (SRC), “A Design Optimization Framework for Process Variation Tolerance,” $390,000 total with $195,000 to Blaauw, PI: Dennis Sylvester, Co-PI: David Blaauw, University of Michigan, 9/2006 - 8/2009
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design” $40,000, gift, 7/2006
- Semiconductor Research Corporation (SRC), “CAD Solutions for Parametric Yield Optimization,” $321,000 total with $160,000 to Blaauw, PI Dennis Sylvester, Co-PI: David Blaauw, University of Michigan, 9/2005 - 7/2008
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design” $40,000, gift, 7/2005
- NSF Engineering Research Center (ERC) for Wireless Integrated Micro Systems (WIMS), “Subthreshold Processor Design,” PI: Kenneth Wise, University of Michigan, $60,000 to Blaauw, 5/2005 - 5/2010
- ARM, Ltd, “Low Power Computing for Embedded Applications,” $5,000,000 total, with approx. $1,600,000 to Blaauw, PI: Trevor Mudge, University of Michigan, Co-PIs: David Blaauw, Scott Mahlke, University of Michigan, 5/2005 - 5/2010

- Semiconductor Research Corporation (SRC), "Optimization of Lithographic Induced Variability for Improved Circuit Performance," $161,029, PI: David Blaauw, 9/2004 - 8/2007
- Intel Corporation, "Power Grid Integrity Analysis," $50,000, gift, 7/2004
- Photronics, Inc. $75,000, gift, 6/2004 - 5/2005
- ARM, Ltd, "Low Power Computing for Embedded Applications," $240,000 total with $60,000 to Blaauw, PI: Trevor Mudge, University of Michigan, Co-PIs: David Blaauw, Scott Mahlke and Todd Austin, University of Michigan, 5/2004 - 5/2005
- National Science Foundation (NSF), Information Technology Research (ITR), "Collaborative Research ITR: Mobile Supercomputing," $1,900,000 total with $320,603 to Blaauw, PI: Prof. Trevor Mudge, Co-PIs: Prof. David Blaauw, Prof. Todd Austin, Prof. Scott Mahlke, University of Michigan, Prof. Wayne Wolf, Princeton University, Prof. Chaitali Chakrabarti, Arizona State University, 11/2003 - 11/2007
- Intel Corporation, "VLSI Design Curriculum," $247,292 total with $61,823 to Blaauw, PI: Richard Brown, Co-PIs: Prof. David Blaauw, Prof. Michael Flynn, and Prof. Dennis Sylvester, University of Michigan, 10/2003 - 10/2004
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), "Power Aware Systems," $600,000 total, PI: David Blaauw, 9/2003 - 9/2006
- IBM Corporation, Center for Advanced Studies, "Static Performance Analysis under Process and Environment Variations," $40,000, Faculty Award, 9/2003
- Intel Corporation, "Power Grid Integrity Analysis," $50,000, gift, 7/2003
- Semiconductor Research Corporation (SRC), "Analysis and Reduction of Simultaneous Gate-Oxide Tunneling and Subthreshold Leakage Current," $360,000 total with $160,000 to Blaauw, PI: David Blaauw, Co-PI: Dennis Sylvester, University of Michigan, 7/2003 - 7/2006
- National Science Foundation (NSF), "Performance Analysis and Optimization for Nanometer Design," $375,000, PI: David Blaauw, 6/2003 - 6/2006
- ARM, Ltd, "Low Power Computing for Embedded Applications," $240,000 total with $60,000 to Blaauw, PI: Trevor Mudge, University of Michigan, Co-PIs: David Blaauw and Scott Mahlke, University of Michigan, 5/2003 - 5/2004
- IBM Corporation, Center for Advanced Studies, "Leakage Characterization and Analysis," $40,000, Faculty Award, 9/2002
- National Science Foundation (NSF), Information Technology Research (ITR), "Methodologies for Robust Design of Information Systems under Multiple Sources of Uncertainty", $1,800,00 total with $450,000 to Blaauw, PI: David Blaauw, Co-PIs: Prof. Dennis Sylvester, University of Michigan, Prof. Sachin Sapatnekar, University of Minnesota, Prof. Sarma Vrudhula, University of Arizona, 8/2002 - 8/2006
- Intel Corporation, "Power Grid Integrity Analysis," $50,000, gift, 7/2002
- MARCO/DARPA - Giga-Scale Research Center (GSRC), "Power Management for Nanometer design," $197,000, PI: David Blaauw, 10/2001 - 8/2003
- Semiconductor Research Corporation (SRC), "Variability in Chip-Level Performance and Signal Integrity Verification," $257,000, PI: David Blaauw, 10/2001 - 10/2004

IV Teaching Experience

Semester	Class	Course Number	Size	Rating (out of 5) Course/Instructor
Fall 2016	VLSI Design I	EECS 427	36	4.85/4.91
Fall 2015	Digital Integrated Circuits	EECS 312	35	4.58/4.81
Fall 2014	Advanced VLSI Design II	EECS 628	26	4.86/4.90
Winter 2014	Advanced VLSI Design	EECS 627	38	4.77/4.77
Fall 2013	VLSI Design I	EECS 427	39	4.74/4.78
Winter 2013	Introduction to Electronic Circuits	EECS 215	120	3.56/4.09
Winter 2012	Advanced VLSI Design	EECS 627	37	4.87/4.87
Fall 2011	VLSI Design I (Section 2)	EECS 427	18	4.79/4.79
Fall 2011	VLSI Design I (Section 1)	EECS 427	35	4.83/4.83
Winter 2011	Advanced VLSI Design	EECS 427	9	4.88/4.88
Fall 2010	Advanced VLSI Design II	EECS 628	19	4.81/5.00
Winter 2010	Advanced VLSI Design	EECS 627	19	4.85/4.96
Winter 2009	Advanced VLSI Design	EECS 627	23	4.75/4.75
Fall 2008	VLSI Design I	EECS 427	28	4.67/4.56
Winter 2007	Advanced VLSI Design	EECS 627	20	4.79
Fall 2006	VLSI Design I	EECS 427	31	4.89
Winter 2006	Advanced VLSI Design	EECS 627	22	4.55
Fall 2005	Topics in VLSI Design	EECS 598	12	4.25
Winter 2005	Advanced VLSI Design	EECS 627	20	4.79
Winter 2004	Advanced VLSI Design	EECS 627	35	4.59
Fall 2003	Introduction to Logic Design	EECS 270	87	4.77
Winter 2003	Advanced VLSI Design	EECS 627	36	4.61

Fall 2002	Introduction to Logic Design	EECS 270	109	4.77
Winter 2002	Advanced VLSI Design	EECS 627	40	4.31
Fall 2001	Issues in High-Performance Deep-Submicron Design	EECS 598	11	4.75

V Publications

A. Books

1. Ashish Srivastava, Dennis Sylvester and David Blaauw, Statistical Analysis and Optimization for VLSI: Timing and Power, Kluwer Academic Publishers, 2005

B. Book Chapters

1. Sechang Oh, Wanyeong Jung, Hyunsoo Ha, Jae-Yoon Sim, David Blaauw, "Energy-Efficient CDCs for Millimeter Sensor Nodes," Chapter in Efficient Sensor Interfaces, Advanced Amplifiers and Low Power RF Systems: Advances in Analog Circuit Design 2015, Springer, 2016. pp. 45-64.
2. Sechang Oh, Wanyeong Jung, Hyunsoo Ha, Jae-Yoon Sim, David Blaauw, "Energy-Efficient CDCs for Millimeter Sensor Nodes," Chapter in Advances in Analog Circuit Design, Kofi Makinwa, Andrea Baschirott, and Pieter Harpe, editors, Springer Publishing Company, 2015
3. Shidhartha Das, David Roberts, David Blaauw, David Bull, Trevor Mudge, "Architectural Techniques for Adaptive Computing", Chapter in Adaptive Techniques for Dynamic Processor Optimization: Theory and Practice, Alice Wang and Sam Naffziger, editors, Springer Publishing Company, 2008
4. David Blaauw, Sanjay Pant, Rajat Chaudhry and Rajendran Panda, "Design and Analysis of Power Supply Networks," Chapter in *Electronic Design Automation for Integrated Circuits Handbook*, Louise Sheffer, Luciano Lavagno and Grant Martin, editors, CRC Press, 2005
5. Sarvesh Kulkarni, Ashish Srivastava, Dennis Sylvester, David Blaauw, "Power Optimization Techniques using Multiple Supply Voltages," Chapter in *Closing the Power Gap between ASIC and Custom*, David Chinnery and Kurt Keutzer, editors, Kluwer Academic Publishers, 2005
6. Dongwoo Lee, Bo Zhai, David Blaauw, Dennis Sylvester, "Static Leakage Reduction through Simultaneous V_t/T_{ox} and State Assignment," Chapter in *Ultra Low-Power Electronics and Design*, Enrico Macii, editor, Kluwer Academic Publishers, 2004
7. David Blaauw, Abhijit Dharchoudhury, Rajendran Panda, "Design and Analysis of Power Distribution Networks for Processor Design," Chapter in IEEE *Design of High Performance Microprocessors Circuits*, Anantha Chandrakasan, William Bowhill, and Frank Fox, editors, IEEE Press, 2000
8. Abhijit Dharchoudhury, Shantanu Ganguly, David Blaauw, "Timing and Signal Integrity Analysis," Chapter in *Handbook for VLSI Design*, Wai Kai Chen, editor, IEEE Press, 2000

C. Invited Articles

1. Taekwang Jang, Gyouho Kim, Benjamin Kempke, Michael Henry, Nikolaos Chiotellis, Carl Pfeiffer, Dongkwun Kim, Yejoong Kim, Zhiyoong Foo, Hyeongseok Kim, Anthony Grbic, Dennis Sylvester, Hun-Seok Kim, David Wentzloff, David Blaauw, "Circuit and System Designs of Ultra-low Power Sensor Nodes with illustration in a miniaturized GNSS Logger for Position Tracking: Part I—Analog Circuit Techniques," *IEEE Transactions on Circuits and Systems I (TCAS-I)*, accepted
2. Taekwang Jang, Gyouho Kim, Benjamin Kempke, Michael Henry, Nikolaos Chiotellis, Carl Pfeiffer, Dongkwun Kim, Yejoong Kim, Zhiyoong Foo, Hyeongseok Kim, Anthony Grbic, Dennis Sylvester, Hun-Seok Kim, David Wentzloff, David Blaauw, "Circuit and System Designs of Ultra-low Power Sensor nodes with Illustration in a Miniaturized GNSS Logger for Position Tracking:

Part II—Data Communication, Energy Harvesting, Power Management and Digital Circuits," *IEEE Transactions on Circuits and Systems I (TCAS-I)*, accepted

3. Wanyeong Jung, Dennis Sylvester, David Blaauw, "Low-Power Switched-Capacitor Converter Techniques for Small IoT Systems," European Conference on Circuit Theory and Design (ECCTD), September 2017
4. Taekwang Jang, Myungjoon Choi, Yao Shi, Inhee Lee, Dennis Sylvester and David Blaauw, "Millimeter-Scale Computing Platform for Next Generation of Internet of Things," IEEE International Conference on RFID (RFID), May 2016
5. Taekwang Jang, Seokhyeon Jeong, Myungjoon Choi, Wanyeong Jung, Gyouho Kim, Yen-Po Chen, Yejoong Kim, Wootaek Lim, Dennis Sylvester, David Blaauw, "Key Building Blocks and Integration Strategy of a Miniaturized Wireless Sensor Node," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2015
6. Nathaniel Pinckney, David Blaauw, Dennis Sylvester, "Low Power Near-Threshold Design," IEEE Solid-State Circuits Magazine, June 2015
7. Inhee Lee, Yejoong Kim, Suyoung Bang, Gyouho Kim, Hyunsoo Ha, Yen-Po Chen, Dongsuk Jeon, Seokhyun Jeong, Wanyeong Jung, Mohammad Hassan Ghaed, Zhiyoong Foo, Yoonmyung Lee, Jae-Yoon Sim, Dennis Sylvester, and David Blaauw, "Circuit Techniques for Miniaturized Biomedical Sensors," IEEE Custom Integrated Circuits Conference (CICC), September 2014
8. David Blaauw, Dennis Sylvester, Prabal Dutta, Yoonmyung Lee, Inhee Lee, Sechang Bang, Yejoong Kim, Gyouho Kim, Pat Pannuto, Ye-Shang Kuo, Dongmin Yoon, Wanyeong Jung, ZhiYoong Foo, Yen-Po Chen, Seok Hyeon Jeong, Myungjoon Choi, "IoT Design Space Challenges: Circuits and Systems" 2014 IEEE Symposium on VLSI Technology, June 2014
9. Yoonmyung Lee, Dennis Sylvester, David Blaauw, "Circuits for Ultra-Low Power Millimeter-Scale Sensor Nodes," 2012 Asilomar Conference on Signals, Systems and Computers (Asilomar), November 2012
10. David Blaauw, Dennis Sylvester, Yoonmyung Lee, Inhee Lee, Suyoung Bang, Yejoong Kim, Gyouho Kim, Hassan Ghaed, "From Digital Processors to Analog Building Blocks: Enabling New Applications through Ultra-Low Voltage Design," **Invited paper** to the IEEE Subthreshold Microelectronics Conference (SubVt), Plenary Keynote, October 2012
11. Nathaniel Pinckney, Korey Sewell, Ronald Dreslinski, Dave Fick, David Blaauw, Dennis Sylvester, Trevor Mudge, "Assessing the Performance of Parallelized Near-Threshold Computing," ACM/IEEE Design Automation Conference (DAC), June 2012
12. Yoonmyung Lee, YeJoong Kim, Dongmin Yoon, David Blaauw, Dennis Sylvester, "Circuit and System Design Guidelines for Ultra-Low Power Sensor Nodes," ACM/IEEE Design Automation conference (DAC), June 2012
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203. Scott Hanson, Mingoo Seok, Dennis Sylvester, David Blaauw, "Nanometer Device Scaling in Subthreshold Circuits," ACM/Design Automation Conference (DAC), June 2007

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209. Sarvesh Kulkarni, Dennis Sylvester and David Blaauw "A Statistical Approach to Body Bias Clustering for Post-Silicon Tuning," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2006
210. Rajeev Rao, David Blaauw and Dennis Sylvester, "Soft Error Reduction in Combinational Logic Using Gate Resizing and Flip-flop Selection," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2006
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221. Amit Jain, Vladimir Zolotov, David Blaauw, "Accurate Delay Computation for Noisy Waveform Shapes," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2005
222. Sanjay Pant, David Blaauw, "Static Timing Analysis Considering Power Supply Variations," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2005

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229. David Blaauw, Kaviraj Chopra, "CAD Tools for Variation Tolerance," ACM/IEEE Design Automation Conference (DAC), June 2005

230. Eric Karl, Dennis Sylvester, David Blaauw, "Timing Error Correction Techniques for Voltage-Scalable On-Chip Memories," IEEE International Symposium on Circuits and Systems (ISCAS), May 2005

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41. David Blaauw, Tim Edwards, "Generating False Path Free Timing Graphs Using Node Splitting," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), March 1999, pg. 112-117
42. David Blaauw, "Power Management Issues in High Performance Processor Design," IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), March 1999, pg. 2
43. Daksh Lenther, Satya Pullela, David Blaauw, Shantanu Ganguly, "Hierarchical Clock-network Optimization," ACM Physical Design Workshop, April 1996, pg. 49-54
44. John Willis, Rob Newshutz, Lance Thompson, Jeff Graves, Tom Dillinger, Jeff Snyder, Nimish Radia, Joe Skovira, David Blaauw, Sidhartha Mohanty, Zhiyuan Li, Sandra Samelson, Matt Lin, "MinSim: Optimized, Compiled VHDL Simulation Using Networked & Parallel Computers," IEEE VHDL International User Forum, October 1993, pg. 137-144

G. Patents Issued

1. "Electrostatic discharge clamp circuit for ultra-low power applications," Patent number 9,716,381, issued July 25, 2017
2. "Measurement circuitry and method for measuring a clock node to output node delay of a flip-flop," Patent number 9,638,752, issued May 2, 2017
3. "Ultra Low Power Temperature Insensitive Current Source With Line and Load Regulation," Patent Number 9,639,107, issued May 2, 2017
4. "Protocol for an electronic device to receive a data packet from an external device," Patent number 9,635,147, issued April 25, 2017
5. "Integrated circuit using topology configurations," Patent Number 9,589,601 issued March 7, 2017
6. "Single Cycle Arbitration Within an Interconnect," Patent Number 9,514,074 B2 issued December 6, 2016
7. "Error recovery within integrated circuit," Patent Number 9,448,875, issued September 20, 2016
8. "Storage Device Supporting Logical Operations, Methods and Storage Medium," Patent Number 9,396,795, issued July 19, 2016.
9. "Low Power Oscillator with Charge Subtraction Scheme," Patent Number 9,385,692, July 5, 2016
10. " True random number generator," Patent Number 9,335,972, May 10, 2016
11. "Memory Circuit Including Read Voltage Boost," Patent Number 9,275,702 issued March 1, 2016
12. "Error Recovery Within Integrated Circuit," Patent Number 9,164,842 issued October 20, 2015

13. “Low Power Reference Current Generator with Tunable Temperature,” Patent Number 9147443 issued September 29, 2015
14. “Randomized Value Generation,” Patent Number 8,930,427 issued January 6, 2015
15. “Crossbar circuitry for applying an adaptive priority scheme,” Patent Number 8,868,817 issued October 21, 2014
16. “Apparatus and Method for Transferring a Data Signal Propagated Along a Bidirectional Communication Path Within a Data Processing Apparatus,” Patent Number 8,713,232 issued April 29, 2014
17. “Error Recovery Within Integrated Circuit” Patent Number 8,650,470 issued February 11, 2014
18. “Reference voltage generator having a two transistor design,” Patent Number 8,564,275 issued October 22, 2013
19. “Crossbar circuitry for applying an adaptive priority scheme and method of operation of such crossbar circuitry,” Patent Number 8,549,207 issued October 1, 2013
20. “Integrated circuit memory power supply,” Patent Number 8,526,261 issued Setember 3, 2013
21. “Vertical interconnect patterns in multi-layer integrated circuits,” Patent Number 8,381,155 issued February 19, 2013
22. “Random Number Generator,” Patent Number 8,346,832 issued January 1, 2013
23. “Cache memory system for a data processing apparatus,” Patent Number 8,335,122 issued December 18, 2012
24. “Stalling synchronization circuits in response to a late data signal,” Patent Number 8,276,014 issued September 25, 2012
25. “Crossbar circuitry for applying a pre-selection prior to arbitration between transmission requests and method of operation of such crossbar circuitry,” Patent Number 8,255,610, issued August 28, 2012
26. “Crossbar circuitry and method of operation of such crossbar,” Patent Number 8,230,152, issued July 24, 2012
27. “Single Event Upset Error Detection Within an Integrated Circuit,” Patent Number 8,185,812, issued May 22, 2012
28. “Error Recovery Within Processing Stages of an Integrated Circuit,” Patent Number 8,185,786, issued May 22, 2012
29. “Memory Cell Structure, a Memory Device Employing Such a Memo,” Patent Number 8,107,290, issued January 31, 2012
30. “Crossbar Circuitry and Method of Operation of Such Crossbar” Patent Number 8,108,585, issued on January 31, 2012
31. “Error Detection in Precharged Logic,” Patent Number 8,103,922, issued on January 24, 2012
32. “Error Detection in Precharged Logic,” Patent Number 8,006,147, issued on August 23, 2011
33. “Isolation Circuity and Method for Hiding a Power Consumption Characteristic of an Associated Processing Circuit,” Patent Number 7,880,339, issued on February 1, 2011
34. “Integrated Circuit Memory Access Mechanisms,” Patent Number 7,864,562, issued on January 4, 2011
35. “On-chip Power Supply Voltage Regulation,” Patent Number 7,839,129, issued on November 23, 2010

36. “Integrated Circuit with Error Correction Mechanisms to Offset Narrow Tolerancing,” Patent Number 7,701,204, issued on April 20, 2010
37. “Error Detection and Recovery Within Processing Statges of an Integrated Circuit,” Patent Number 7,650,551, issued on January 19, 2010
38. “Data Processor Memory Circuit,” Patent Number 7,533, 226, issued on May 12, 2009
39. “Systematic and Random Error Detection and Recovery Within Processing Stages of An Integrated Circuit,” Patent Number 7,337,356, issued on February 26, 2008
40. “Error Recovery Within Processing Stages of an Integrated Circuit,” Patent Number 7,320,091, issued on January 15, 2008
41. “Data Retention Latch Provision Within Integrated Circuits,” Patent Number 7,310,755, issued on December 18, 2007
42. “Error detection and recovery within processing stages of an integrated circuit,” Patent Number 7,278,080, issued on October 2, 2007
43. “Address Decoding,” Patent Number 7,263,015, issued on August 28, 2007
44. “Systematic and random error detection and recovery within processing stages of an integrated circuit,” Patent Number 7,162,661, issued on January 9, 2007
45. “Methods for analyzing integrated circuits and apparatus therefor,” Patent Number 7,149,674, issued on December 12, 2006
46. “Noise analysis for an integrated circuit model,” Patent Number 7,093,223, issued on August 15, 2006
47. “Memory System having Fast and Slow Data Reading Mechanisms,” Patent Number 7,072,229, issued on July 4, 2006
48. “Data Processor Memory Circuit,” Patent Number 7,055,007, issued on May 30, 2006
49. “Memory System Having Fast and Slow Data Reading Mechanisms,” Patent Number 6,944,067, issued on September 13, 2005
50. “Actively-Shielded Signal Wires,” Patent Number 6,919,619, issued on July 19, 2005
51. “Method and Apparatus for Controlling Current Demand in an Integrated Circuit”, Patent Number 6,819,538, issued on November 16, 2004
52. “Cross Coupling Delay Characterization for Integrated Circuits,” Patent Number 6,799,153, issued on September 28, 2004
53. “Iterative, Noise-Sensitive Method of Routing Semiconductor Nets,” Patent Number 6,480,998, issued on November 12, 2002
54. “Waveform Manipulation in Time Warp Simulation,” Patent Number 6,195,628, issued on February 27, 2001
55. “Optimizing Combinational Circuit Layout through Iterative Restructuring,” Patent Number 6,074,429, issued on June 13, 2000
56. “In-Transit Message Detection for Global Virtual Time Calculation in Parallel Time Warp Simulation,” Patent Number 5,956,261, issued on September 21, 1999
57. “Method for Optimizing Element Sizes in a Semiconductor Device,” Patent Number 5,903,471, issued on May 11, 1999
58. “Updating Hierarchical DAG Representations through a Bottom up Method,” Patent Number 5,790,416, issued on August 4, 1998

59. “Complementary Network Reduction for Load Modeling,” Patent Number 5,790,415, issued on August 4, 1998
60. “Simulation Corrected Sensitivity,” Patent Number 5,787,008, issued on July 28, 1998
61. “Accurate Delay Prediction Based on Multi-Model Analysis,” Patent Number 5,751,593, issued on May 12, 1998
62. “Apparatus and Method for the Automatic Determination of a Standard Library Height within an Integrated Circuit Design,” Patent Number 5,737,236, issued April 7, 1998
63. “Integrated Circuit Design and Manufacturing Method and an Apparatus for Designing an Integrated Circuit in Accordance with the Method,” Patent Number 5,689,432, issued on November 18, 1997
64. “Method and Apparatus for Designing an Integrated Circuit,” Patent Number 5,666,288, issued on September 9, 1997
65. “Logic Gate Size Optimization Process for an Integrated Circuit Whereby Circuit Speed is Improved While Circuit Areas is Optimized,” Patent Number 5,619,418, issued on April 8, 1997
66. “Message Sequence Number Control in a Virtual Time System,” Patent Number 5,617,561, issued on April 1, 1997

VI Scholarly Addresses

A. Conference Keynote Addresses and Invited Presentations

1. Invited presentation, "Low-Power Circuit Techniques for IoT Energy Harvesting," International Symposium on Quality Electronic Design (ISQED), March 2016
2. Plenary Keynote Address, "From Digital Processors to Analog Building Blocks: Enabling New Applications through Ultra-Low Voltage Design," IEEE Subthreshold Microelectronics Conference (SubVt), October 2012
3. Invited presentation, "Adaptive Sensing and Design for Reliability," IEEE International Reliability Physics Symposium, May 2010
2. Invited presentation, "Architectural Techniques for Self-Adaptive Computing," IEEE International Solid-State Circuits Conference (ISSCC), February 2007
3. Invited presentation, "Energy Optimality and Variability in Subthreshold Design," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), September 2006
4. Invited presentation, "Energy Efficient Design for Subthreshold Supply Voltage Operation," IEEE International Symposium on Circuits and Systems (ISCAS), May 2006
5. Invited presentation, "Extended Dynamic Voltage Scaling for Low Power Design," IEEE International SOC Conference, September 2004
6. Invited presentation, "Signal Integrity Issues in High Performance Design," IEEE International Workshop-Power And Timing Modeling, Optimization and Simulation (Patmos), Switzerland, September 2001
7. Invited presentation, "Inductance 101: Analysis and Design," ACM/IEEE Design Automation Conference, June 2001
8. Invited presentation, "Inductance Extraction and Modeling," ACM/IEEE Great Lakes Symposium on VLSI Design (GLSVLSI), March 2000
9. Keynote address, "Power Management Issues in High Performance Processor Design," IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), Italy, March 1999
10. Keynote address, "Industrial Perspectives on Emerging CAD Tools for Low Power Processor Design," ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 1998

B. Conference Tutorials

1. "Managing Variations Through Adaptive Design Techniques," half-day tutorial, IEEE International Solid-State Circuits Conference (ISSCC), February 2009
2. "Circuit and CAD Techniques for Low Power Design," full day tutorial with co-presenter Anantha Chandrakasan, ACM/IEEE Design Automation Conference (DAC), June 2007
3. "Future Trends and Issues in DVS," full day tutorial with co-presenters Barry Pangrle, David Flynn, David Tamura, ACM/IEEE Design Automation Conference (DAC), June 2005
4. "Leakage Issues in IC Design: Trends, Estimation, Avoidance," embedded tutorial with co-presenter Anirudh Devgan, ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2005
5. "Low Power Robust Computing," full day tutorial with co-presenters Todd Austin, Krisztián Flautner, Nam Sung Kim, Trevor Mudge, Dennis Sylvester, ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2004

6. "Standby Leakage Analysis and Optimization Methods for VLSI Design," full day tutorial with co-presenters Anirudh Devgan, Siva Narendra, Farid Najm, ACM/IEEE International Conference on Computer Aided Design (ICCAD), November 2003
7. "Design for Manufacturing in the Sub-100nm Era," full day tutorial with co-presenters Louis Scheffer, Sani Nassif, Andrzej Strojwas, ACM/IEEE Design Automation Conference (DAC), June 2003
8. "Inductance Extraction and Modeling," half-day tutorial with co-presenters Shannon Morton, Phillip Restle, Claude Gauthier, IEEE International Solid-State Circuits Conference (ISSCC), February 2002
9. "On-Chip and Package Inductance Issues," half day tutorial with co-presenter Rajendran Panda, ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2001
10. "Signal Integrity Analysis in High Performance Design," full day tutorial with co-presenters Anirudh Devgan, Abhijit Dharchoudhury, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 1999
11. "Interconnect-Driven Performance Optimization for Deep Submicron Layout Systems," full day tutorial with co-presenters Jason Cong, Ren-Song Tsay, ACM/IEEE Design Automation Conference (DAC), June 1997

C. University Lectures and Seminars Presentations

1. "Razor: Power and Reliability Trade-Offs in DVS," Invited Presentation, India Institute of Technology (IIT) Mumbay, India, December 2004
2. "Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation," Invited Seminar, University of Delft, Netherlands, August 2004
3. "Dynamic Voltage Scaling Based on Timing Speculation," Invited Presentation, University of Arizona, October 2003
4. "Statistical Analysis of Circuit Performance," Distinguished Lecture Series, University of Toronto, April 2003
5. "Signal Integrity in High Performance Design," Center for Low Power Electronic Seminar Series, University of Arizona, February 2001
6. "Deep Submicron Issues in High Performance Designs," Microsystems Technology Laboratories Seminar Series, Massachusetts Institute of Technology, October, 2000
7. "CAD Challenges for High-Performance and Low-Power Processor Designs," Electrical and Computer Engineering Graduate Seminar, University of Illinois, Urbana-Champaign, February 1999
8. "Emerging Deep Submicron Issues in Industrial Designs," Electrical and Computer Engineering Graduate Seminar, Purdue University, February 1999

D. Industrial Invited Presentations

1. "Low Voltage Circuits for Ultra Low Energy Consumption," QualCom Corporation, San Diego, CA, May, 2007
2. "Energy Efficient Computation using Low Voltage Operation," Sun MicroSystems, Santa Clara, CA, May, 2007
3. "Ultra Low Power Sensor Design using Extreme Voltage Scaling," Philips Research Laboratory, Eindhoven, Netherlands, August, 2006
4. "Low Power Sensor Design," Totoya Research Center, Detroit, MI, April, 2006

5. “Subthreshold Processor Design,” Freescale Semiconductor, Austin, TX, January 2006
6. “Computer-Aided Design Methods for Nano-meter VLSI Designs,” Intel Corporation, Strategic CAD Laboratory, Portland, OR, January 2006
7. “Advanced Circuit Design Techniques for Low-Power Design,” Intel Corporation, Circuits Research Laboratory, Portland, OR, January 2006
8. “Subthreshold Design for Low Power Sensor Processors,” ARM Ltd, Cambridge, England, December 2005.
9. “Razor: Low Power and Robust Design using DVS,” Nvidia Design Corporation, San Jose, CA, November 2005
10. “Statistical Timing Analysis: Basic Principles and State-of-the-Art,” CLK Design Automation, Boston, MA, October 2005
11. “Razor: Low Power and Robust Design using DVS,” Freescale Semiconductor, Austin, TX, October 2005
12. “Statistical Performance Analysis and Optimization,” Synopsys Inc, San Jose, CA, February 2005
13. “Circuit Analysis and Optimization Method for High-Performance Design,” Intel Strategic Computer-Aided Design Laboratory, Portland, OR, December 2004
14. “Energy efficient computation using subthreshold operation,” Intel Circuits Research Laboratory, Portland, Oregon, December 2004
15. “Razor Prototype Chip Results,” ARM Ltd, Cambridge England, September 2004
16. “Subliminal Systems, the Final Computing Frontier,” ARM Ltd, Cambridge England, September 2004
17. “Statistical Timing Analysis,” LSI Logic Corporation, May 2004
18. “Analysis and Minimization Techniques for Subthreshold and Gate Oxide Leakage Current,” Intel Circuits Research Laboratory, Portland, Oregon, January 2004
19. “Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation,” Intel Circuits Research Laboratory, Portland, Oregon, January 2004
20. “Razor: Dynamic Voltage Scaling Based on Timing Speculation,” IBM Austin Research Laboratory, Austin, Texas, October 2003
21. “Statistical Performance Analysis,” Intel Timing Verification Seminar, Portland Oregon, June 2003
22. “Leakage Analysis for High-Speed Circuits,” Intel Circuits Research Laboratory, Portland, Oregon, May 2003
23. “Statistical Timing Analysis,” Magma Design Automation, December 2003
24. “Performance Analysis of Power-Supply Noise on High-Speed Circuits,” Intel Strategic Computer-Aided Design Laboratory, Portland, Oregon, May 2003
25. “Leakage and Power Analysis for Deep-Submicron VLSI,” Texas Instruments Corp., Dallas, Texas, April 2003
26. “Performance and Power Analysis in High-Performance VLSI Designs,” Motorola Advanced Design Technology Group, Austin, Texas, February 2003
27. “Leakage Analysis and Reduction Methods,” IBM Austin Research Laboratory, Austin, Texas, February 2003
28. “Statistical Timing Analysis for VLSI Design,” IBM Design Automation Professional Interest Seminar, IBM T. J. Watson Research Center, York Town, New York, September 2002

29. “Variability in Chip-Level Performance Analysis,” Intel Performance Verification Seminar, Intel Inc., Haifa, Israel, May 2002
30. “Signal Integrity Methods for Deep Submicron Design,” Cadence Deep-Submicron Design Seminar, Cadence Berkeley Labs, Berkeley, California, December 2001
31. “Signal Integrity Issues in High-Performance Design,” Motorola Internal Conference on Signal Integrity, Austin, Texas, October 2000
32. “Circuit Analysis Techniques,” Motorola Timing Meeting, Motorola, Inc., Tel Aviv, Israel, April 2000

VII Professional Activities

A. Professional Societies

- Senior Member of the Institute of Electrical and Electronics Engineers (IEEE).
- Member of the Association of Computing Machinery (ACM).

B. Editor, Co-Editor, and Associate Editor Positions

- Associate editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), December 2003 - January 2006
- Co-guest editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), special issue on the Design Automation Conference, 2002
- Co-guest editor, *IEEE Design and Test of Computers*, special issue on the Design Automation Conference, 2002
- Co-guest editor, *IEEE Transactions on Very Large Scale Integration Systems* (*T-VLSI*), special issue on Low Power Electronics, 1999

C. Conference and Workshop Chair Positions

- Panel Chair, ACM/IEEE Design Automation Conference (DAC), 2003
- Co-Chair, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2002
- Co-Chair, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2001
- General Co-Chair, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2000
- Tutorial Chair, ACM/IEEE Design Automation Conference (DAC), 2000
- Co-Chair, technical program committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 1999

D. Consulting & Advisory Boards

- **Technical Consulting and Advisory boards**
  - Member of University of Illinois at Urbana – Champaign Advisory Panel 2013 – current
  - Gear Inc. 2013 – 2015
  - Apache Design Automation – member of advisory board
  - Nascentric, Technical Consulting, 2008
  - CLK Design Automation (CLK-DA), Technical Consulting, 2005 – 2008
- **Legal Consulting**
  - Parkins Coie LLP, 2014 – 2015
  - WilmerHale, 2012 – 2013
  - Alston & Bird, 2010 – 2011
  - Weil, Gotshal & Manges, 2008 – 2010
  - WilmerHale, 2007

- **Conference Organization**
  - Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2009
  - Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2008
  - Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2007
  - Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2007
  - Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2006
  - Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2006
  - Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2006
  - Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2005
  - Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2005
  - Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2005
  - Member, executive committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2005
  - Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2004
  - Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2004
  - Member, technical program committee, ACM Workshop on Power-Aware Computer Systems (PACS), 2004
  - Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2004
  - Member, technical program committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2004
  - Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2003
  - Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2003
  - Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2003
  - Member, technical program committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2003
  - Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2003

- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2002
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2002
- Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2002
- Member, technical program committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2002
- Member, technical program committee, ACM/IEEE Design Automation and Test in Europe Conference (DATE), 2002
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2001
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2001
- Member, technical program committee, IEEE International Conference on Computer Design (ICCD), 2001
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2000
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2000
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2000
- Member, technical program committee, IEEE International Conference on Computer Design (ICCD), 2000
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2000
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 1999
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 1999
- Member, technical program committee, IEEE International Conference on Computer Design (ICCD), 1999
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 1999
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 1998
- Member, technical program committee, IEEE International Conference on Computer Design (ICCD), 1998
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 1998
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 1997

F. Refereeing and Reviewing

- NSF, SRC, Natural Science and Engineering Research Council of Canada (NSERC)

- IEEE , IEEE T-VLSI, ACM TODAES, IEEE D&T
- DAC, ICCAD, ISLPED, ICCD, ISPD, TAU, DATE, ISCAS, ISQED, PACS