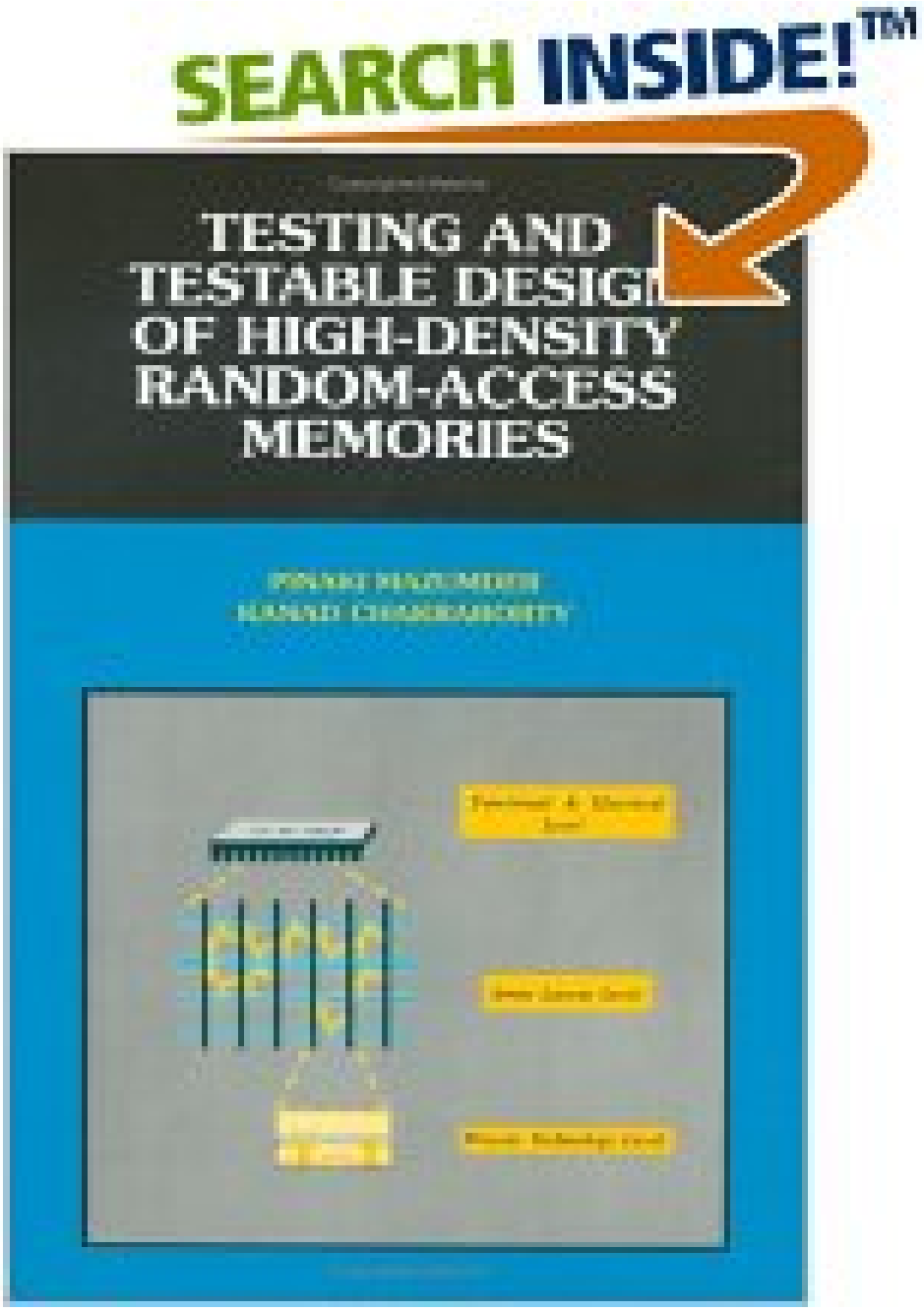

Testing and Testable Design of High-Density Random-Access Memories (Frontiers in Electronic Testing) (Hardcover)

by Pinaki Mazumder, Kanad Chakraborty "Over the last two decades, semiconductor memories have been the fastest growing market in the semiconductor industry..." (more)

Key Phrases: Texas Instruments, Inductive Fault Analysis, Perform Entry (more...)

Editorial Reviews

Book Description

Testing and Testable Design of High-Density Random-Access Memories deals with the study of fault modeling, testing and testable design of semiconductor random-access memories. It is written primarily for the practising design engineer and the manufacturer of random-access memories (RAMs) of the modern age. It provides useful exposure to state-of-the-art testing schemes and testable design approaches for RAMs. It is also useful as a supplementary text for undergraduate courses on testing and testability of RAMs. Testing and Testable Design of High-Density Random-Access Memories presents an integrated approach to state-of-the-art testing and testable design techniques for RAMs. These new techniques are being used for increasing the memory testability and for lowering the cost of test equipment. Semiconductor memories are an essential component of digital computers -- they are used as primary storage devices. They are used in almost all home electronic equipment, in hospitals and for avionics and space applications. From hand-held electronic calculators to supercomputers, we have seen generations of memories that have progressively become smaller, smarter and cheaper. For the past two decades there has been vigorous research in semiconductor memory design and testing. Such research has resulted in bringing the dynamic RAM (DRAM) to the forefront of the microelectronics industry in terms of achievable integration levels, high performance, high reliability, low power and low cost. The DRAM is regarded as the technological driver for the commercial microelectronics industry. Testing and Testable Design of High-Density Random-Access Memories deals with real- world examples that will be useful to readers. This book also provides college and university students with a systematic exposure to a wide spectrum of issues related to RAM testing and testable design.

Book Info

Presents an integrated approach to state-of-theart testing and testable design techniques for RAMs. Deals with the study of fault modeling, testing and testable design of semiconductor random access memories.