# PINAKI MAZUMDER[1]

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## I. Visa Status

U.S. Citizen (from 1995); Permanent Resident (1989-1995).

## II. Educational Qualification

| | | |
|---|---|---|
| Ph.D. in Computer Engineering | University of Illinois, Urbana-Champaign | 1987 |
| M. Sc. in Computer Science | University of Alberta, Canada | 1985 |
| B.S. in Electrical Engineering | Indian Institute of Science | 1976 |

B.Sc. in Physics Honors, First rank in the university amongst estimated 100,000 students in all disciplines.

## III. Work Experience

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| 1998- to date | Professor, Dept. of EECS, University of Michigan, Ann Arbor |
| 1996-1997 | Research Fellow at University of California, Berkeley |
| 1996-1997 | Visiting Associate Professor at Stanford University, Palo Alto |
| 1997 (Summer) | Visiting Professor at NTT Research Laboratories, Atsugi-shi, Japan |
| 1992-1998 | Tenured Associate Professor, Dept. of EECS, University of Michigan, Ann Arbor |
| 1987-1992 | Assistant Professor, Dept. of EECS, University of Michigan, Ann Arbor |
| 1982-1987 | Research Assistant, University of Illinois, and University of Alberta, Canada |
| 1985, 1986 (Summer) | Member of Technical Staff, AT&T Bell Laboratories, Indian Hill, Chicago |
| 1976-1982 | Senior Design Engineer, Bharat Electronics Ltd., India |

## IV. Research Interest

Nanocircuits, Nanoarchitectures, Modeling and Simulation Tools for Nano and Quantum Electronic Circuits; Ultra-fast Circuit Design with Compound Semiconductor Devices; Very Deep Sub-micron CMOS VLSI: Mixed Signal System Design, Testing Methodology, and Chip Layout Automation.

## V. Awards

- Fellow of IEEE, 1999 “for contributions in the field of VLSI”
- Digital Equipment Corporation Faculty Award: Excellence in Research
- Departmental Research Excellence Award (1995), The University of Michigan
- BF Goodrich National Collegiate Invention Award
- DARPA Research Excellence Award for the work in Quantum MOS Project
- Best Undergraduate Student Medal
- IETE Best Student Paper Award, and IETE Best Paper Presentation Award
- NSF Research Initiation Award
- Bell Northern Research Laboratory Faculty Development Grant
- Commendation Letter from the Dean of College of Engineering, University of Michigan, for Excellence in Teaching

[1] Fellow of IEEE, Member of Sigma Xi, and Member of Phi Kappa Phi

- US Patent on Digital Logic Design Using Negative Differential Resistance Diodes and Field-Effect Transistors, US Patent No. 5903170, awarded on May 11, 1999.
- US Patent on High-speed, Compact, Edge-Triggered Flip-Flop Circuit Topologies Using NDR Diodes and FET's, US Patent No. 6,323,709, awarded on Nov. 21, 2001.
- US and International Patents on Method and Apparatus to Improve Noise Tolerance of Dynamic Circuits, US Patent No. 7,088,143, awarded on Aug. 8, 2006.

## VI. Research Funding

1. National Science Foundation (RIA): $69,948; Sept. 1988 - Aug. 1991
2. Bell Northern Research Laboratory: $20,900; Nov. 1988 - Aug. 1989
3. National Science Foundation: $90,620; Aug. 1989 - July 1990
4. Digital Equipment Corporation: $180,000; Sept. 1989 - Aug. 1992
5. Office of Naval Research: $420,000; Sept. 1988 - Aug. 1991, shared with Prof. K.G. Shin (PI) & Dr. C. Ravishankar
6. National Science Foundation: $125,000; Jan. 1991 - Dec. 1993
7. Rackham Faculty Research Grant: $9,980; June 1991 - May 1993
8. U.R.I. Program (US Army): $250,000 (my portion); Jan. 1988 - Dec. 1992
9. General Motors: $20,000; May 1992 - Dec. 1992
10. International Business Machines: $45,000 (student fellowship); Sept. 1990 - Aug.1993
11. National Science Foundation: $47,000; Sept. 1992 - Dec. 1993
12. Hewlett Packard: $81,400; Jan. 1993 - Dec. 1995
13. Office of Vice President Research: $52,300; Mar. 1995 - Feb. 1996
14. Defense Advanced Research Projects Agency (DARPA): $825,000; May 1993 - Jan. 1997, shared with Prof. George I. Haddad (PI)
15. National Science Foundation: $182,400; Mar. 1994 - Feb. 1998
16. U.R.I. Program (US Army): $150,000; Jan. 1993 - June 1997
17. State of Michigan (through DTM Center): $200,000; July 1995 - June 1998
18. Texas Instruments (subcontract of a DARPA project): $304,000; June 1995 - May 1998
19. Army Research Office's MURI-95 (Co-PI with 7 others): $4,000,000; 1995-2000 + 1 year.
20. Army Research Office's MURI-96 (Co-PI with 13 others): $5,000,000; 1996-2001 + 1 year.
21. Defense Advanced Research Projects Agency: $750,000; June 1997- May 2000 (Co-PIs: Prof. G. I. Haddad and Dr. J. East)
22. National Science Foundation: $300,000; June 2002
23. Nippon Electric Company, Japan: $40,000;
24. National Science Foundation: $195,000; June 2002
25. Hughes Research Laboratory (subcontract of an Office of Naval Research project); $270,000; 1998-2001
26. NanoLogic Inc. $10,000;
27. Air Force Office of Scientific Research: $5,000,000: 2001-2006 (Co-PI with 10 other investigators, my portion is $450,000)
28. Naval Research Laboratory: $303,000: 2001-2002; (PI)
29. National Science Foundation: $210,000: 2001-2004
30. Korean Government Nanoelectronics Research: $200,000: 2001-2002 (PI: G.I. Haddad).
31. Naval Research Laboratory: $820,000: 2002-2005; (PI)
32. Tera-Level Nanoelectronics Project, Korean Government: $170,000: 2003-2006; (PI)
33. National Science Foundation: $120,000: 2004-2007
34. National Science Foundation, Nanoelectronics Interdisciplinary Research Teams (NIRT): $240,000: 2005-2008
35. Air Force Office of Scientific Research, Plasmonics Applications in VLSI: $480,000: 2006-2009

### Pending Grants

1. DARPA (PI), About $1,000,000 (for 3 years)
2. DARPA (PI), About $1,000,000 (for 3 years)
3. NSF ITR 2004 (PI with 4 Co-PI's), About $200,000 (for 4 years)
4. NSF (CISE program) (PI), About $300,000 (for 3 years)
5. NSF (ECS program) (PI), About $300,000 (for 3 years)

## VII. Consulting and Industrial Interactions

***Past Advisory Board Member***: 1. Sequence Design Automation, 2. Silicon Value Inc., 3. NanoLogic, Inc.; ***Advisor and Expert Witness***: in lawsuits involving circuit designs of DRAM and SRAM chips. ***Technical Consultant***: Served as technical consultant for many semiconductor companies in the following areas: testable and self-repairable designs of embedded cache memories, soft-error problems in FPGA's, circuit design for spread-spectrum communications, AMLCD display hardware, nanoelectronic circuits and simulation tools.

## VIII. Committees and Professional Activities

1. Member of Board of Editors, *Proceedings of the IEEE*
2. Associate Editor, *IEEE Transactions on VLSI Systems*, 1997-2000
3. Guest Editor, *IEEE Transactions on VLSI Systems* - A Special Issue on Impact of Emerging Technologies on VLSI Systems, December 1997
4. Guest Editor (with Dr. A. Seabaugh), *Proceedings of the IEEE* - A Special Issue on Nanoelectronic Devices and Circuits, June 1998
5. Guest Editor, *Journal of Electronic Testing - Theory and Application* - A Special Issue on Multi-megabit Memory Testing, April 1994
6. Guest Editor (with Prof. J.P. Hayes), *IEEE Design & Test Magazine* - A Special Issue on Memory Testing, 1993
7. Editorial Advisory Board, *The Arabian Journal for Science and Engineering*, King Fahd University of Petroleum and Minerals, Saudi Arabia.
8. Council of Editors, *International Society for Genetic and Evolutionary Computation* (ISGEC)
9. Member, NSF Research Initiation Awards Selection Panel, 1991
10. Member, NSF Career Award Panel, 1998
11. Member, NSF ITR Panel, 2001
12. Member, NSF Career Award Panel, 2004
13. Member, NSF Career Award Panel, 2005
14. Member, NSF Engineering Panel, 2006
15. Member, SACUA Research Policies Committee of Senate Assembly, 2002-2205.
16. Member, Electrical Engineering and Computer Science Curriculum Committee, 2002-2003.
17. Member, Electrical Engineering and Computer Science DCO Committee, 2002-2003.
18. Member, Computer Science and Engineering Graduate Curriculum Committee, 1988-89, 1998-2000, 2002-.
19. Counselor, Computer Engineering Undergraduate Students, 1990-94
20. Member, Computer Science and Engineering Graduate Admission Committee, 1995-96
21. Member, IEEE Standards Subcommittee for Semiconductor Memories, 1989-90
22. Member, IEEE Test Technologies Committee
23. Member, IEEE VLSI Technical Committee
24. Program Chair, 1999 IEEE Great Lakes VLSI Conference
25. Program Committee, 1992 Fault-Tolerant Computing Symposium Workshop
26. Program Committee, 1992 IEEE Defects and Fault Tolerance Workshop
27. Program Committee, 1993 IEEE Intl. Conference on Memory Testing
28. Program Committee, 1994 IEEE Intl. Conference on Memory Testing
29. Program Committee, 1994 IEEE Asian Testing Symposium
30. Program Committee, 2000 IEEE Great Lakes VLSI Conference
31. Proposals Reviewed for: US National Science Foundation, The Israel Science Foundation, Louisiana University Board of Regents, and US Army Research Office, New Jersey Center for Science and Technology.

## IX. Professional Experience

### *Industrial Experience* (6.5 years)

During the summers of 1985 and 1986, I worked as a Member of Technical Staff at AT&T Bell Laboratories. I was one of the three engineers who started Bell Lab's *CONES/SPRUCE* project - a new behavioral synthesis and layout automation tool for rapid prototyping of digital circuits.

During 1976-1982, I worked as a Senior Design Engineer at Bharat Electronics Ltd. (a collaborator of RCA/GE) in its Integrated Circuits Division. Primarily I worked as a computer-aided design (CAD) and application engineer. I was involved in the design and fabrication of a number of analog and digital integrated circuits using both bipolar and CMOS technologies. Was responsible for leading a team of CAD and application engineers in the following IC development projects: i) ICs for raster-scan vertical deflection systems, ii) ICs for sync processing and horizontal deflection systems, iii) ICs for high-gain pre-amplifiers with automatic gain adjustments, iv) Video and audio IF stages ICs for vestigial-AM and FM signal detection and amplification, v) LCD and AC Plasma display drive ICs. Over 100 million commercial chips were fabricated based on my design works.

### *Teaching Experience* (19 years)

Currently I am working as a Professor at the Department of Electrical Engineering and Computer Science of the University of Michigan, Ann Arbor, Michigan.

Graduate courses developed/taught: 1) Optimization and Synthesis of VLSI Layout, 2) Testing of Digital Circuits and Systems, 3) Advanced Computer Architectures, and 4) Nanocircuits and Nanoarchitectures.

Undergraduate courses upgraded/taught: 1) Digital Logic Design, 2) Digital Integrated Circuit Design, 3) VLSI System Design, and 4) Nanocircuits and Nanoarachitectures for Undergraduate Students.

### *Student Theses Supervised*

*Ph.D. Theses Completed*

1. J. Yih, "Built-In Self-Repair of Embedded Memory and Logic Arrays," 1990. Currently at IBM T. J. Watson Research Center, Yorktown, New York.

2. K. Shahookar, "Genetic Algorithms for CAD Layout Problems," 1994. Currently at his start-up company.

3. H. Esbensen, "Application of Genetic Algorithms for Cell Placement and Routing Problems," 1994. Currently at Avant! Fremont, California.

4. V. Ramachandran, "Parallel Architectures for Multilayer Wire Routing Problems," 1994. Currently at Cadence Design Systems, San Jose, California.

5. S. Mohan, "Design of Ultra-fast Digital Circuits using Quantum Electronic Devices," Dec. 1994. Currently at Xilinx Corporation, Campbell, California.

6. K. Chakraborty, "Built-In Self-Repairable RAM Compiler Design," Mar. 1997. Currently at Agere Design, Murray Hills, New Jersey.

7. M. Bhattacharya, "Simulation and Emulation of Digital Integrated Circuits Containing Resonant Tunneling Diodes," Oct 1999. Currently at Avant! Fremont, California.

8. S. Kulkarni, "Quantum MOS Circuits and Systems," Oct 1999. Working in IDT, Atlanta, Georgia.

9. A. Gonzalez, ”Multiple-Valued Logic and High-Speed Digital Circuits Using Resonant Tunneling Diodes,” June 2001. Currently at IDT, Atlanta, Georgia.

10. Li Ding, “ Dynamic Noise Analysis in Deep Sub-micron CMOS VLSI Systems,” Feb. 2004. Currently at Synopsis, Sunnyvale, California.

11. Q. W. Xu, “Accurate Interconnect Modeling for Efficient Transient Simulation in VLSI Chip Design,” May 2006, currently at Cadence Design Systems.

*M.S. Theses/Projects Completed:*

1. B. Brighton, Pseudo-Random Testing for Embedded Memories
2. K. Quasim, Analog Circuit Testing
3. J. Kapson, Parallel CAD Architecture
4. D. Berryman, Parallel Processing for VLSI Routing
5. M. Smith, Self-Repairable Memory Array Using Digital Neural Circuit
6. E. Chan, RTD-based Multi-valued Circuit Design
7. A. Arunachalam, Fine-Grained Parallel Routing
8. A. Gonzalez, Multi-valued Adder Design Using CMOS and RTD
9. A. Gupta, Self-Repairable ROM Generator
10. J. Xiong, Quantum MOS Circuit Design
11. G. Mittal, Simultaneous Switching Noise Analysis in Embedded Memories
12. V. Warraich, Web-based Applets Design for Digital Logic
13. M. Kumshikar, Amorphous TFT-based Driver Logic Design for AMLCD Panel
14. G. Shankar, Amorphous TFT-based Operational Amplifier Design for AMLCD Panel
15. V. Ramachandran, Array Machine for VLSI Routing
16. S. Mohan, Parametric Testing for SRAM’s Using GaAs High Electron Mobility Transistors
17. S. Kulkarni, CMOS and RTD-based Correlators Design
18. K. Shahookar, Genetic Algorithm for VLSI Placement
19. H. Chan, Macro-cell Placement Using Genetic Algorithm
20. L. Ding, Noises in Deep Sub-micron VLSI Chips
21. Q. W. Xu, VLSI Interconnect Modeling Using Differential Quadrature Method
22. B. Wang, 3-Dimensional Full Chip Simulation by Transmission Line Matrix Method
23. H. Zhang, Ultra-fast RTD-based Circuit Design.
24. S.R. Li, RTD-based Cellular Nonlinear Networks
25. D. Shi, Quantum Dot Based Image Processing
26. M. Rajagopal, Modeling of Resonant tunneling Diodes
27. W. Lee, Image Processing Applications of Quantum Dots

*Number of Doctoral Students Currently Being Supervised:* 6.
*Visitors:*

1. Dr. Ueymura, NEC, Japan;

2. Prof. Choi, Hanyang University, South Korea;

3. Mr. T. Glotzner, Germany;

4. Mr. H. Esbensen, Aarhus University, Denmark.;

5. Dr. Q. W. Xu, China;

6. Mr. P. Kelly, Ulster University, UK;

7. J. P. Sun, China

## X. Research Projects

I have been conducting research on ***six*** aspects of VLSI system design: i**) Nanoelectronic Circuits**: **Modeling, Simulation and Applications**, ii) **Quantum MOS circuit and CAD tools**, iii)**Very deep submicron CMOS design**, iv) **Random-access memories testing and fault-tolerance**, v) **Self-repairable VLSI design techniques**, vi) **Layout automation of high-performance VLSI chips.**

- **Nanoelectronic Circuits Using Quantum Dots:** Modeling of I-V characteristics using Schrödinger equation and scattering matrix; Image processing with self-assembled array of quantum dots. (2002 --- i.e., sarted in 2002 and continuing)

- **Nanoelectronic Circuits Using Mesoscopic Quantum MOS:** Visual computing by Cellular Nonlinear Networks consisting of ensemble of Q-MOS cells: hardware and algorithms. (2001--)

- **RTD-based High-speed Circuits:** Nanopipelined high-speed (60 GHz and above) communication circuits using resonant tunneling devices. (1994 ---)

- **Very Deep Submicron CMOS Circuits and Design Methodology:** Optimal adiabatic low-power CMOS circuit design, Optimal transistor sizing for high-speed CMOS design, CMOS dynamic noise modeling, Interconnect noise modeling, Simultaneous switching noise modeling, Methodology for fast detection of noise violation in SoC/VLSI, etc. (1998 ---)

- **Simultion Tool for Nanoelectronics:** Augmented SPICE simulator (QSPICE) design for quantum and other non-linear devices. (1994 ---)

- **Simulation Tool for RTD-based Ultra-fast Circuits:** 3-Dimensional full chip simulation tool design for high-speed circuits by using Transmission Line Matrix (TLM) method. (1998 -- )

- **Interconnect Delay Modeling:** High-speed interconnect delay modeling in VLSI chips by using Differential Quadrature methods that converge faster than Finite Difference methods. (1999 ---)

- **EMI Effects on VLSI Chips:** Krylov subspace solver and Green's function solver for VLSI chip design simulation. An EMI full-chip simulation tool is built for estimating delay and thermal failures in VLSI chips due to electromagnetic interferences (EMI). This research will lead to the development of nanometric FET models that will require solving Schrodinger equation, Poisson equntion and Maxwell's equations to derive the device charcateristics. (2000 ---)

- **Semiconductor Memory Testing:** Testing algorithms for high-density silicon DRAM's and SRAM's; built-in self-testing; random pattern testing, error correction; memory chip yield; failure diagnosis. (1985 --)

- **Self-Healing Techniques for VLSI Chips:** Silicon compilers for RAM, ROM, PLA, etc. with built-in self-repair capabilities; self-repairable processor, systolic and cellular arrays. (1989 --)

- **VLSI Layout SynthesisTools:** Distributed layout tools using genetic algorithms for concurrently running on a network of workstations– partitioning, placement, routing, floorplnning, etc. (1988-96)

- **Hardware Accelerator for VLSI Routing:** Polymorphic array architecture for unified parallel routing to describe maze, channel, switchbox, and area connectivities; Design of a routing chip using polymorphic array architecture; HAM: Multilyer maze router using hexagonal array machine. (1988-95).

- **VLSI Data-structures:** General theory of planar tessellations on triangular and quadrilateral lattices yielding quad-tree data-structures and their applications in VLSI layout synthesis and gridded image processing (1985—1989).

## VLSI Circuit Design

This research is supported by: DARPA, Army Research Office, National Science Foundation, Office of Naval Research, Air Force Scientific Research Office, Hughes Research Laboratory, Nippon Electric Company, and Texas Instruments/Raytheon TI Systems.

Research activities include: a) Low Power CMOS Circuit Design, b) Circuit Analysis Techniques Using Accurate Short-Channel Models, c) High-Speed CMOS Circuit Design, d) Mixed Analog and Digital Systems Design, e) Modeling of Failures in RAM's, ROM's, and PLA's due to EM Pulses, f) Estimation of EMI Effects on Digital VLSI Chips, g) Modeling of Simultaneous Switching Noise in Very Deep Sub-micron Design, h) Modeling of Cross-talk Noise in Very Deep Sub-micron Design, I) Modeling of Transient Noise such as Glitches in Very Deep Sub-micron Design, j) Modeling of Quantum Dots and Image Processing with QD Array, k) Visual Computing with Quantum MOS Circuits, l) Quantum MOS Circuit Design Using Tunneling Devices and CMOS, m) Spice Simulator for Quantum Circuits, n) DQM and Modified Method of Characteristics Based Interconnect Delay Modeling of Lossy Transmission Lines, o) DQM based RC Interconnect Modeling and Reduction Algorithms, p) Variable-mesh Electromagnetic-based Device and Integrated Circuit Simulator (VEDICS) for Accurate Simulation of High-speed Circuits.

The focus of the above research activities is to develop *core* competence in VLSI circuit design by combining disparate technical skills in various fields of circuit design, EM theory, quantum Physics and accompanying CAD tools that are required to design low-power and high-speed circuits. We have designed several patented circuit topologies

## VLSI Testing and Reliable Design

Research supported by: NSF and Army Research Office. Research projects include: a) Testing of High-Density Silicon Semiconductor Memories, b) Silicon Compilers with Built-In Self-Testing and Self-Repair Capabilities for Embedded Memory and Programmable Logic Arrays, c) Testing and Diagnosis of Deep Sub-micron VLSI Chips.

The focus of the above research activities is to characterize and model previously non-encountered obfuscating faults that mostly manifest due to technological parametric variations in new sub-micron VLSI fabrication technologies, and to design *novel* and efficient test and diagnosis algorithms that can detect those faults, in addition to conventional functional faults. In multimillion transistor VLSI chips, where deeply embedded components cannot be tested external to the chip, built-in self-testing circuits are being designed to test those components comprehensively, as well as new self-repair hardware are being designed to restructure the chip automatically so that faulty chips can repair themselves. The two aspects of this research are: to improve the chip manufacturability by improving the yield, and to ameliorate the survivability of the system due to on-line self-repair.

## VLSI Layout Automation

Research supported by: DEC, GM, IBM, BNR, NSF. Research projects include: a) Distributed Layout Tools for VLSI Design: Partitioning, Floorplanning, Placement and Routing of Standard Cell, Macro-cell, and Sea-of-gates styles of VLSI layouts, b) CADIVA: A Layout Critiquing Tool that Automatically Refines a Chip Layout for Minimizing Process Related Defects and Helps Increase Chip Yield and Reliability.

The goal of this research is to develop a suite of distributed layout tools by employing the genetic algorithm (GA) as a core parallel search technique. The GA accomplishes combinatorial optimization of a physical system by applying biological operators, namely crossover, mutation and inversion, on the genotype, a chromosomal string representation of the problem and by improving the objective function iteratively over numerous generations. Whereas conventional deterministic and stochastic optimization techniques perform sequentially, the GA's intrinsic parallelism in its problem solving strategy can be harnessed to efficiently coordinate the parallel search process over a network of workstations by paying very small communication overhead. At present, very little is understood about the convergence mechanism of the GA or the quality of solution it can potentially accomplish, unless appropriate quasi-mathematical models are designed through a combination of stochastic analysis and inference of empirical results. The intent of this research is to develop this theoretical framework through the design and usage of distributed layout tools.

## Software Developed by NDR Research Group

- ***Q-SPICE***: A Spice-based circuit simulator for two and three terminal CMOS, GaAs, InP and GaSb devices with negative differential resistance characteristics such as RTD, RTT and RHET. New homotopy based convergence algorithms were developed to improve DC convergence of RTD based nonlinear circuits that regular SPICE program fails to simulate

- ***VEDICS***: Variable-mesh Electromagnetic Device and IC simulator, a full-chip detail simulator for estimating circuit performance at high speed. It uses transmission line matrix method to solve Maxwell-like wave equations and thereby VEDICS can account for reflections, scattering and inductive effects in a VLSI chip.

- ***DQM Timing Tool***: A Differential Quadrature Method based interconnect delay modeling tool has been developed t estimate signal delays through non-uniform multiple interconnects having parasitic capacitances and mutual inductances

- ***BISRRAMGEN***: A VLSI compiler for automatic generation of embedded byte-oriented memories with built-in self-testing and self-repair capabilities

- ***RTD Modeling Tools***: Envelope function based RTD modeling tool that is used in optimizing RTD structures along with Q-Spice.

- ***Quantum Dot Modeling Tool***: This tool solves Three-Dimensional the Schrödinger equation and the Poisson equation self-consistently to model tunneling currents in pyramidal quantum dots.

- ***Thermal Simulator***: This Green function solver can estimate thermal distribution in a 3-D CMOS VLSI chip with multiple active layers.

- ***Wolverines***: Genetic algorithm based VLSI standard cell layout generation tool that runs concurrently on distributed workstations to search in parallel near optimal layout solutions. The GA-based tool also utilized a meta genetic process to select various parameters like crossover rate, mutation rate, population size, etc. by using a second-level GA technique.

- ***QECDOE***: Quantum Electronic Circuit Design Optimization Environment is a tool that is utilized to optimize circuit-level electrical parameters like power consumption, speed, noise margin, etc. by optimizing both two dimensional transistor areas and three-dimensional structures of mesoscopic devices such as quantum wells in RTD's.

## XI. Main Accomplishments and Contributions

### Industrial R&D Experience

- Worked 6 years in industrial R&D laboratories. Designed analog and digital integrated circuits (went into production for over 100 million pieces) and developed the first C-language based EDA synthesis tool (Cones) at AT&T Bell Labs, Indian Hill, Chicago.

### Research Accomplishments in Semiconductor Memories

- Invented a new testable memory circuit to perform multiple-cell, line-mode testing, a method that is now used in all DRAM chips in order to reduce memory chip testing cost by two orders of magnitude. Recently, two German and some international patents on testable memory design, issued after the publication of my papers on memory testing, have been annulled because my invention predated those patents owned by Siemens, Toshiba, Samsung, etc.
- Proposed layout and process based parallel test algorithms that are now widely used by memory manufacturers in testing mega- and giga-bit DRAM and SRAM chips.
- Identified the mechanism of double-bit errors due to alpha particles striking between trench DRAM cells, and proposed a new on-chip double-bit error correcting circuit that improves memory storage reliability by million times.

### Research Accomplishments in Self-Repair of VLSI chips

- Proposed for the first time a class of self-repair techniques for various VLSI memories.
- Developed a unified approach to Built-in Self-repair of VLSI chips by proposing pseudo-analog adaptive network of threshold elements that can perform combinatorial optimization algorithms such as maximum matching and node covering on bipartite graphs. These area-efficient and accurate hardware algorithmic techniques are key to automatic repair of VLSI chips.

### Research Accomplishments in Quantum MOS and High-speed Circuits

- Accurate Modeling of RTD's and Quantum Dots; Circuit applications of quantum dots and RTD's.
- Developed several new circuit configurations that employ quantum-effect devices to improve speed and reduce power consumption of integrated circuits.
- Augmented Spice program to incorporate a number of quantum-effect devices and developed homotopy based new routines for enhancing DC and Transient convergences encountered in simulating highly nonlinear circuits having multiple DC solutions.
- Developed Differential Quadrature Method based interconnect modeling techniques and combined the wiring model with Spice.
- Developed Finite Difference Quadrature Method for modeling the signal integrity in a VLSI chip in presence of electromagnetic waves emanated from on-chip and external sources
- Developed noise modeling techniques for SoC and designed new noise-aware design techniques.

### Research Accomplishments in VLSI Layouts

- Developed a suite of distributed layout tools to demonstrate capabilities of Genetic Algorithms for solving placement, partitioning, floor-planning, and routing problems on a network of workstations (NOW).
- Developed a suite of layout critique tools that can automatically optimize a finished a layout to reduce manufacturing defects occurring randomly at various process steps.
- Developed a unified parallel VLSI chip routing method by using an ensemble of polymorphic processing elements which can improve the speed by an order of magnitude for a wide class of chip routing styles like maze, channel, switch-box, area, and so on.

## XII. Publications

### Books and Book Chapters

#### Authored Text Book

1. P. Mazumder and K. Chakraborty, "Testing and Testable Design of Random-Access Memories", ***Kluwer Academic Publishers***, 1996 (428 pages).

2. P. Mazumder and E. Rudnick, "Genetic Algorithms for VLSI Layout and Test Automation", ***Prentice Hall***, 1999 (460 pages).

3. K. Chakraborty and P. Mazumder, "Fault Tolerance and Reliability Aspects of Random-Access Memories," ***Prentice Hall***, 2002. (440 pages)

4. P. Mazumder, "Introduction to Digital Systems", Video Book on DVD, produced at MGM Studio (Orlando, Florida), ***Laureate Education, Inc.,*** 2005.

5. P. Mazumder, "Models and Techniques for VLSI Routing", ***Springer Verlag***, (under preparation)

6. R. Rajasuman (Editor) and P. Mazumder (Editor), "Semiconductor Memories: Testing and Reliability", ***Computer Science Press***, May 1998.

7. R. J. Lomax (Editor) and P. Mazumder (Editor), "Great Lakes Symposium on VLSI, 1999", ***Computer Science Press***, March 1999.

### Text Book Chapter

8. K. Shahookar and P. Mazumder, "Standard Cell Placement and the Genetic Algorithm", Book chapter in "Advances in Computer-Aided Engineering Design, Vol. II", I. N. Hajj (editor), ***Jai Press***, Greenwich, Connecticut, 1990, pp. 159-234.

9. W. K. Fuchs, M. F. Chang, S. Y. Kuo, P. Mazumder and C. B. Stunkel, "The Impact of Parallel Architecture Granularity on Yield", Book chapter in "Designing for Yield," Moore, Strowjas and Maly (editors), ***Adam Hilger Publisher***, 1988.

10. P. Mazumder and J. H. Patel, "Parallel Testing of Parametric Faults in DRAM", in "Advanced Research in VLSI: Design and Applications of Very Large Scale Systems", Leighton and Allen (editors***), MIT Press***, 1988. (Presented at the 5-th Massachusetts Institute of Technology Conference on VLSI).

11. P. Mazumder, "Design of a Fault-Tolerant DRAM with New On-Chip ECC", Book Chapter in "Defects and Fault Tolerance in VLSI Systems", I. Koren (editor), ***Plenum Press***, 1989.

12. H. Chan and P. Mazumder, "A Systolic Architecture for High-Speed Hyper-graph Partitioning Using a Genetic Algorithm", Book Chapter in "Progress in Evolutionary Computation", Vol. 956***, Springer- Verlag***, Heildelberg, 1995, pp. 109-126.

### Reviewed Journal Publications

13. P. Mazumder, J. H. Patel and W. K. Fuchs, "Methodologies for Testing Embedded Content-Addressable Memories", ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, Jan. 1988, pp. 11-20.

14. P. Mazumder, "Parallel Testing of Parametric Faults in a Three-Dimensional Dynamic Random-Access Memory", ***IEEE Journal of Solid-State Circuits***, Vol. 23, No. 4, Aug. 1988, pp. 933-942.

15. P. Mazumder and J. H. Patel, "Parallel Testing of Pattern-Sensitive Faults in Random-Access Memory", ***IEEE Transactions on Computers,*** Vol. 38, No 3, Mar. 1989, pp. 394-404.
16. P. Mazumder and J. H. Patel, "An Efficient Built-In Self-Testing Algorithm for Random-Access Memory", ***IEEE Transactions on Industrial Electronics*** (Special Issue on Testing) Vol. 36, No. 3, May 1989, pp. 394-407.

17. J. S. Yih and P. Mazumder, "Circuit Behavior Modeling and Compact Testing Performance Evaluation", ***IEEE Journal of Solid-State Circuits***, Vol. 26, No. 1, Jan. 1991, pp. 62-65.

18. P. Mazumder and J. H. Patel, "A Comprehensive Study of Random Testing for Embedded RAM's Using Markov Chains", ***Journal of Electronic Testing: Theory and Applications***, Vol. 3 No. 4, Nov. 1992, 235-250.

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84. Q.W. Xu and P. Mazumder, "Rational ABCD matrix of high-speed interconnect using differential quadrature method," ***IEEE Transactions on VLSI Systems.***

85. H. Esbensen and P. Mazumder, "SAGA: Unification of Genetic Algorithm with Simulated Annealing and Its Application to Macro-Cell Placement," ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, (will be accepted pending some changes).

86. K. Chakraborty and P. Mazumder, "An Efficient, Bus-layout Based Method for Early Diagnosis of Bussed Driver Shorts in Printed Circuit Boards***," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***.*

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94. T. Ueymura, P. Mazumder and L. O. Chua, "Rise Time Analysis of RTD Based Mono-stable to Bi-stable Transition Circuits," ***IEEE Transactions on Circuits and Systems***.

95. L. Ding and P. Mazumder, "Low Power Edge Triggered Flip Flop Design," ***IEEE Journal of Solid-State circuits.***

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98. S. R. Li, P. Mazumder and L. O. Chua, "Design Techniques of RTD-based Cellular Nonlinear Network for Image Processing," ***IEEE Transactions on Nanotechnology.***

99. K. Song and P. Mazumder, "Modeling of Plasmonics Interconnect," ***IEEE Transactions on Nanotechnology.***

100. W. Lee and P. Mazumder, "Color Image Processing by Quantum Dots," ***IEEE Transactions on Nanotechnology.***

## Rigorously Reviewed Conference Publications

**(Generally these conferences have acceptance ratio between 15% and 35% and they require rigorous review of full paper before the decision on a paper is made. The following papers are mostly 4 or more published pages in the proceedings).**

101. P. Mazumder, J. H. Patel and W. K. Fuchs, "Design and Algorithms for Parallel Testing of Random-Access and Content-Addressable Memory," ***Proceedings ACM/IEEE 24th Design Automation Conference,*** Florida, Jun. 1987, pp. 688-694 (nominated for the Best Paper Award).

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138. G.I. Haddad and P. Mazumder, "Resonant Tunneling Devices and Their Applications," ***Proceedings on IEEE Symposium of Heterostructure Devices***, Sapporo, Japan, Aug. 1996. (**Invited**)

139. P. Mazumder, "Multi-valued Logic Design Using HBT's and RTD's," ***Proceedings on Frontiers in Electronics***, Tenerife, Spain, Jan. 1997. (**Invited**).

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## Workshop Presentations

237. Mazumder, P.,"Quantum circuits and CAD tools design ," ***Proceedings on SRC Nanoelectronics Symposium*** , Aug. 2005. **(Invited)**

238. P. Mazumder, "Q-MOS Circuit Design Techniques and Future Prospects of Q-MOS," ***SRC Nanoelectronic Workshop***, Dec. 1999. Raytheon-TI, Dallas, Apr. 1998. (**Invited**).

239. P. Mazumder, "Visual Computing by Mesoscopic and Nanoscale Systems," ***National Nanoelectronics Initiative Workshop***, Organized Jointly by NNCO, NSF, ONR, AFOSR and DARPA, February 2004. (**Invited**)

240. P. Mazumder, "Quantum Dot Based Cellular Image Processing: Theory and design," ***IEEE Workshop on Cellular Nonlinear Networks***, July, Budapest, Hungary (**Invited**).

241. P. Mazumder, "Design of a Fault-Tolerant DRAM with New On-Chip ECC," ***IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems,*** Oct. 1988, Springfield, Massachusetts.

242. P. Mazumder, "A Test Methodology for Electronic Neural-Network Associative Memory***," International Neural Network Society First Annual Meeting***, Sep. 1988, Boston, Massachusetts.

243. P. Mazumder, "Effects of HPEM and UWB Pulses on a System-on-a-Chip Digital Circuits," ***MURI Workshop on EM Effects on Electronic Circuits,*** Chicago, November 2003.

244. P. Mazumder, "Study of Signal integrity in VLSI Chips in Presence of High-Power Electromagnetic Pulses, "***MURI Workshop on EM Effects on Electronic Circuits,*** Chicago, January 2003.

245. P. Mazumder, "Hexagonal Mesh Architecture for Routing," ***Office of Naval Research Workshop***, Washington, Nov. 1989.

246. P. Mazumder, "Hexagonal Mesh Reconfiguration Algorithms," ***Office of Naval Research Workshop***, Washington, Nov. 1990.

247. P. Mazumder, "Ultra-fast Circuit Design with NDR Devices," ***Advanced Research Project Agency: Ultra Project***, Santa Fe, Oct. 1993.

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251. P. Mazumder, "Q-MOS Circuit Design," ***Defense Advanced Research Project Agency***, Raytheon, Dallas, 1999.

252. P. Mazumder, "RTD Circuit Design***," Office of Naval Research***, Ann Arbor, 1998.

253. P. Mazumder, "Ultra-fast Circuit Design with NDR Devices," ***Defense Advanced Research Project Agency***, Santa Fe, Oct. 1997.

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### Technical Reports

255. P. Mazumder and J. H. Patel, "Parallel Testing of Pattern-Sensitive Faults in Random-Access Memory," *Technical Report CSG-56, Coordinated Science Laboratory*, Aug. 1986.

256. P. Mazumder, "Networks and Embedding Aspects of Hyper-cellular Structures for On-Chip Parallel Processing," *M. Sc. Thesis, Department of Computer Science, University of Alberta*, 1985.

257. P. Mazumder and J. H. Patel, "Testable RAM Design," *SRC Corporate Research*, 1986 Annual Report.

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260. A. Chakravarthy and P. Mazumder, "Gate Matrix Layout Techniques," *CSE-TR-12-90, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan*, Ann Arbor, 1990.

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263. K. Shahookar and P. Mazumder, "VLSI Cell Placement Techniques," *CRL-TR-07-88, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan*, Ann Arbor, Aug. 1988.

264. P. Mazumder, "CPLA - A Software Tool That Automatically Generates "C"-Model for PLA's," *Bell Laboratories Technical Memorandum, 55612-1A-262*, Aug. 1985.

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266. P. Mazumder, "Automatic Integrated Circuit Synthesizer: Generates PLA Layout from Behavioral Description Written in C Language," *Bell Laboratories Technical Memorandum, 55612-1A-262*, Aug. 1985.

### Publications in Industry (during 1976-1982)

Published over fifteen technical papers and application ideas while working at the Bharat Electronics Ltd. during 1976-1982. Topics included

- An Integrated Circuit Design for the Raster-Scan Vertical Deflection System.
- An Integrated Circuit Design for the Sync Processing Circuit
- Integrated Chip Set for Laser Range Finder in Military Applications
- An Integrated Circuit Design for High-Gain Pre-Amplifier with Automatic Level Controller
- A Integrated Circuit Design for Hearing-Aid Amplifier

- An Integrated Circuit Design for Quadrant Detection and Amplification of Frequency-Multiplexed Voice Signal
- A Large-Scale Integrated Circuit Design for Stepper-Motor-Driven Analog Clock Chip
- Study of Failure Modes in CMOS ICs During Handling
- Leakage-Current-Based Fault Characterization in a Non-planar Gas Discharge Display
- IC Design Considerations in Fabrication of Large Planar Plasma Display
- Application Notes on Analog and Digital Circuits

All these were published in BEL Application Notes and BEL Technical Report.

## XIII. Book Reviews

1. J.V. Oldfield, J.P. Gray, T.A. Kean, and R.C. Dorf, "Field-Programmable Gate Arrays for Implementation and Rapid Prototyping of Digital Systems", ***John Wiley and Sons, Inc.***, New York.
2. J. Beetam, "Computer Architectures", ***Aksen Associates Inc. Publishers,*** California.
3. "The Science and Technology of Microelectronic Processing", ***Saunders College Publishing***, Pennsylvania.
4. D. Pradhan, "Fault-Tolerant System Design", ***Prentice Hall***, New Jersey.
5. Price, "Introduction to VLSI Design", ***Prentice Hall,*** New Jersey.
6. C.P. Ravi Kumar, "Computer-Aided Design for VLSI Systems", ***Kluwer Academic Publishers,*** Massachusetts.
7. Fu, "Neural Networks in Computer Intelligence", ***Prentice Hall,*** New Jersey.
8. P. Banerjee, "Parallel Algorithms for VLSI Computer-Aided Design Applications", ***Prentice Hall,*** New Jersey.
9. R. Karri, "Automatic Synthesis of Fault-tolerant VLSI Systems", ***Kluwer Academic Publishers,*** Massachusetts.
10. A. S. Sedra and K. C. Smith, "SPICE Simulation: Microelectronics Circuits", ***Prentice Hall.***
11. A. B. Marcovitz, "Introduction to Logic Design," ***McGraw Hill.***
12. N. Jha and S. Gupta, "Testing of Digital Systems," ***Cambridge Press.***

## XIV. Technical Presentations (excluding conferences and workshops)

### At Industries and National Laboratories

### Formal Talks

1. Quantum electronic circuit design at ***Intel Corporation***, Santa Clara, California.
2. Quantum electronic circuit design at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
3. Quantum electronic circuit design at ***Silicon Value***, Jerusalem, Israel.
4. Quantum electronic circuit design ***at Fraunhofer Institute***, Freiburg, Germany.
5. Quantum electronic circuit design at ***Hitachi Central Research Laboratories***, Kokubunji, Japan.
6. Quantum electronic circuit design at ***NEC Corporation***, Tsukuba, Ibaraki, Japan.
7. Quantum electronic circuit design at ***Fujitsu***, Morinosato-Wakamiya, Japan.
8. Quantum electronic circuit design at ***Texas Instruments***, Dallas, Texas.
9. Quantum electronic circuit design at ***Hughes Research Laboratories***, Los Angeles, California.
10. Memory testing at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
11. Memory testing at ***Digital Equipment Corporation***, Hudson, Massachusetts
12. Memory testing at ***Fujitsu***, Morinosato-Wakamiya, Japan.
13. Memory testing at ***Intel***, Santa Clara, California
14. Memory testing at ***Hitachi Central Research Laboratories***, Kokubunji, Japan.
15. Memory testing at ***AT&T Bell Laboratories***, Murray Hill, New Jersey.
16. Memory testing at ***Bell Northern Research Laboratories***, Ottawa, Canada
17. Embedded memory compilation at ***Synopsys,*** Palo Alto, California.
18. Embedded memory compilation at ***Neo-Magic Corporation***, Santa Clara, California.
19. Embedded memory compilation at ***Ambit Design Systems***, Santa Clara, California.
20. Memory testing at ***Micron Technology***, Boise, Idaho.
21. Memory testing at ***MCC***, Austin, Texas
22. Memory testing at ***Texas Instruments***, Bangalore, India.
23. Memory testing at ***AT&T Bell Laboratories***, Holmdel, New Jersey.

24. VLSI chip testing at ***ERIM Research Laboratory***, Ann Arbor, Michigan.
25. VLSI layout techniques at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
26. VLSI layout techniques at ***General Motors Research***, Warren, Michigan.
27. VLSI layout techniques at ***Bell Northern Research Laboratories***, Ann Arbor, Michigan.
28. VLSI layout techniques at ***Cypress Semiconductor***, Santa Clara, California
29. VLSI layout techniques at ***National Semiconductor***, Santa Clara, California
30. Built-in self-repairable IC design at ***Nippon Electric Company***, Princeton, New Jersey.
31. Built-in self-repairable IC design at ***Bell Communications Research***, Morris Town, New Jersey.
32. Built-in self-repairable IC design at ***Ford Motors Company***, Dearborn, Michigan.
33. Built-in self-repairable IC design at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
34. Research activities on circuit design at ***IBM Watson Research Center***, New York.
35. Research activities on circuit design at ***Hitachi Development Laboratories***, Mobarra, Japan.
36. Research activities on circuit design at ***David Sarnoff Research Center***, Princeton, New Jersey.
37. Research activities on circuit design at ***NEC Central Research*** Laboratories, Kanagawa, Japan.
38. Quantum electronic circuit design at ***Sun Microsystems,*** Sunnyvale, California
39. Dynamic noise analysis methodology for VLSI design at ***Sun Microsystems***, Mountainview, California
40. Dynamic noise analysis methodology for VLSI design at ***Sequent design Automation***, San Jose, California
41. Quantum electronic circuit design at ***AMD,*** Sunnyvale, California

### Informal Presentations

42. Memory testing at ***Texas Instruments***, Houston, Texas.
43. Embedded memory testing at ***Logic Vision***, San Jose, California.
44. VLSI layout techniques at ***Avant!,*** Fremont, California.
45. VLSI layout techniques at ***International Business Machine***, Fishkill, New York.
46. Memory testing at ***LSI Logic***, Milpitas, California.
47. VLSI chip layouts at ***Xilinx***, Inc., San Jose, California.
48. Built-in self-repairable design at ***Phillips Laboratories***, Kirtland, New Mexico.
49. Built-in self-repairable design at ***Altera Corporation,*** San Jose, California.

### Formal Talks at Universities

50. Multilayer VLSI routing techniques at ***University of California***, Berkeley, California.
51. Memory testing at ***Stanford University***, Palo Alto, California.
52. Quantum electronic circuit design at ***University of Illinois***, Urbana-Champaign, Illinois.
53. Quantum electronic circuit design at ***University of California***, Berkeley, California.
54. Quantum electronic circuit design at ***Gerhard-Mercater University***, Duisburg, Germany.
55. VLSI layout design at ***Princeton University***, Princeton, New Jersey.
56. Memory testing at ***Purdue University***, West Lafayette, Indiana.
57. Memory testing at ***University of Southern California***, Los Angeles, California.
58. Built-in self-repairable IC design at ***University of Iowa***, Iowa City, Iowa.
59. Memory testing at ***King Fahd University***, Saudi Arabia.
60. Quantum electronic circuit design at ***Nanjing University,*** Nanjing, China
61. Memory testing at ***Johns Hopkins University***, Baltimore, Maryland.
62. Quantum electronic circuit design at ***Ohio State University***, Columbus, Ohio
63. Memory testing at ***University of Minnesota***, Minneapolis, Minnesota.
64. Quantum electronic circuit design at ***University of Tokyo***, Tokyo, Japan.
65. Quantum electronic circuit design at ***Delft Technological University***, Delft, Netherlands.
66. Quantum electronic circuit design at ***King Fahd University***, Saudi Arabia.
67. Quantum electronic circuit design at ***Universidad de Las Palmas de Gran Canaries***, Spain.
68. Quantum electronic circuit design at ***South East University,*** Nanjing, China
69. Memory testing and repair algorithms at ***Indian Institute of Technology***, New Delhi, India.
70. Memory testing at ***Texas A&M University***, College Station, Texas.
71. Quantum electronic circuit design at ***Northwestern University***, Evanston, Illinois
72. Built-in self-repairable IC design at ***Wayne State University***, Detroit, Michigan.
73. VLSI layout design at ***Indian Institute of Science***, Bangalore, India.

74. Built-in self-repairable design at ***Association of Computing Machine Symposia***, Ann Arbor, Michigan.

### Formal Visits to University Laboratories

75. VLSI Design and Education Center, ***University of Tokyo***, Tokyo, Japan.
76. Computer Engineering Research Center, ***University of Texas***, Austin, Texas.
77. Nanoelectronics Laboratory, ***University of Texas***, Dallas, Texas.
78. Testing Laboratory, ***Technical University of Budapest***, Budapest, Hungary.
79. ***Rice University***, Houston, Texas.
80. ***University of North Carolina***, Chapel Hill.
81. ***Virginia Commonwealth University***, Richmond, Virginia.
82. ***Oxford University***, Oxford, England.

## XV. Teaching Accomplishments

Received Letter of Commendation for Teaching from the Dean of College of Engineering.

### Courses Taught and Developed

1. Winter 2003: EECS 270: Logic Design
   Evaluation: 4.02/5.0 (first item) and 3.77/5.0 (second item)
2. Fall 2002: EECS 579: Digital Testing
   Evaluation: 3.88/5.0 (first item) and 3.90/5.0 (second item)
3. Winter 2002: EECS 270: Digital Logic Design
   Evaluation: 4.25/5.0 (first item) and 4.33/5.0 (second item)
4. Winter 2001: EECS 270: Logic Design
   Evaluation: 4.02/5.0 (first item) and 4.32/5.0 (second item)
5. Fall 2000: EECS 270: Digital Logic Design
   Evaluation 3.74/5.0 (first item) and 4.17/5.0 (second item)
6. Fall 1999: EECS 427: VLSI Design
   Evaluation: 4.05/5.0 (first item) and 3.50/5.0 (second item)
7. Fall 1998: EECS 270: Logic Design
   Evaluation: 4.00/5.0 (first item) and 3.99/5.0 (second item)
8. Winter 1999: EECS 579: Digital Testing
   Evaluation: 3.42/5.0 (first item) 3.20/5.0 (second item)
9. Fall 1998: EECS 270: Digital Testing
   Evaluation: 4.00/5.0 (first item) and 3.99/5.0 (second item)
10. Winter 1998: Digital Logic
    Evaluation: 4.00 (first item) and 3.99 (second item)
11. Fall 1997: Taught EECS 427: VLSI Design
    Evaluation: 4.71 (first item) and 4.58 (second item)
12. Winter 1996: Taught EECS 527: Computer-Aided Design for VLSI Systems
    Evaluation: 4.50 (first item) and 4.10 (second item)
13. Fall 1995: Taught EECS 427: VLSI Design
    Evaluation: 4.55 (first item) and 3.94 (second item)
14. Winter 1995: Taught EECS 527: Computer-Aided Design for VLSI Systems
    Evaluation: 4.25 (first item) and 4.08 (second item)
15. Fall 1994: Taught EECS 427: VLSI Design
    Evaluation: 4.81 (first item) and 4.12 (second item)
16. Fall 1993: Taught EECS 427: VLSI Design
    Evaluation: 4.32 (first item) and 3.83 (second item)
17. Spring 1992: Taught EECS 270: Digital Logic Design
    Evaluation: 4.6 (first item) and 4.43 (second item)
18. Winter 1992: Taught EECS 527: Computer-Aided Design for VLSI Systems

Evaluation: 4.00 (first item) and 4.25 (second item)

19. Fall 1991: Taught EECS 427: VLSI Design
    Evaluation: 4.13 (first item) and 3.88 (second item)
20. Spring 1991: Taught EECS 270: Digital Logic Design
    Evaluation: 4.54 (first item) and 4.71 (second item)
21. Winter 1991: Taught EECS 570: Advanced Computer Architecture
    Evaluation: 4.20 (first item) and 3.89 (second item)

Legend: 5.0 – Excellent, 4.0 – Very Good, 3.0 – Good, 2.0 – Fair, 1.0 – Poor.

## XVI. Extracurricular Activities

I am an avid tennis player and have been playing the game for the past 30 years, whenever I am not injured. Some of my sports awards that perhaps I am more proud of than my professional achievements are listed below. Of course, I belong to the category of hackers who pay to play rather than get paid to play. So these awards are small consolations for my efforts in these games.

- **Tennis**: Between 1975 and 2002, won several prizes in Singles and Doubles Events (between 4.0 and 4.5 NTRP levels) in Ann Arbor City Open Tennis Tournament, Ypsilanti (Michigan) City Open Tennis Tournament, Bangalore City Industrial Tennis Tournament, Indian Institute of Science Tennis Tournament, Bharat Electronics Ltd. Club Tennis Tournament, Huron Valley Tennis Club Tournament, etc.

- **Badminton**: Represented Indian Institute of Science in Karnataka State University Tournament and due to the presence of Pradeep Padukone, the brother of legendary World Badminton Champion Prakash Padukone, on our I.I.Sc. team, we won the tournament in 1975. Also won 3 prizes in I.I.Sc. Gymkhana Tournaments.

- **Table Tennis**: Between 1974-1976, won 4 prizes in I.I.Sc. Gymkhana Tournaments.

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