Test Economics

- Economics defined
- Costs
- Production
- Benefit - cost analysis
- Economics of *design-for-testability* (DFT)
- Quality and *yield loss*
- Summary

The Meaning of Economics

Economics is the study of how men choose to use scarce or limited productive resources (land, labor, capital goods such as machinery, and technical knowledge) to produce various commodities (such as wheat, overcoats, roads, concerts, and yachts) and to distribute them to various members of society for their consumption.

-- Paul Samuelson

Engineering Economics

Engineering Economics is the study of how engineers choose to optimize their designs and construction methods to produce objects and systems that will optimize their efficiency and hence the satisfaction of their clients.

Costs

- Fixed cost
- Variable cost
- Total cost
- Average cost

Example: *Costs of running a car*

Fixed cost	$25,000	Purchase price of car
Variable cost	20 cents/mile	Gasoline, maintenance, repairs
Total cost	$25,000 + 0.2$x$	For traveling x miles
Average cost	$\$\dfrac{25{,}000}{x} + 0.2$	Total cost / x

Simple Cost Analysis

Case 1: 10,000 miles/yr, $12,500 resale value after 5 years

$$\text{Average cost} = \$\ \frac{25{,}000 - 12{,}500}{50{,}000} + 0.2 = 45 \text{ cents/mile}$$
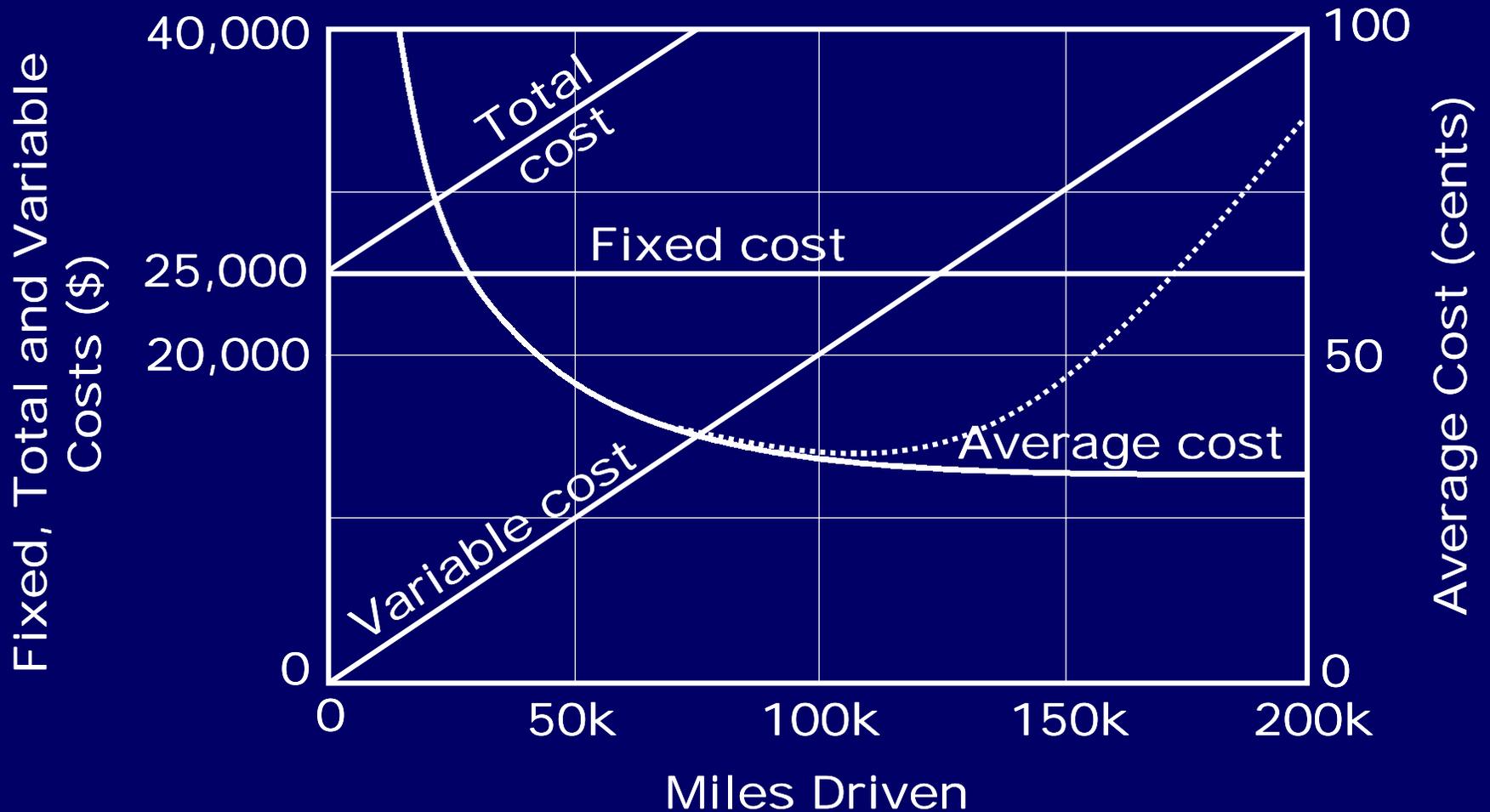
Case 2: 10,000 miles/yr, $6,250 resale value after 10 years

$$\text{Average cost} = \$\ \frac{25{,}000 - 6{,}250}{100{,}000} + 0.2 = 38.75 \text{ cents/mile}$$

Case 3: 10,000 miles/yr, $0 resale value after 20 years

$$\text{Average cost} = \$\ \frac{25{,}000 - 0}{200{,}000} + 0.2 = 32.5 \text{ cents/mile}$$

Cost Analysis Graph

Production

- Inputs (*x*): Labor, land, capital, enterprise, energy (*x* may include both fixed and variable costs)
- Production output, $Q = f(x)$
- Average product, Q / x
- Marginal product, dQ / dx

Law of Diminishing Returns

If one input of production is increased keeping inputs constant, then the output may increase, eventually reaching a point beyond which increasing the inputs will cause progressively less increase in output.
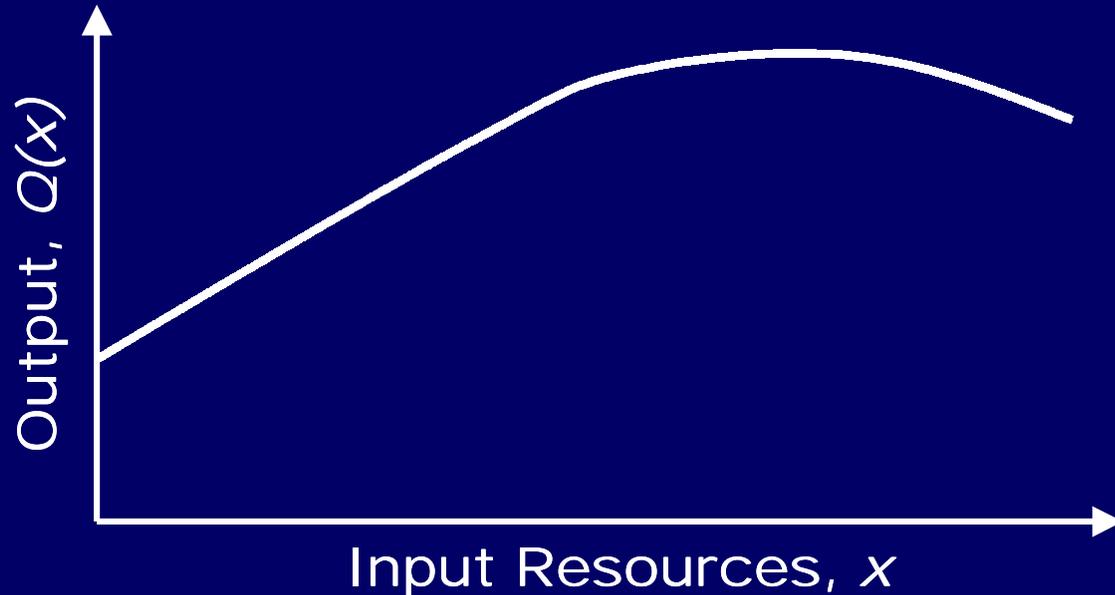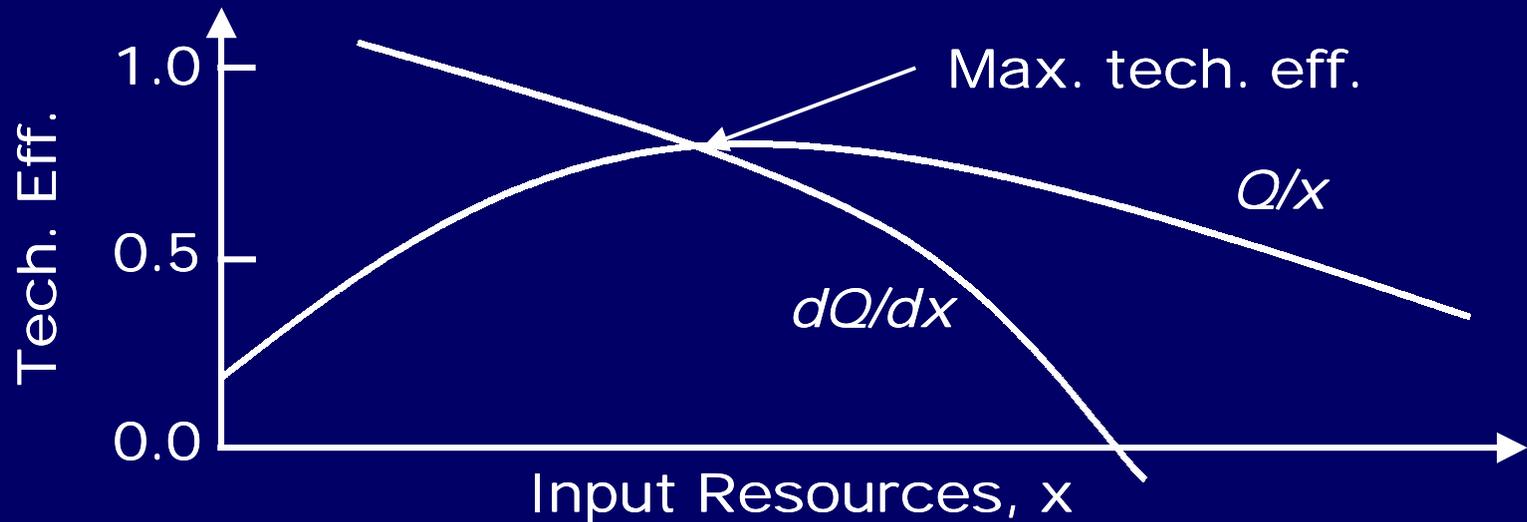
Technological Efficiency

Technological efficiency = Q/x
where x = variable cost

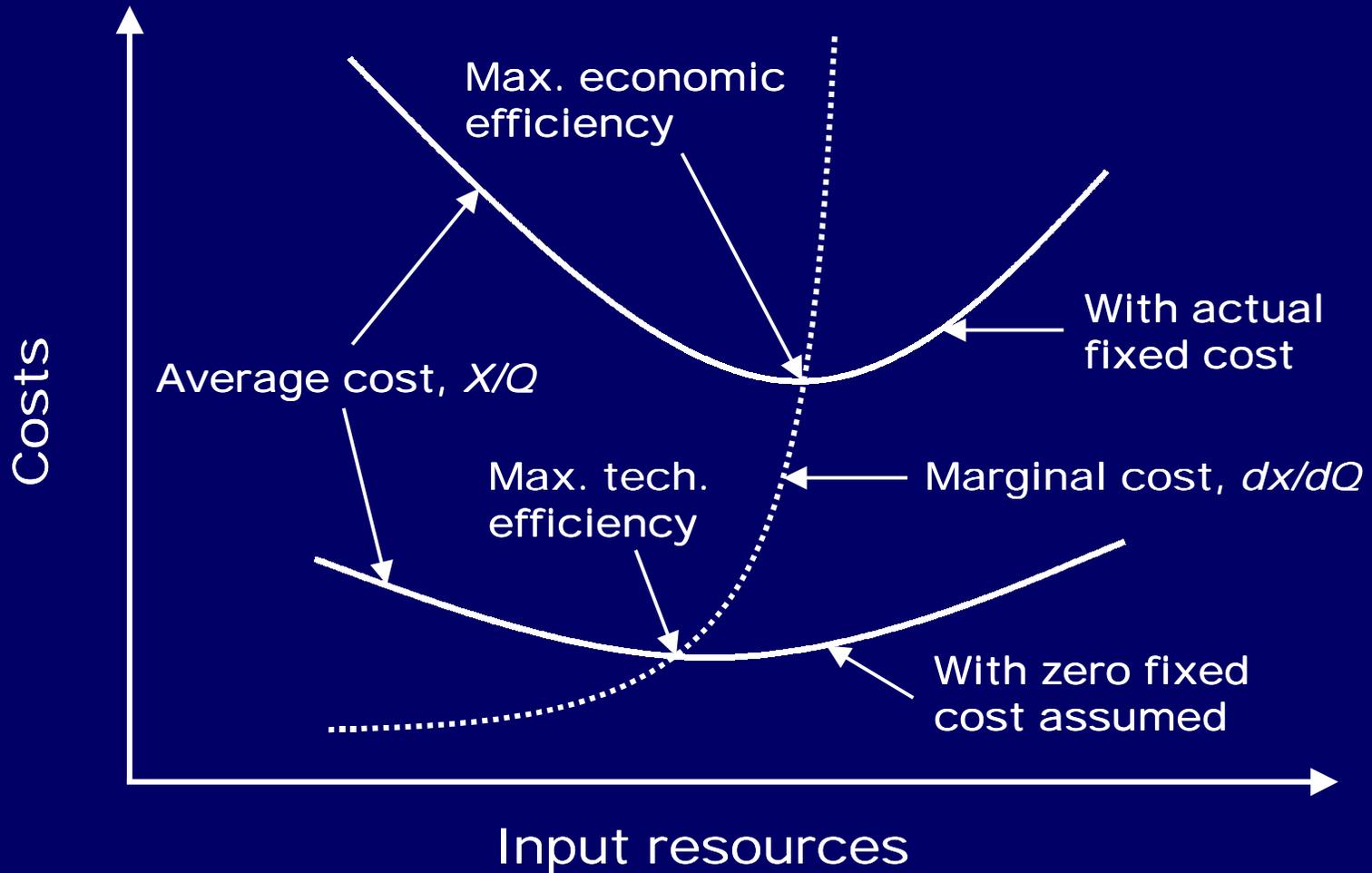To maximize tech. Efficiency:

$$\frac{dQ}{dx} \frac{Q}{x} = 0; \qquad \frac{1}{x}\frac{dQ}{dx} - \frac{Q}{x^2} = 0 \quad \text{or} \quad \frac{Q}{x} = \frac{dQ}{dx}$$

Max. tech. eff.

Q/x

dQ/dx

Tech. Eff.

1.0

0.5

0.0

Input Resources, x

Economic Efficiency

- Maximum economic efficiency minimizes the total average cost X/Q, where X is the total (fixed + variable) cost.

- Maximum economic efficiency is achieved when total average cost equals the marginal cost, $X/Q = dX/dQ$.

- For average cost = marginal cost
  - Take variable cost to maximize technological efficiency
  - Take total cost to maximize economic efficiency

Maximum Efficiencies

Costs (y-axis)

Input resources (x-axis)

Max. economic efficiency

With actual fixed cost

Average cost, X/Q

Max. tech. efficiency

Marginal cost, dx/dQ

With zero fixed cost assumed

Mass Production

- Production can be increased at a faster rate than the increase of inputs. This is known as *increasing returns to scale.*
- Some reasons for increasing returns to scale
    - Technological factors
    - Specialization
    - Only some inputs are increased
- If increase of inputs continues, eventually the law of diminishing returns applies.

Benefit-Cost Analysis

- Benefits: Savings in manufacturing costs (capital and operational) and time, reduced wastage, automation, etc.
- Costs: Extra hardware, training of personnel, etc.
- Benefit/cost ratio

$$\text{B/C ratio} = \frac{\text{Annual benefits}}{\text{Annual costs}} > 1$$

Economics of Design for Testability (DFT)

- Consider life-cycle cost; DFT on chip may impact the costs at board and system levels.

- Weigh costs against benefits
  - Cost examples: reduced yield due to area overhead, yield loss due to non-functional tests
  - Benefit examples: Reduced ATE cost due to self-test, inexpensive alternatives to burn-in test

Benefits and Costs of DFT

Level	Design and test	Fabri-cation	Manuf. Test	Maintenance test	Diagnosis and repair	Service interruption
Chips	+ / -	+	-			
Boards	+ / -	+	-		-	
System	+ / -	+	-	-	-	-

+   Cost increase
-   Cost saving
+/- Cost increase may balance cost reduction

Summary

- Economics teaches us how to make the right trade-offs.
- It combines common sense, experience and mathematical methods.
- The overall benefit/cost ratio for design, test and manufacturing should be maximized; *one should select the most economic design over the cheapest design.*
- A DFT or test method should be selected to improve the product quality with minimal increase in cost due to area overhead and yield loss.

Yield Analysis & Product Quality

- Yield and manufacturing cost
- Clustered defect yield formula
- Yield improvement
- *Defect level*
- Test data analysis
- Example: SEMATECH chip
- Summary

VLSI Chip Yield

- A manufacturing defect is a finite chip area with electrically malfunctioning circuitry caused by errors in the fabrication process.
- A chip with no manufacturing defect is called a good chip.
- Fraction (or percentage) of good chips produced in a manufacturing process is called the *yield*. Yield is denoted by symbol *Y*.
- Cost of a chip:

$$\frac{\text{Cost of fabricating and testing a wafer}}{\text{Yield x Number of chip sites on the wafer}}$$

Clustered VLSI Defects

Good chips

Faulty chips
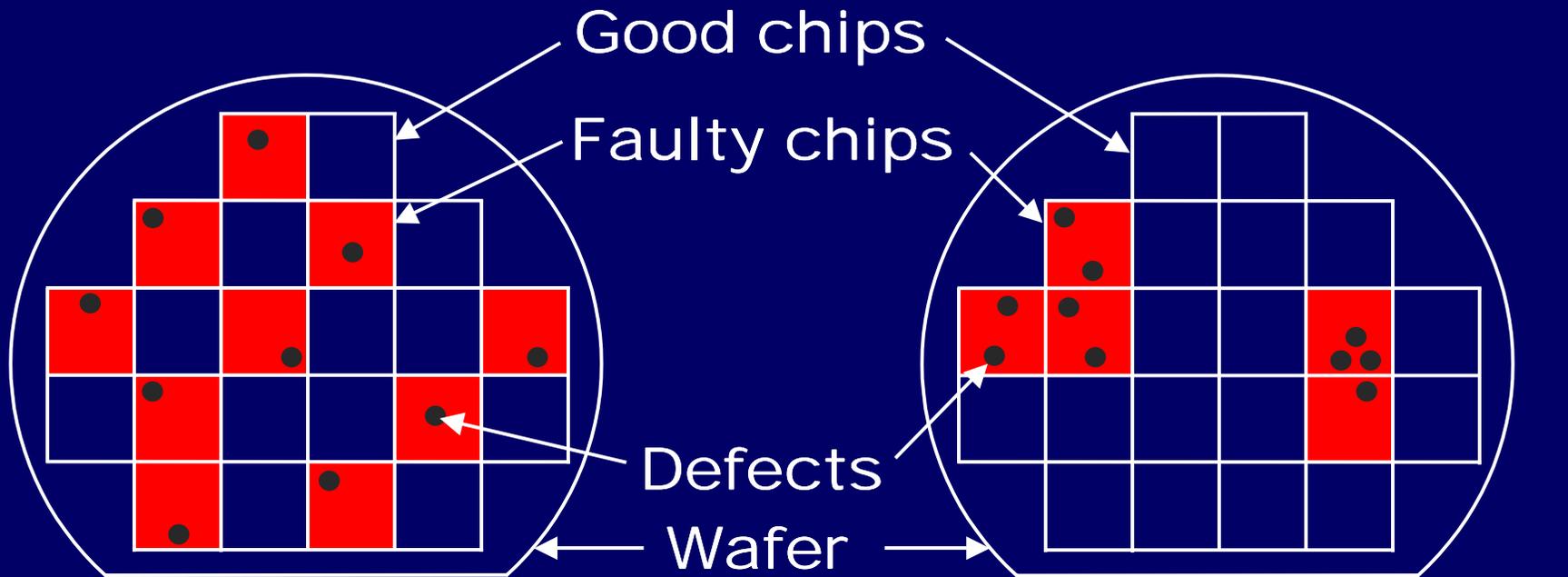
Defects

Wafer

Unclustered defects
Wafer yield = 12/22 = 0.55

Clustered defects (VLSI)
Wafer yield = 17/22 = 0.77

Yield Parameters

- Defect density (d) = Average number of defects per unit of chip area
- Chip area (A)
- Clustering parameter (α)
- Negative binomial distribution of defects, $p(x)$ = Prob (number of defects on a chip = x)

$$= \frac{\Gamma(\alpha + x)}{x!\,\Gamma(\alpha)} \cdot \frac{(Ad/\alpha)^x}{(1 + Ad/\alpha)^{\alpha + x}}$$

where Γ is the gamma function
$\alpha = 0$, $p(x)$ is a delta function (max. clustering)
$\alpha = \infty$, $p(x)$ is Poisson distr. (no clustering)

Yield Equation

Y = Prob (zero defect on a chip) = p (0)

$$Y = (1 + Ad / \alpha)^{-\alpha}$$

Example: Ad = 1.0, α = 0.5, Y = 0.58

Unclustered defects: $\alpha = \infty$, $Y = e^{-Ad}$

Example: Ad = 1.0, $\alpha = \infty$, Y = 0.37

too pessimistic !

Defect Level or Reject Ratio

- *Defect level* (DL) is the ratio of faulty chips among the chips that pass tests.
- DL is measured as *parts per million* (ppm).
- DL is a measure of the effectiveness of tests.
- DL is a quantitative measure of the manufactured product quality. For commercial VLSI chips a DL greater than 500 ppm is considered unacceptable.

Determination of DL

- From field return data: Chips failing in the field are returned to the manufacturer. The number of returned chips normalized to one million chips shipped is the DL.

- From test data: Fault coverage of tests and chip fallout rate are analyzed. A modified yield model is fitted to the fallout data to estimate the DL.

Modified Yield Equation

- Three parameters:
    - Fault density, f = average number of stuck-at faults per unit chip area
    - Fault clustering parameter, β
    - Stuck-at fault coverage, T
- The modified yield equation:

$$Y(T) = (1 + TAf/\beta)^{-\beta}$$

Assuming that tests with 100% fault coverage ($T = 1.0$) remove all faulty chips,
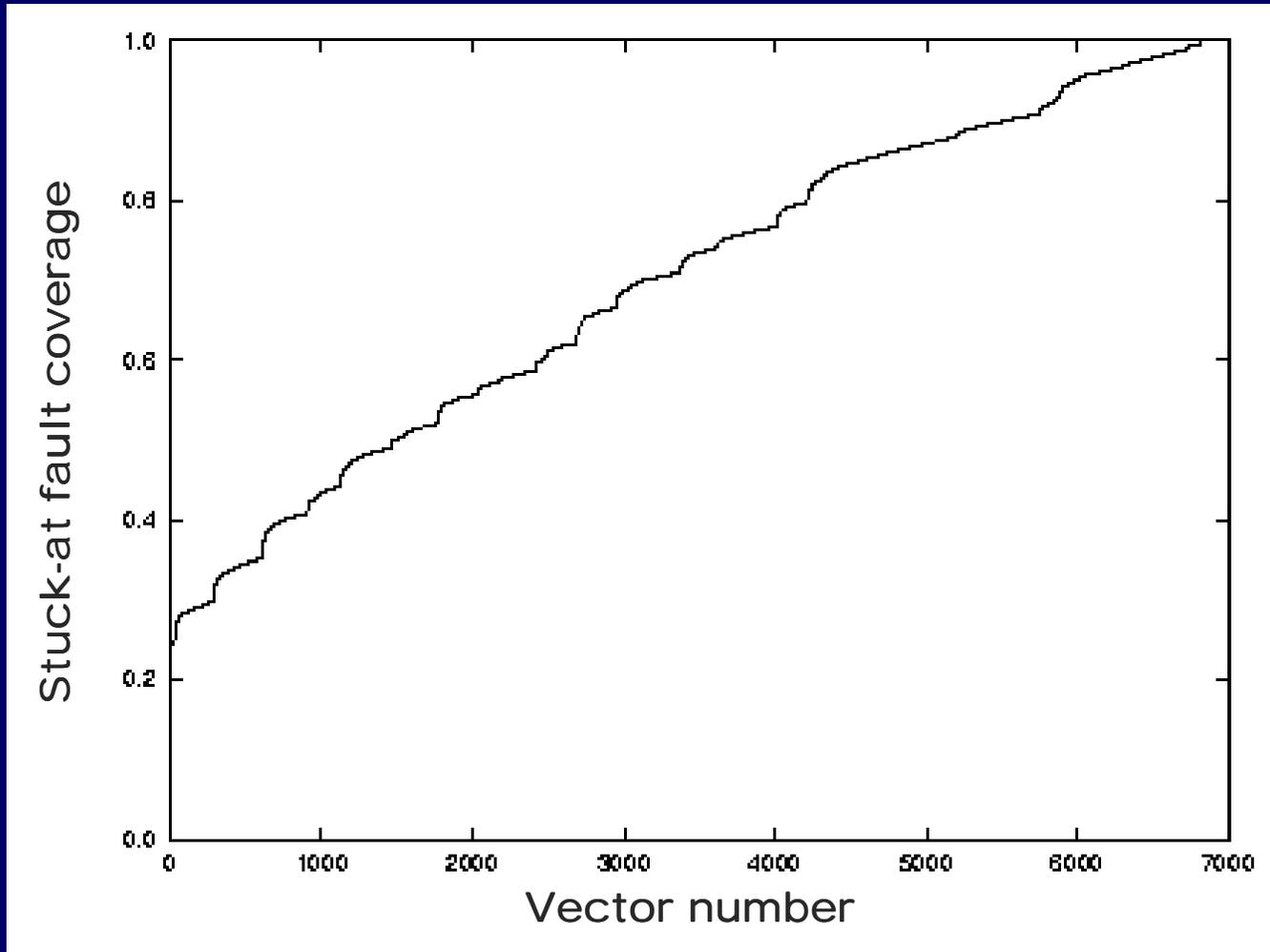
$$Y = Y(1) = (1 + Af/\beta)^{-\beta}$$

Defect Level

$$DL(T) = \frac{Y(T) - Y(1)}{Y(T)}$$

$$= 1 - \frac{(\beta + TAf)^{\beta}}{(\beta + Af)^{\beta}}$$

Where T is the fault coverage of tests, Af is the average number of faults on the chip of area A, β is the fault clustering parameter. Af and β are determined by test data analysis.
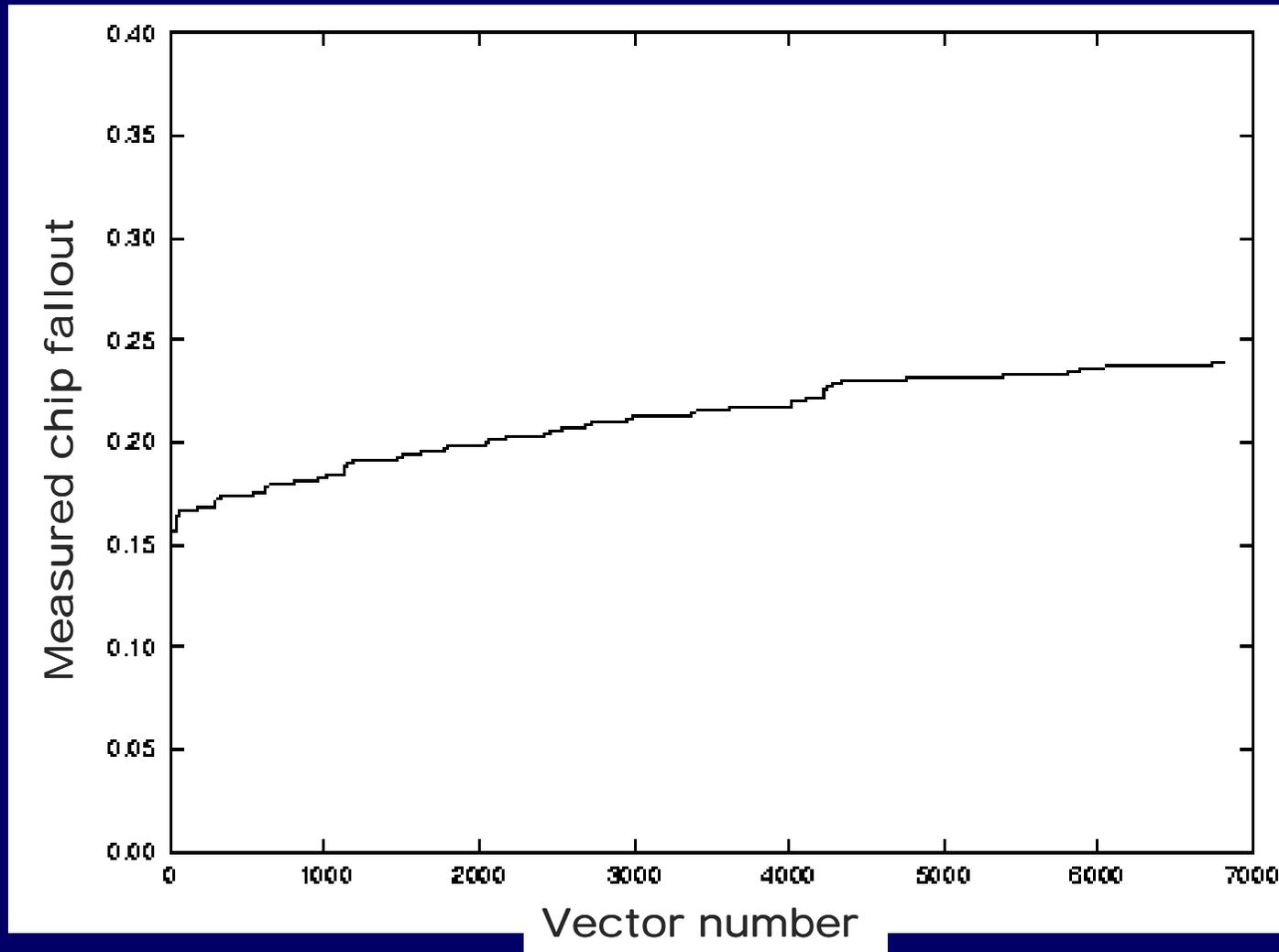
Example: SEMATECH Chip

- Bus interface controller ASIC fabricated and tested at IBM, Burlington, Vermont
- 116,000 equivalent (2-input NAND) gates
- 304-pin package, 249 I/O
- Clock: 40MHz, some parts 50MHz
- 0.45μ CMOS, 3.3V, 9.4mm x 8.8mm area
- Full scan, 99.79% fault coverage
- Advantest 3381 ATE, 18,466 chips tested at 2.5MHz test clock
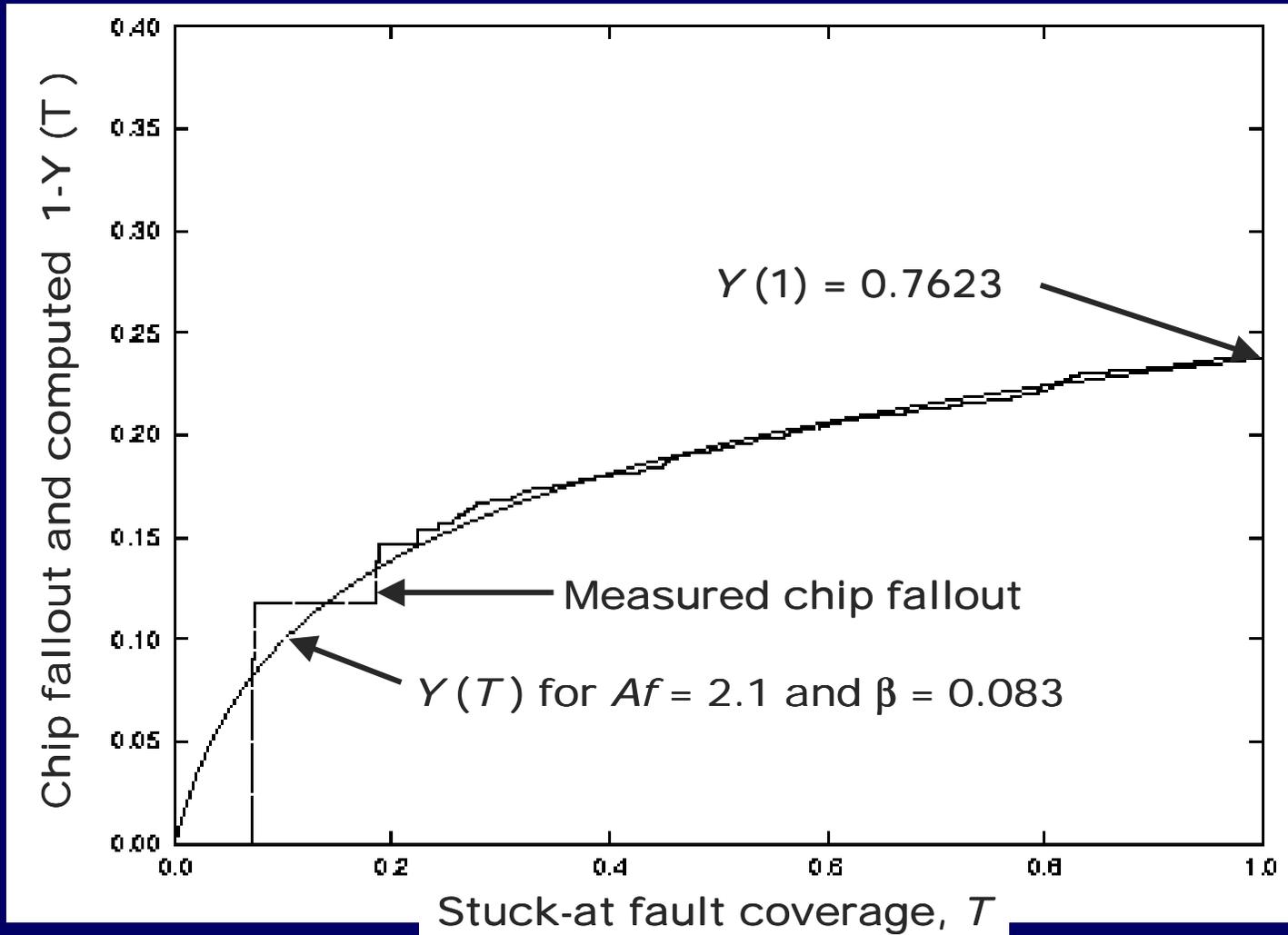- Data obtained courtesy of Phil Nigh (IBM)
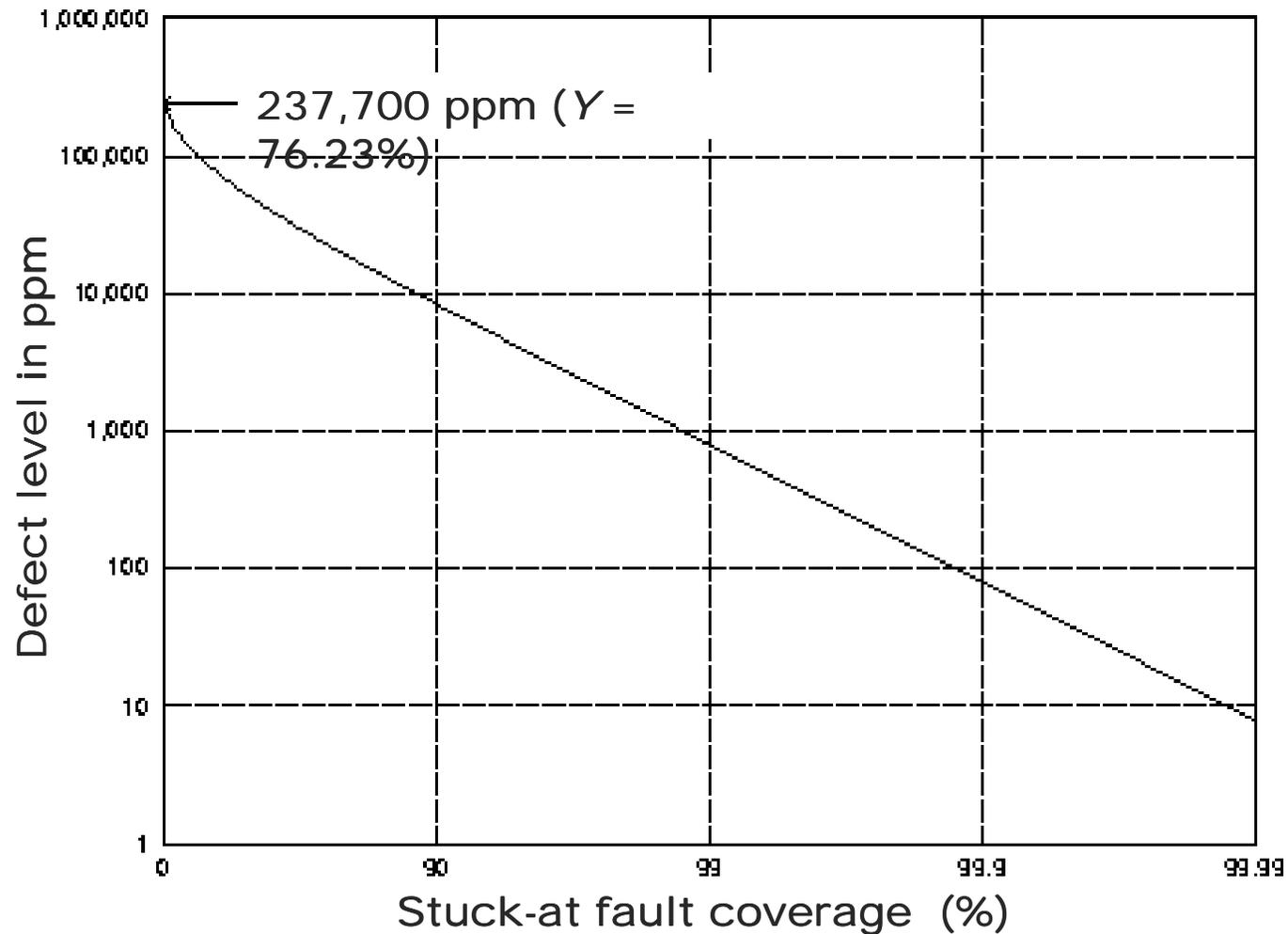
Test Coverage from Fault Simulator

Measured Chip Fallout

Model Fitting

Chip fallout and computed $1-Y(T)$ versus Stuck-at fault coverage, T

$Y(1) = 0.7623$

Measured chip fallout

$Y(T)$ for $Af = 2.1$ and $\beta = 0.083$

Computed DL

Summary

- VLSI yield depends on two process parameters, defect density (d) and clustering parameter (α)
- Yield drops as chip area increases; low yield means high cost
- Fault coverage measures the test quality
- Defect level (DL) or reject ratio is a measure of chip quality
- DL can be determined by an analysis of test data
- For high quality: DL < 500 ppm, fault coverage ~ 99%