Test of Basic Gates

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Testing for Single Stuck Line (SSL) Faults

3-input NAND Gate

	a/0	a/1	b/0	b/1	c/0	c/1	z/0	z/1
000							X	
001							X	
010							X	
011		X					X	
100							X	
101				X			X	
110						X	X	
111	X		X		X			X

- number of SSLs=4x2=8
- Minimal test set t={011, 101, 110, 111}
- Inversions on inputs/outputs do not change the number of tests

Testing for SSL

	a/0	a/1	b/0	b/1	z/0	z/1
00		X		X		X
01			X		X	
10	X				X	
11					X	

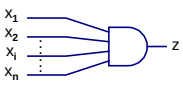
- number of SSLs = 3x2 = 6
- Minimal test set t={00, 01, 10}
- t also tests 2-input nor gate

Test Set for AND/NAND; OR/NOR Gates

# of Inputs	Gate Type	Test Set
2	AND/NAND	{00, 10, 11}
3	AND/NAND	{011, 101, 110, 111}
2	OR/NOR	{00, 01, 10}
3	OR/NOR	{00, 100, 010, 001}

- ***Theorem 1***: An n-input AND or NAND gate has a unique minimal set of n+1 tests that covers(or detects) all single-stuck-line (SSL) faults:
  011 · · ·11, 101 · · ·11, 110 · · ·11, · · ·, 111 · · ·10, 111 · · ·11
- ***Theorem 2***: An n-input OR or NOR gate has a unique minimal set of n+1 tests that covers (or detects) all SLL faults:
  100 · · ·00, 010 · · ·00, 001 · · ·00, 000 · · ·01, 000 · · ·00

Test Set for AND/NAND; OR/NOR Gates

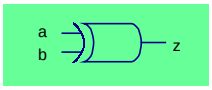


- SA1
  - Input line x_i is tested for x_i/1 if x_i=0 $\wedge \forall j \neq I$ x_j=1
  - {$\forall I$ x_i/1, z/1} is an equivalent class of faults

  $\Rightarrow$ n tests patterns test n+1 SA1 faults corresponding to all inputs and output lines
- SA0: Test vector 11 · · ·11 tests z/0 and $\forall i$ x_i/0

  $\Rightarrow$ The test vector 11 · · ·11 tests n+1 SA0 faults
- Minimal test set required to test 2(n+1) SSL faults is *n+1*

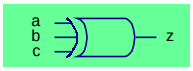
Test Set for XOR/XNOR Gates



	a/0	a/1	b/0	b/1	z/0	z/1
00		X		X		X
01		X	X		X	
10	X			X	X	
11	X		X			X

- No essential test vector
- At least 3 tests needed to cover all faults
- Minimal complete tests: T_1={00, 01, 10}; T_2={00, 01, 11}; T_3={00, 10, 11}; T_4={01, 10, 11}
- Every input pattern detects an SSL fault on every line of the gate

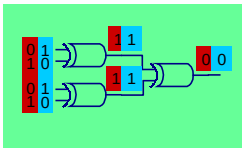
Test Set for XOR/XNOR Gates

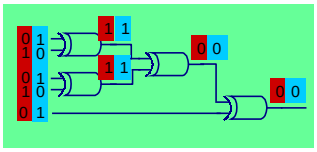


	a/0	a/1	b/0	b/1	c/0	c/1	z/0	z/1
000		X		X		X		X
001		X		X	X		X	
010		X	X			X	X	
011		X	X		X			X
100	X		X		X	X		
101	X		X	X			X	
110	X		X			X		X
111	X		X		X		X	

- No essential test vector
- Any 2 complementary input patterns form a complete test set
- Example: (000, 111) or (010, 101)

Tests for Parity Circuit





- General n-input XOR gate (z=1 iff total # of 1's is odd)
- If n=2m+1 (odd), then any two complementary input patterns (X, X') detect all SSL faults in an XOR or XNOR gate
- If n=2m (even), then any (X, X') detect all SSL faults affecting input lines, but only one fault z/d [d=0, 1], on the output line. A third test to detect z/d' is needed.