EECS 427 – VLSI Design I

Winter 2013

Instructor:	Prof. Pinaki Mazumder Office: 4765 BBB Email: eecs270.mazum@gmail.com Office hours: TBD (Other times available by appointment)
GSI:	Mahmood Barangi/ Yalcin Yilmaz Email: eecs427gsi@umich.edu Office hours: Monday 3-5pm Wednesday 5-7pm Thursday 10am-12pm Location: TBD
Lectures:	Monday and Wednesday 10:30am – noon, 1003 EECS
Laboratory:	Friday 4:30 – 6:30 pm, 1003 EECS
Webpages:	http://ctools.umich.edu
Textbook:	Neil Weste and David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison Wesley, Fourth Edition, 2011. (Required)
Support:	CAEN hotline (764-2236), email caen@umich.edu, in person at room 1315 of the Duderstadt Center, or online at http://www.engin.umich.edu/caen/hotline for printer, network, machine, account, or similar problems. Joel VanLaven Email: jvanlav@eecs.umich.edu Contact Joel for major CAD tool issues. Consult Mahmood/Yalcin first.

Description

This course introduces mask-level integrated circuit design. Correct engineering design methodology is emphasized. Topics covered in lectures include: CMOS processes, mask layout methods and design rules; circuit characterization and performance estimation; logic families and sizing; and CMOS subsystem and system design.

Prerequisites

EECS 270 and 312. Students are expected to know logic design, transistor-level circuit design (especially static CMOS), and basic device physics. Some background in computer architecture is helpful (EECS 370/470), but not required.

Assignments

This is a project-oriented course in which you will design a moderate-sized CMOS integrated circuit. Tutorials will be given at the beginning and another later in the semester. You can work at your convenience. CAEN Labs are open 24 hours a day.

There will be 9 CAD assignments that build up the baseline of your final project. The baseline project involves the design of a 16-bit RISC microprocessor. The initial cell designs (CAD assignments 1 and 2) probably will not be used in the final project and must be done individually. You are encouraged to interact with others, but until you are asked to form teams, the work on your cell designs, simulations, etc., must be your own.

Submission Policy

CAD assignments will be submitted electronically and are due at 4pm on the due date. Be sure to do your design work in the class directory so that we will have access to it. Do not change the access rights to your class directory. Do not modify submitted files after the deadline. Late penalties are 25% for each day after the deadline. Note that late penalties are applied only to those portions of the assignment that are finished late. For example, if the schematic and functional verification was completed on time but layout was late, only the layout portion will be subject to the late penalty.

Project

The final project will be done in teams of five. The project must be completed, and you must submit a final report in the format specified. Within the constraints of available funding, eligible projects will be fabricated free of charge through the MOSIS service. If your project is fabricated, it must be tested; you can get credit for testing it in EECS 579 or as a directed study project.

Examinations

There will be two quizzes during the semester. Quizzes will be held in class.

Grading Scheme

The following grading scheme will be roughly followed:

CAD assignments	35% (9 CAD assignments)
Final project	35% (report, presentation, demo, and individual contributions)
Quizzes	30% (2 quizzes)

Honor Code

All students in the class are presumed to be decent and honorable, and all students in the class are bound by the College of Engineering Honor Code. You may not seek to gain an unfair advantage over your fellow students; you may not consult, look at, or possess the unpublished work of another without their permission; and you must appropriately acknowledge your use of another's work. Any violation of the honor policies appropriate to each piece of course work may be reported to the Honor Council, and if guilt is established penalties may be imposed by both the course instructor and the Faculty Committee on Discipline. Such penalties can include, but are not limited to, zero grades on assignments, letter grade deductions, or expulsion from the University. **If you have any questions about this course policy, please consult the course instructor**.

Tentative Schedule

Revised: 1/2/12
Text: Sections in WH (Weste and Harris, 4th)
Due dates: CAD assignments will be due on Fridays at 4pm (electronic submission).

Lecture	Date	Topic	Reading	Due Dates
1	1/09 We	Introduction		
2	1/14 Mo	Fabrication and layout	WH: 1.5, 3	
3	1/16 We	Estimate delay / Sizing	WH: 4	CAD1: Mux – 1/18
--	1/21 Mo	*No Class, MLK day*		
4	1/23 We	Estimate delay / Sizing	WH: 4	
5	1/28 Mo	Logical Effort	WH: 4	CAD2: FF – 1/25
6	1/30 We	Logical Effort	WH: 4	
7	2/04 Mo	Adders	WH: 11.2	CAD3: Regfile – 2/1
8	2/06 We	Adders	WH: 11.2	
9	2/11 Mo	Logic families	WH: 9.2-9.3	--
10	2/13 We	Logic families	WH: 9.2-9.3	
11	2/18 Mo	Logic families	WH: 9.2-9.3	CAD4: ALU – 2/15
12	2/20 We	Dynamic power	WH: 5.2	
13	2/25 Mo	Static power	WH: 5.3	CAD5: Shifter – 2/22
14	2/27 We	----- Midterm 1 -----		CAD6: Prog. Count – 3/1
--	3/04 Mo	*No Class, SPRING BREAK*		
--	3/06 We	*No Class, SPRING BREAK*		
15	3/11 Mo	SRAM	WH: 12.2	
16	3/13 We	SRAM	WH: 12.2	Project Proposal due
17	3/18 Mo	Sequential	WH: 10.2-10.3	
18	3/20 We	Sequential	WH: 10.2-10.3	CAD7: Datapath – 3/22
19	3/25 Mo	Multiplier	WH: 11.8, 11.9	
20	3/27 We	Multiplier	WH: 11.8, 11.9	CAD 8: Control - 3/29
21	4/01 Mo	Shifter	WH: 11.8, 11.9	
22	4/03 We	Design for Test	WH: 15.5-15.6	
23	4/08 Mo	New topics/overflow		
24	4/10 We	----- Midterm 2 -----		
25	4/15 Mo	Power and clock distribution	WH: 13.3-13.4	
23	4/17 We	Variability and reliability	WH: 7.2-7.3	
24	4/22 Mo	----- Final project presentations -----		CAD 9: Demo is on 4/24, Report is due on 4/27