# EECS 312: Digital Integrated Circuits Fall 2005

**Instructor:** Prof. Pinaki Mazumder
4765 CSE Building
mazum@eecs.umich.edu

**Office hours:** Tues/Thurs 4:30 pm – 5:00 pm If you cannot make office hours but want to meet with me, please set up an appointment by phone (3-2107) or by sending an e-mail.

**Graduate Student Instructors:** Gregory Brandon, brandon@umich.edu
**Office hours:** TBA

**Class Meeting Times:** 001 LEC T TH 3:00-4:30 at 133 CHRYS

**EWRE 104** 011 DIS F 12:30-1:30

**EWRE 104** 012 DIS F 1:30-2:30

**Course webpage:** *Ctools website: https://ctools.umich.edu/*
You need your umich password to access the site!

**Purpose:** EECS 312, *Digital Integrated Circuits*, is a junior-level digital circuits course for both electrical and computer engineering majors. Building upon pre-existing knowledge of MOSFET/BJT device operation, the student will learn to analyze and design digital circuits in various logic families, including static CMOS, domino, and pass-transistor logic. Tradeoffs among these logic families will be emphasized (e.g. noise immunity vs. speed, density vs. static power), allowing students to make informed decisions on when to use each style. They will be introduced to SPICE simulators and will use SPICE heavily in designing various blocks of logic in lab assignments as well as a design project. Key memory structures (SRAM, DRAM) will be described in detail. This class will put students in an ideal position to take EECS 427 where they will design and layout a 16-bit RISC microprocessor based on the circuit design principles learned in 312.

## Course objectives

1. To teach students the analysis and design of static CMOS digital circuits.
2. To develop a thorough understanding of the static and dynamic characteristics (delay, power, noise immunity, density) of various MOS based logic families (CMOS, pseudo-NMOS, pass transistor, domino).
3. To introduce and familiarize students with circuit simulation tools (SPICE) which will be invaluable to them in later courses (e.g. EECS 427) and industry as circuit designers.

4. To provide students the chance to work together on small design projects where they attempt to minimize certain objective functions while meeting other design constraints for a functional unit.
5. To teach the operation and importance of memory structures (SRAM, DRAM) in large digital systems.
7. To provide students with the required knowledge to make informed decisions on when to use different logic styles and the tradeoffs inherent in those decisions.
8. To teach students to analyze the effect of interconnect parasitics on circuit performance.
9. To introduce students to important future trends in large-scale digital circuit design, including manufacturability issues and barriers to device scaling.

## Catalog description

Design and analysis of static CMOS inverters and complex combinational logic gates. Dynamic logic families, pass-transistor logic, ratioed logic families. Sequential elements (latches, flip-flops). Bipolar-based logic; ECL, BiCMOS. Memories; SRAM, DRAM, EEPROM, PLA. I/O circuits and interconnect effects. Design projects. Lecture and software labs.

## Prerequisites:

EECS 215

## Textbook/Required Material:

*Digital Integrated Circuits: A Design Perspective*, J. Rabaey, A. Chandrakasan, and B. Nikolic, Prentice-Hall, 2003 (2nd edition).

## Grading

The final grade in this course consists of four parts:

| | |
|---|---|
| Homework | 20% |
| Software Labs (incl. Project) | 30% |
| 6-8 Quizzes | 25% |
| Final Exam | 25% |

**Late policy:** Homeworks are to be handed in at the **beginning** of lecture on the due date. Late homework will be accepted for 24 hours after this time with a 30% penalty. Solutions will then be posted and no further homework will be accepted.

| Lecture | Date | Topic | Text | Homework |
|---|---|---|---|---|
| 1 | **1/05** | Course intro, digital IC overview | 1.1, 1.2 | |
| 2 | **1/10** | Overview of CMOS circuits | notes | Tutorial |
| 3 | **1/12** | PN junction & MOSFET Theory I | 3.3 | Week |
| 4 | **1/17** | MOSFET Theory II | 3.3 | |
| 5 | **1/19** | CMOS fabrication | 3.3, notes | Lab #1 |
| 6 | **1/24** | Device fab (cont.), scaling, SPICE models notes | 2.2, 2.3 | HW #1 |
| 7 | **1/26** | CMOS inverter, VTC | 5.1- 5.3 | |
| 8 | **1/31** | CMOS inverter, delay analysis | 5.4 | |
| 9 | **2/2** | CMOS inverter, power analysis | 5.5.1 | Lab #2 |
| 10 | **2/7** | CMOS gates, delay | 6.1, 6.2.1 | |
| 11 | **2/9** | CMOS gates, power | 6.2.1 | HW #2 |
| 12 | **2/14** | Scaling intro + PVT; process corners notes | 3.4, 5.6 | |
| 13 | **2/16** | Dynamic logic, pass-transistor | 6.2.3 | Lab #3 |
| 14 | **2/21** | Dynamic logic, domino, np-cmos | 6.3, 6.4.1 | HW #3 |
| 15 | **2/23** | Comparisons between dynamic and CMOS | notes | |
| 16 | **3/07** | Low-power design techniques | 6.4.2, notes | Lab #4 |
| 17 | **3/09** | Wire parasitics | 4.3, 4.4 | |
| 18 | **3/14** | Interconnect issues; noise, RC delay | 9.2, 9.3 notes | HW #4 |
| 19 | **3/16** | Interconnect issues: repeaters | 9.3, notes | |
| 20 | **3/21** | Sequential elements: latches | 7.1, 7.2.1, 7.2.2 | |
| 21 | **3/23** | Sequential elements: flip-flops | 7.2.3, 7.2.5 | |
| 22 | **3/28** | Other sequential elements | 7.3.2, 7.5, 7.6 | |
| 23 | **3/30** | More Sequential Elements | notes | HW #5 |
| 24 | **4/04** | Memories, ROMs | 12.1, 12.2.1 | |
| 25 | **4/06** | Memories, SRAM | 12.2.3 | Design Project |
| 26 | **4/11** | Memories, DRAM | 12.2.3 | HW #6 |
| 27 | **4/13** | Course review | | |

**SYLLABUS OF EECS 312**

| Discussion Schedule | | |
|---|---|---|
| 01/06 | No Homework | |
| 01/13 | HW #1 | Due on: 1/24 |
| 01/20 | HW #1 | |
| 01/27 | Mat Lab | |
| 02/03 | HW #2 | Due on: 2/9 |
| 02/10 | HW #3 | |
| 02/17 | HW #3 | Due on: 2/21 |
| 02/24 | HW #4 | |
| 03/10 | HW #4 | Due on: 3/14 |
| 03/17 | Design Project | |
| 03/24 | HW #5 | Due on: 3/30 |
| 03/31 | HW #6 | |
| 04/07 | HW #6 | Due on: 4/11 |
| | | |