EECS 312
Digital Integrated Circuits

Instructor's Name:

Prof. Pinaki Mazumder
mazum@eecs.umich.edu
T,Th 3:00 – 4:30 pm

Overview

- Logistics –Go over syllabus & Course Overview
- Digital ICs are omnipresent: Applications
- The first computers were huge and slow
- Modern Microprocessors and DSP's
  - Trends of power, complexity, productivity
  - Moore's law
- Different styles of VLSI Chip Design
- **What I expect you to learn in this class**

Logistics 1

- Lecture Tuesday/Thursday Chrysler
- Syllabus
- **Website is at: https://ctools.umich.edu**
  *You need your **umich** password (not EECS!)*

- Friday discussion sections led by the GSI, Gregory Brandon
  - Review lecture topics, go through examples, answer questions
  - I may offer supplementary lectures during the discussion hours

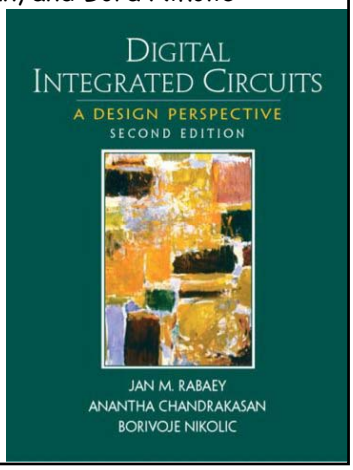
- Software labs – Eldo based
  - Will prepare you for future classes where Accusim is used
  - No set time for these labs – do on your own schedule
  - Lab Reports will be, however, due on the indicated dates

Logistics 2

Textbook:
Digital Integrated Circuits: A Design Perspective, 2nd edition by Jan Rabaey, Anantha Chandrakasan, and Bora Nikolic

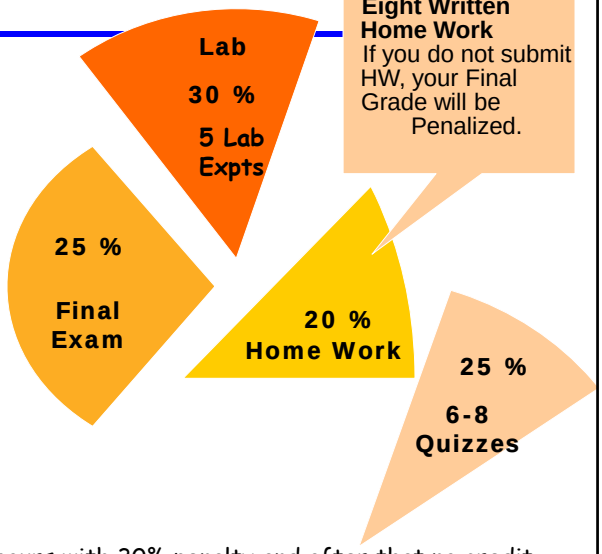
Lecture notes will be posted online a couple of days in advance before class sessions

I will supplement the ppt slides with handouts from other sources throughout the semester



Distribution of Points

- Pay 100% attention to lectures + Discussions
- Read class notes + Handouts regularly
- Try all Homework Problems
- Try all Lab Expts
- Do Design Project



Late Homework Policy: 24 hours with 30% penalty and after that no credit

Lecture	Date	Topic	Text	Homework
1	1/05	Course intro, digital IC overview	1.1, 1.2	
2	1/10	Overview of CMOS circuits	notes	
3	1/12	PN junction & MOSFET Theory I	3.3	
4	1/17	MOSFET Theory II	3.3	
5	1/19	CMOS fabrication	3.3, notes	HW #1
6	1/24	Device fab (cont.), scaling, SPICE models notes	2.2, 2.3	
7	1/26	CMOS inverter, VTC	5.1- 5.3	
8	1/31	CMOS inverter, delay analysis	5.4	HW #2
9	2/2	CMOS inverter, power analysis	5.5.1	
10	2/7	CMOS gates, delay	6.1, 6.2.1	
11	2/9	CMOS gates, power	6.2.1	HW #3
12	2/14	Scaling intro + PVT; process corners notes	3.4, 5.6	
13	2/16	Dynamic logic, pass-transistor	6.2.3	
14	2/21	Dynamic logic, domino, np-cmos	6.3, 6.4.1	HW #4
15	2/23	Comparisons between dynamic and CMOS	notes	
16	3/07	Low-power design techniques	6.4.2, notes	
17	3/09	Wire parasitics	4.3, 4.4	HW #5
18	3/14	Interconnect issues; noise, RC delay	9.2, 9.3 notes	
19	3/16	Interconnect issues: repeaters	9.3, notes	
20	3/21	Sequential elements: latches	7.1, 7.2.1, 7.2.2	HW #6
21	3/23	Sequential elements: flip-flops	7.2.3, 7.2.5	
22	3/28	Other sequential elements	7.3.2, 7.5, 7.6	
23	3/30	More Sequential Elements	notes	HW #7
24	4/04	Memories, ROMs	12.1, 12.2.1	
25	4/06	Memories, SRAM	12.2.3	
26	4/11	Memories, DRAM	12.2.3	HW #8
27	4/13	Course review		

All Pervasiveness of Digital Integrated Circuits

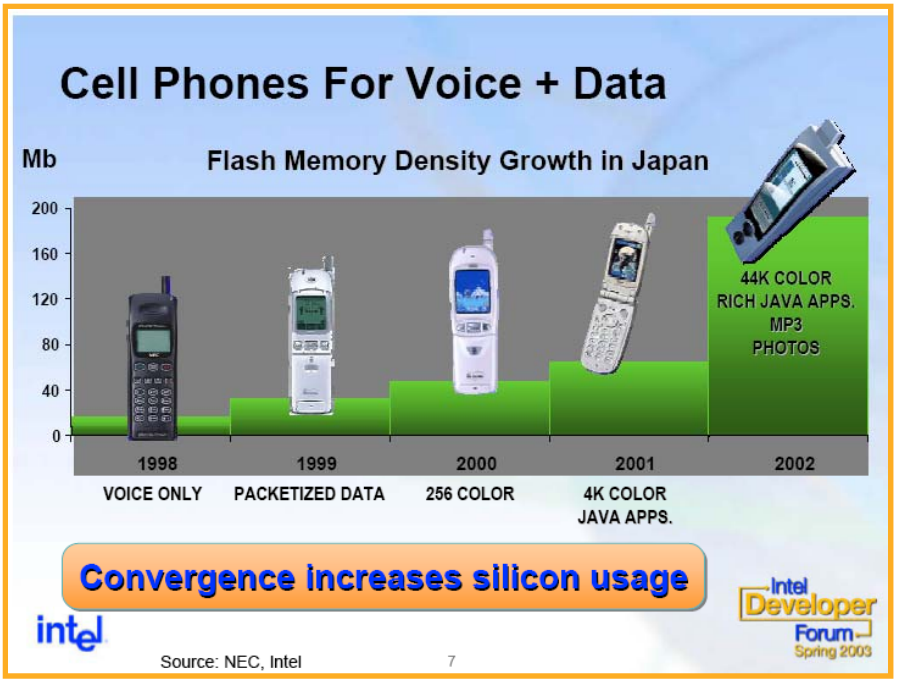
Global Market Size of Semiconductor Devices:
$250 Billion and heading towards $1 Trillion

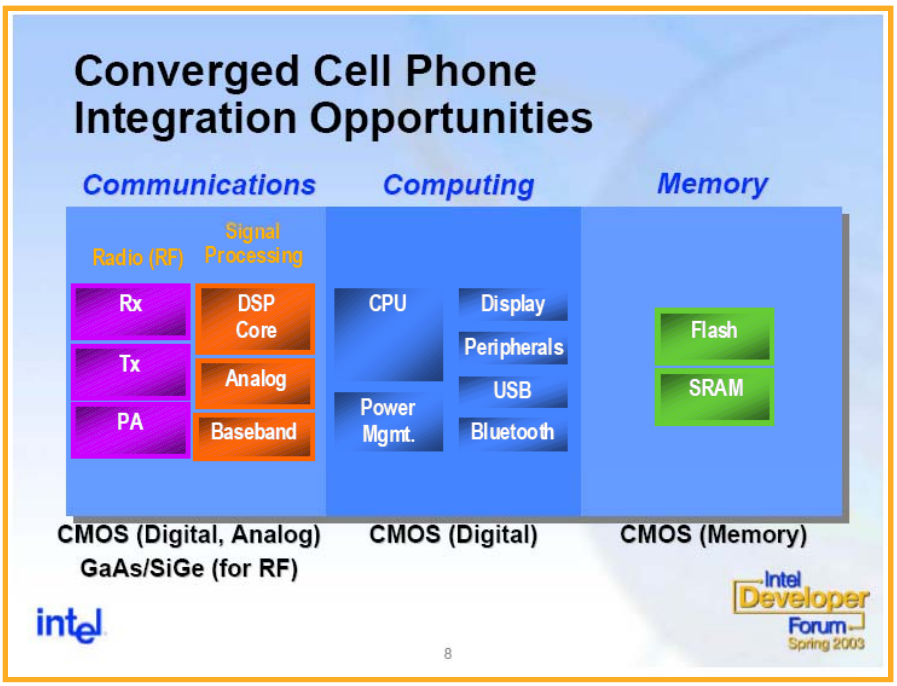
Consumer Electronics: Digital TV, DVD, PDA, Video Camera, Games, ….
Computers: Notebook, Desktop, Clustered PC's, …
Communications: Cell Phone, Answering Machines, …
Appliances: Washing Machine, Microwave Cooker, Thermostat, ….




Merging of Technologies

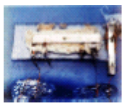
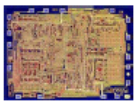
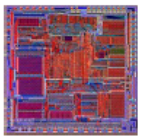
- Computers
  - Embedded Processors
  - Microcontrollers
- Communication
  - Cell Phone
  - Internet Voice Service
- Consumer Electronics
  - Video Camera
  - Personal Organizer
  - Games


Cell Phones For Voice + Data
Mb
Flash Memory Density Growth in Japan
200
160
120
80
40
0
1998
1999
2000
2001
2002
VOICE ONLY
PACKETIZED DATA
256 COLOR
4K COLOR
JAVA APPS.
44K COLOR
RICH JAVA APPS.
MP3
PHOTOS
Convergence increases silicon usage
intel
Source: NEC, Intel
7
Intel
Developer
Forum
Spring 2003

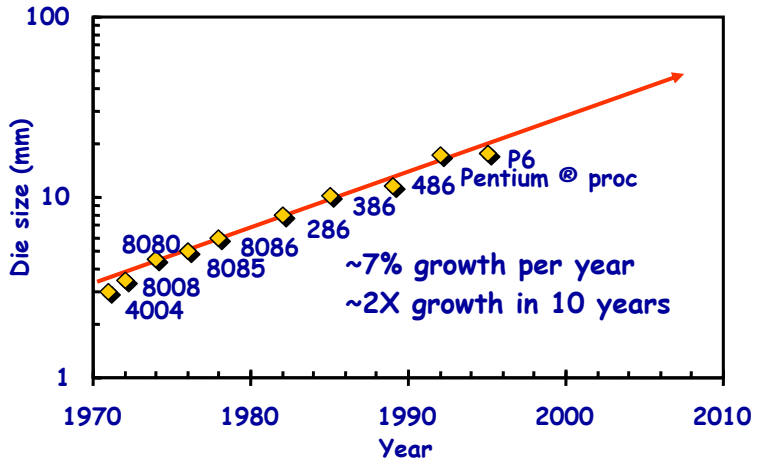

Converged Cell Phone
Integration Opportunities
Communications
Computing
Memory
Radio (RF)
Signal
Processing
Rx
Tx
PA
DSP
Core
Analog
Baseband
CPU
Power
Mgmt.
Display
Peripherals
USB
Bluetooth
Flash
SRAM
CMOS (Digital, Analog)
GaAs/SiGe (for RF)
CMOS (Digital)
CMOS (Memory)
intel
8
Intel
Developer
Forum
Spring 2003

Some History

Detailed History

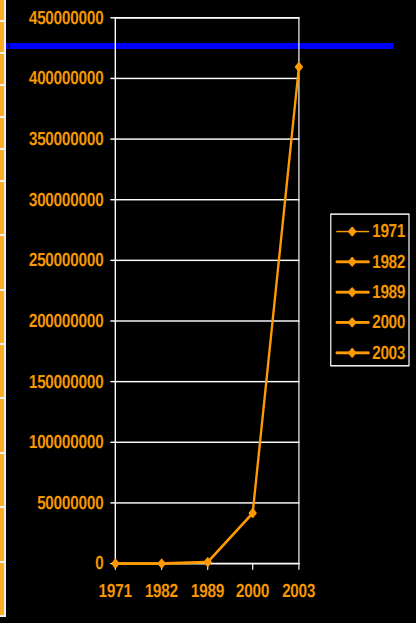
Invention of the transistor (BJT) Shockley, Bardeen, Brattain – Bell Labs	1947	
Single-transistor integrated circuit Jack Kilby – Texas Instruments	1958	
Invention of CMOS logic gates Wanlass & Sah – Fairchild Semiconductor	1963	
First microprocessor (Intel 4004) 2,300 MOS transistors, 740 kHz clock frequency	1970	
Very **L**arge **S**cale **I**ntegration Chips with more than ~20,000 devices	1978	

Larger chips to keep up with more transistors



Integration, Integration, and Integration

	Year of Introduction	Transistors
4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
Intel386™ processor	1985	275,000
Intel486™ processor	1989	1,180,000
Intel® Pentium® processor	1993	3,100,000
Intel® Pentium® II processor	1997	7,500,000
Intel® Pentium® III processor	1999	24,000,000
Intel® Pentium® 4 processor	2000	42,000,000
Intel® Itanium® processor	2002	220,000,000
Intel® Itanium® 2 processor	2003	410,000,000



Design Trends

- Smaller transistors
- Bigger chips (dies)
- Faster clock frequencies
- More complex designs
- Higher power consumption

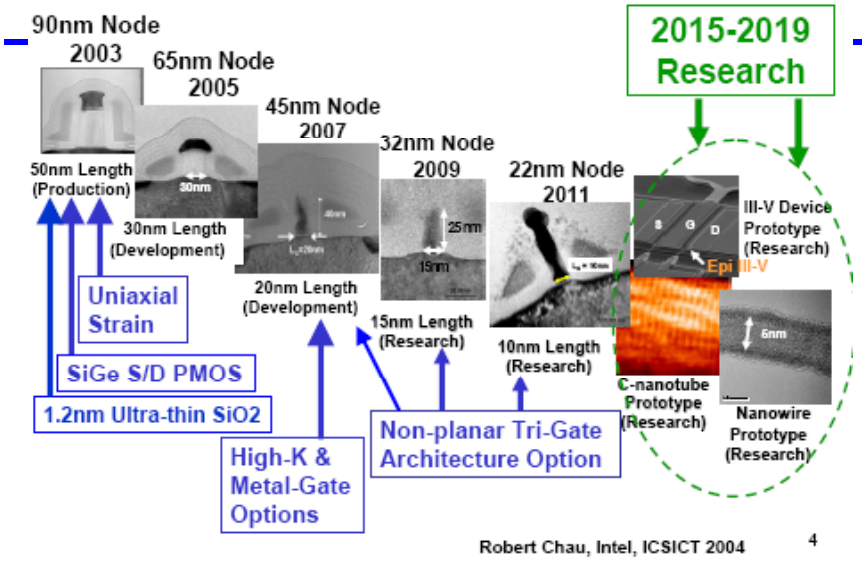
SIA Roadmap of IC Technology
---- The MARCH Continues

Year	1997	1999	2002	2005	2008	2011	2014
Channel length [nm]	250	180	130	100	70	50	35
Short wire Pitch [μm]	0.75	0.54	0.39	0.3	0.21	0.15	0.10
μP Chip Size [mm^2]	300	340	430	520	620	750	901
μP Transistors [10^6]	11	21	76	200	520	1400	3600
Global Clock [MHz]	375	1200	1600	2000	2500	3000	3674
Local Clock [MHz]	750	1250	2100	3500	6000	10000	17000
Dissipation [Watt]	70	90	130	160	170	175	183
Min Logic Vdd [V]	2.1	1.75	1.35	1.0	0.75	0.55	0.4
Wire length [km]	0.8	1.7	3.3	5	9.2	17	25
Wiring levels	6	6-7	7	7-8	8-9	9	10
ASIC Package Pins	1100	1400	1900	2600	3600	5000	6700
DRAM bits/chip	267M	1.07G	4.29G	17.2G	68.7G	275G	1.10T
μP cost/transistor	30	17	508	206	1.1	0.5	0.22

1
2
3
4

Transistor speed > 250 GHz
Circuit speed for μP < 10 GHz

Transistor Scaling and Research Roadmap



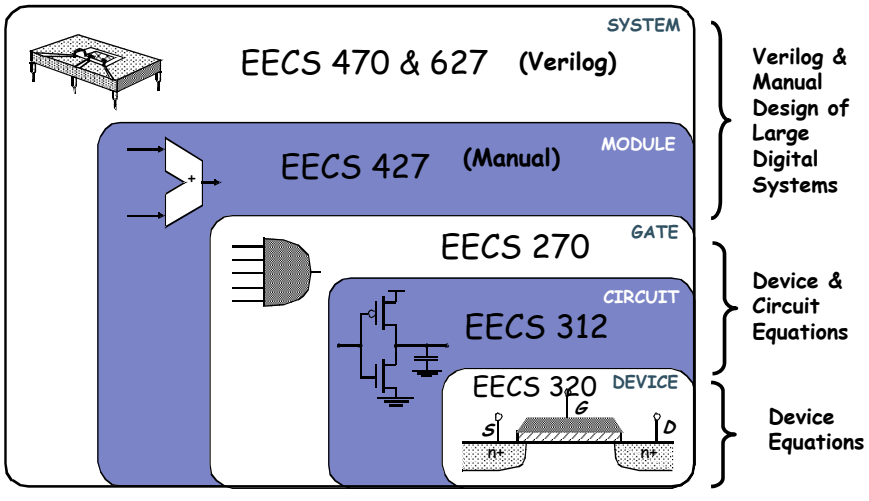
Robert Chau, Intel, ICSICT 2004 4

What does all this mean?

- Chips are getting bigger and harder to design
  - Hierarchical design flow
  - Good design principles needed
- Knowledge of fundamental design practices
- Ability to develop innovative design techniques

- This course is the first step in learning these design principles
  - Next step = 427, then 627, followed by Intel, IBM, or your own start-up

Design Abstraction Levels



What you will learn in this class

- Transistor level digital circuit design
- How to *design* and *analyze* the fundamental building blocks of all large-scale digital ICs
  - CMOS combinational gates
  - Sequential (storage) elements
  - Dynamic circuit families
  - Memories
  - Interconnect-related issues
- Based on the key quality metrics of circuit design:
  - Speed, area, power, cost, reliability

Reading Exercises

- **Read Sections 1.1 & 1.2 (pp. 4-15) of your textbook for subject matters of Today's Lecture**
- **Next lecture: Review of CMOS Logic operation**
- **Lecture Slides are posted. Study the Slides.**
- **Read in advance: Textbook pp. 87-115.**

EPILOGUE

Main Message of Today's Lecture:

- **CMOS Juggernaut will Continue to Scale down to 20 nm and beyond for another 15 to 20 years!**
- **No replacement of CMOS is in sight. Non-Silicon Nanotechnologies such as CNT, Moltronics, NMR, Ion-Trap Quantum Computing, … are only good for research.**
- **Device Physics, Higher Order Physical Effects, Circuit Analysis, Circuit Modeling to Account for Discrepancies Between Analytical Models and SPICE Simulations are Extremely Important for the Nano-scaled CMOS Chip Design. You must learn them in EECS 312 and EECS 427.**

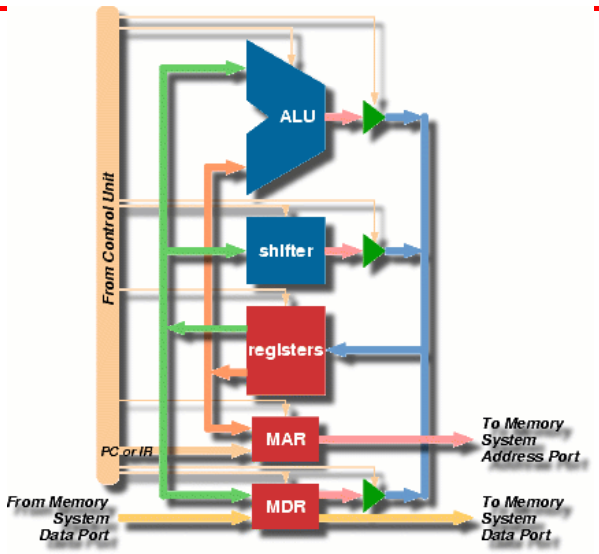
Lecture on Sequential Elements

Pinaki Mazumder

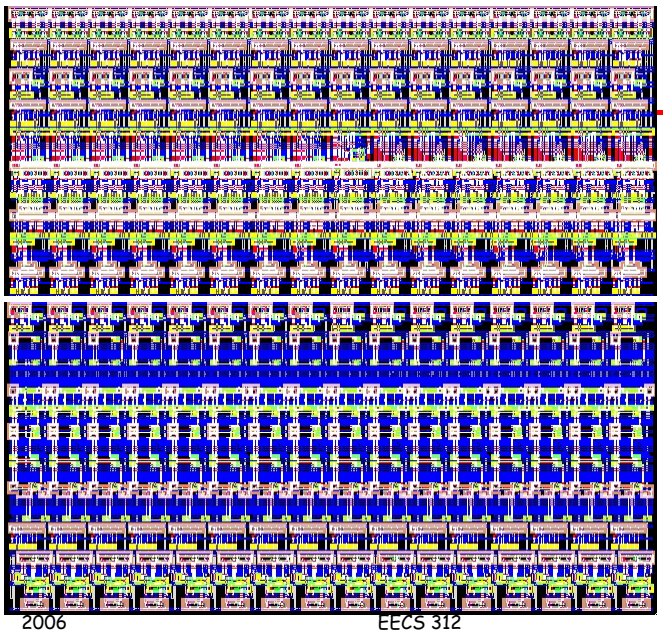
Lecture #20

EECS 312
Reading: 7.1.1, 7.2-7.3.1
Exclude 7.2.4

A TYPICAL PROCESSOR ARCHITECTURE

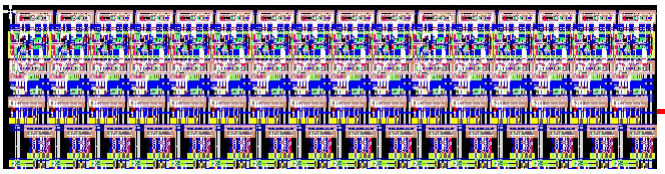


16-bit EECS 427 ISA Processor



ALU

Shifter

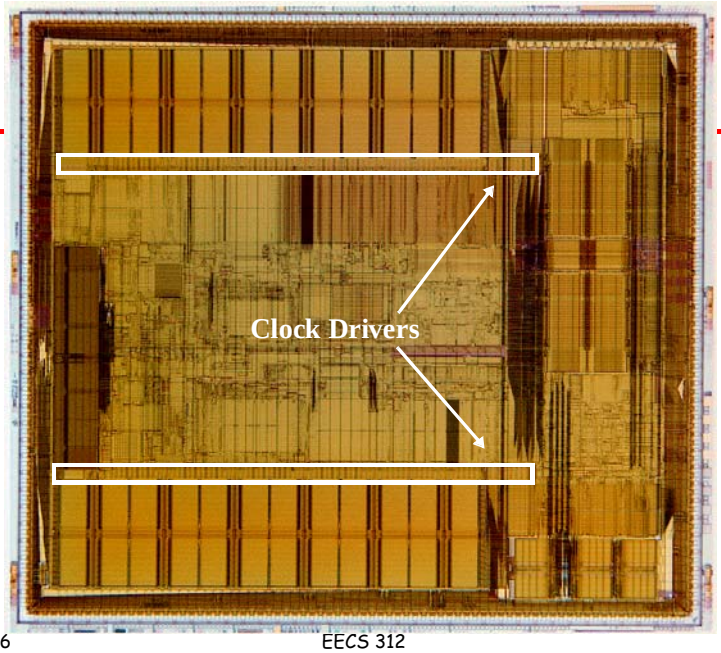


16-bit EECS 427
ISA Processor

Program Counter

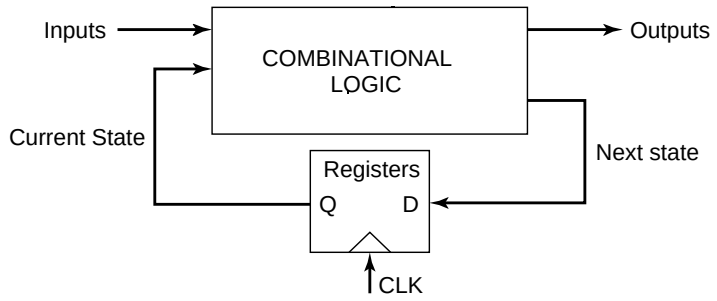
Register File

25



2006 EECS 312 26

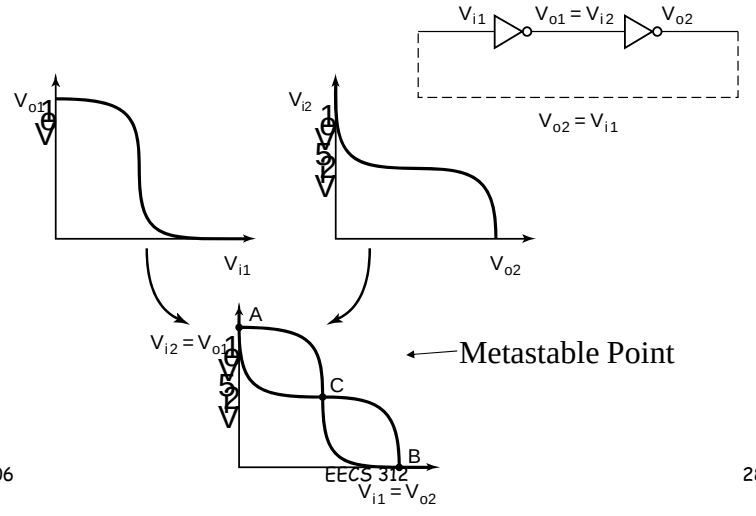
Sequential Logic



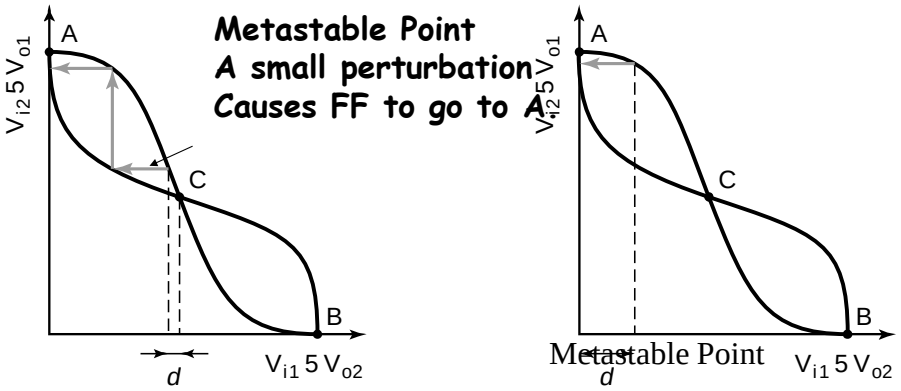
2 storage mechanisms

- **positive feedback** → Static
- **charge-based** → Dynamic

Positive Feedback: Bi-Stability



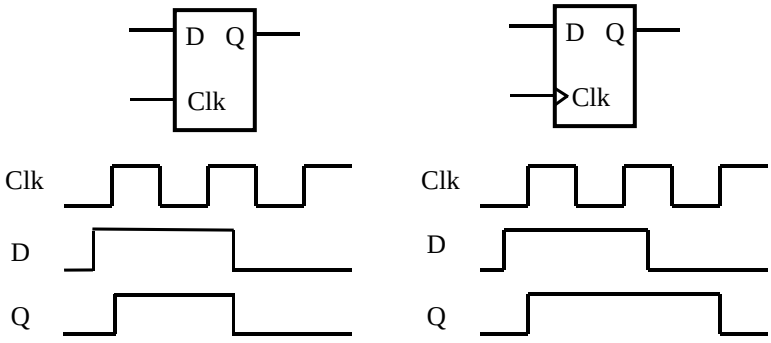
Meta-Stability



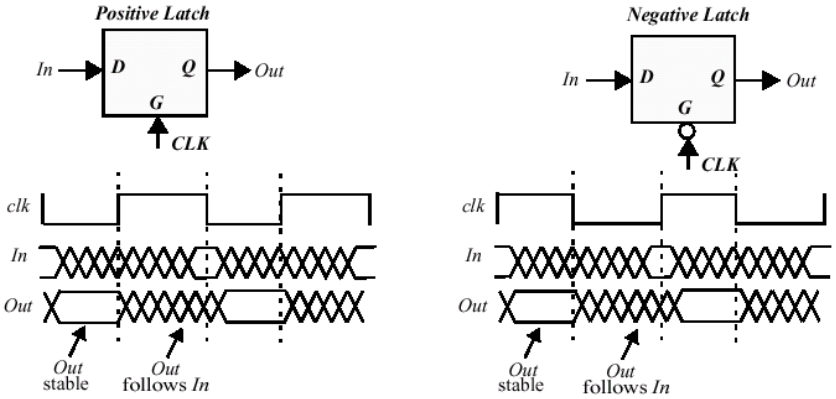
Gain should be larger than 1 in the transition region

Types of Sequential Elements

- Latch
  stores data when
  CLK is either high *or* low
- Register
  stores data when
  CLK rises/falls (edge-triggered)



Types of Latches

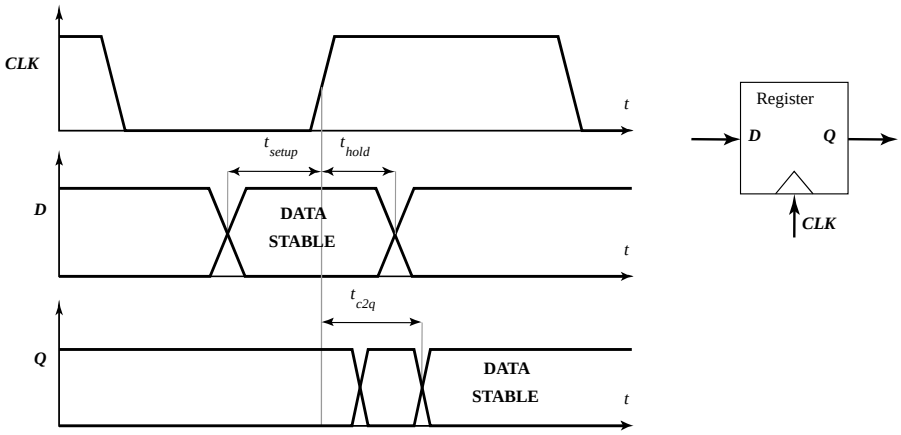


Level-sensitive – A transparent mode and an opaque mode depending on the level of CLK

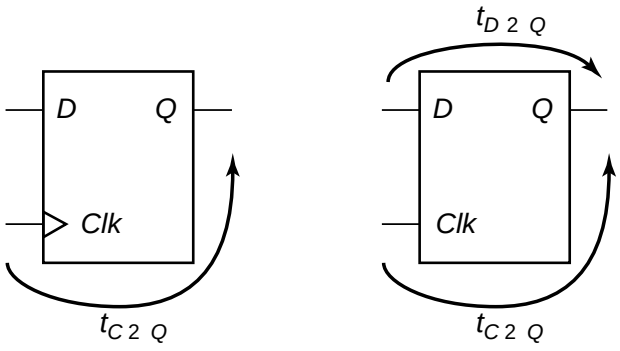
Timing Metrics

- Timing metrics for sequential elements differ from those of combinational logic
- Set-up time
  - Time that data must be valid before clock transitions
- Hold time
  - Time that data must remain valid after the clock edge
- Propagation delay
  - Can be measured from clock to Q or data to Q
  - Which is more meaningful? Depends…

Register: Timing Definitions



Characterizing Timing

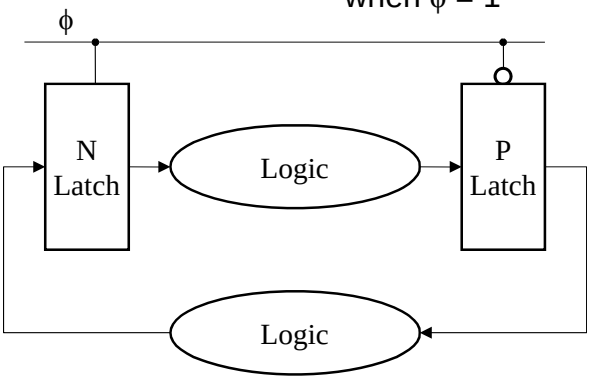


Register Latch

Latch-Based Design

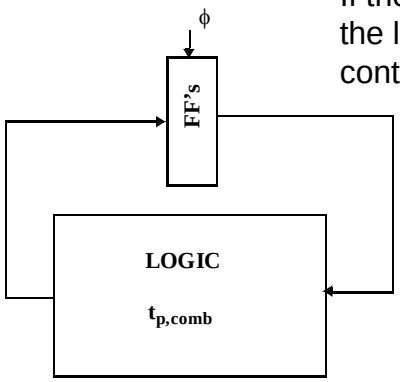
• N latch is transparent when $\phi = 0$

• P latch is transparent when $\phi = 1$



Maximum Clock Frequency

If the data "races" through the logic too fast, the data is contaminated



$t_{c\text{-}Q} + t_{p,comb} + t_{setup} = T$

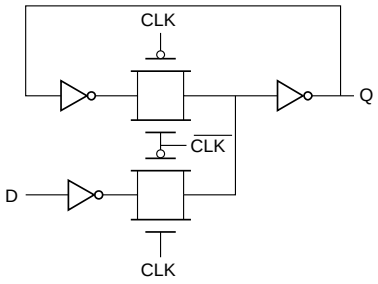
Also:
$t_{cdreg} + t_{cdlogic} > t_{hold}$

t_{cd}: contamination delay = minimum delay

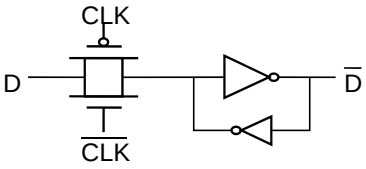
Usually $t_{cdreg} \sim t_{c\text{-}Q}$

Writing into a Static Latch

Use the clock as a decoupling signal that distinguishes between the transparent and opaque states



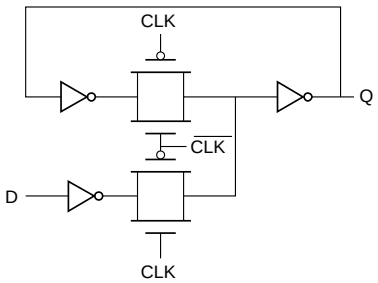
Converting into a MUX



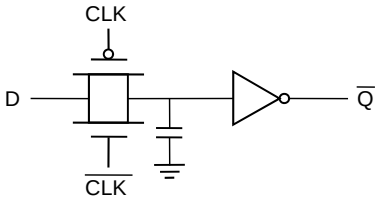
Forcing the state
(can implement as NMOS-only)

Storage Mechanisms

Static

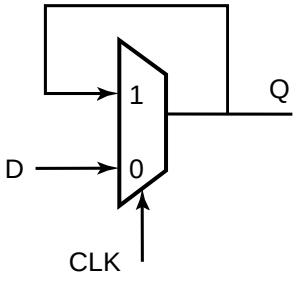


Dynamic (charge-based)



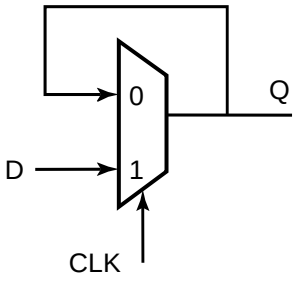
Mux-Based Latches

Negative latch (transparent when CLK= 0)



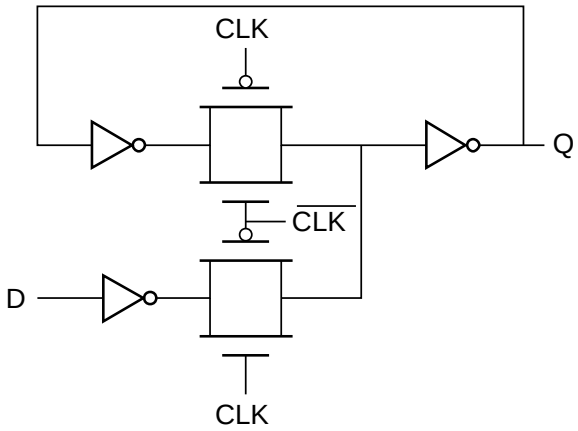
$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

Positive latch (transparent when CLK= 1)

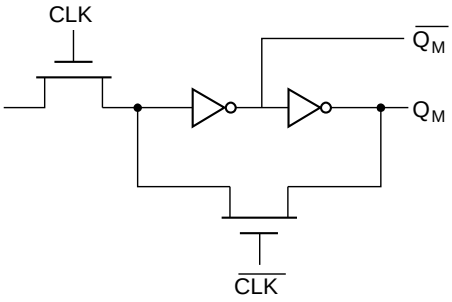


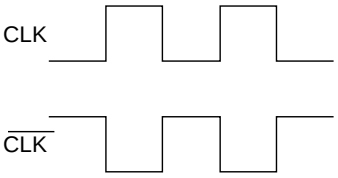
$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

T-gate Mux-Based Latch



Pass-transistor Mux-Based Latch

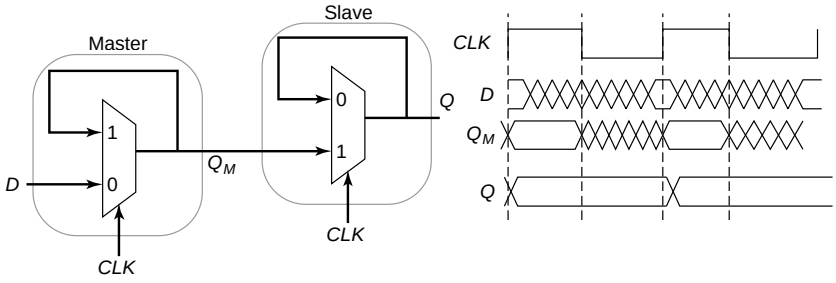




NMOS only

Non-overlapping clocks

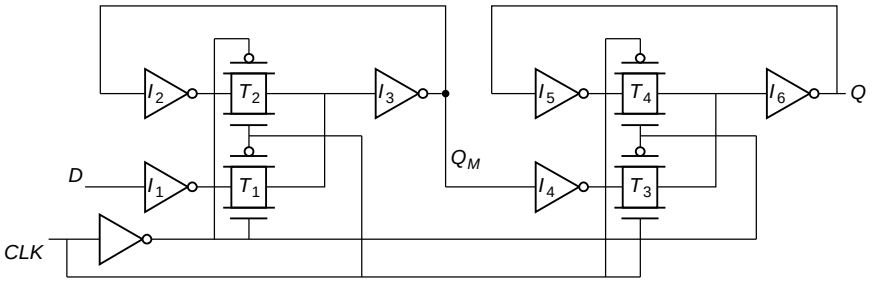
Master-Slave (Edge-Triggered) Register



Two opposite latches act to trigger on clock edge
Also called master-slave topology
Advantage: Transparency window is limited and more controllable
Disadvantage: Slower

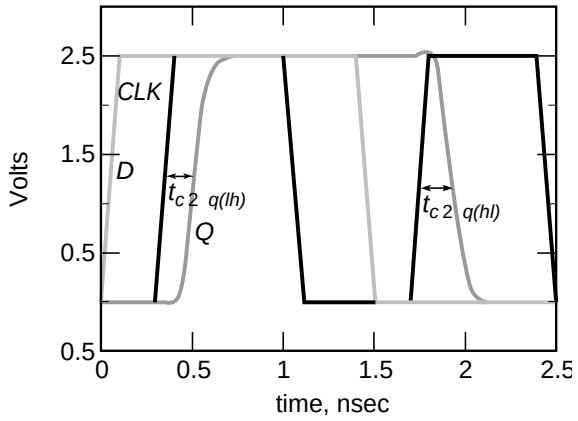
Master-Slave Register

Multiplexer-based latch pair

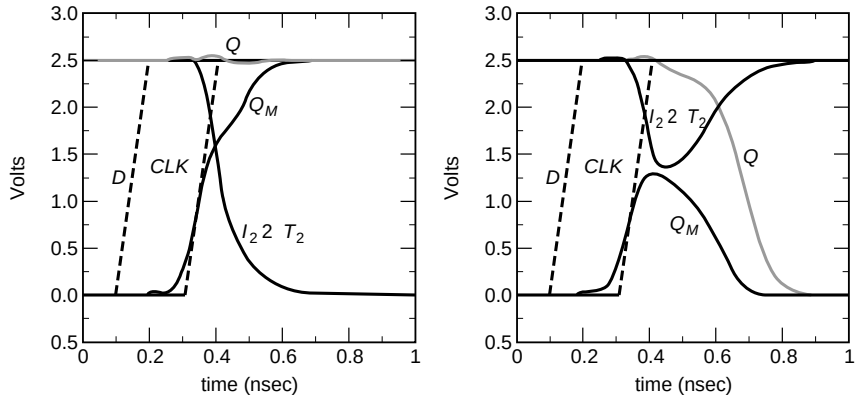


High clock load (high switching activity, large power)

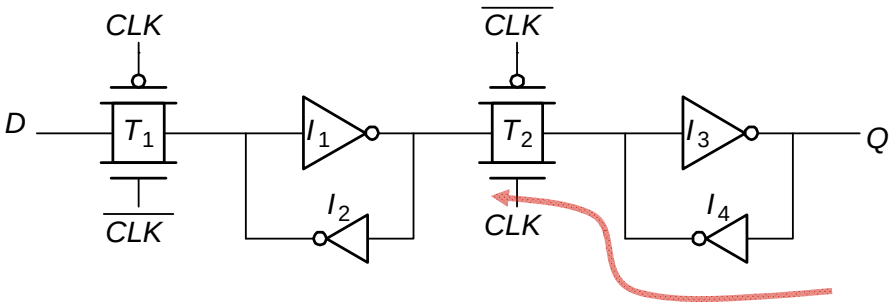
Clk-Q Delay



Setup Time Depiction



Reduced Clock Load Master-Slave Register



Only 2 T-gates and 4 INV

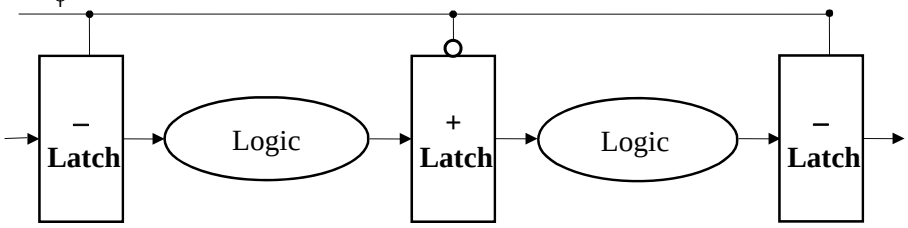
New data must now overpower the previously held state

Possible reverse conduction path (keep I_4 weak)

Latch-Based Design

– latch is transparent when $\phi = 0$

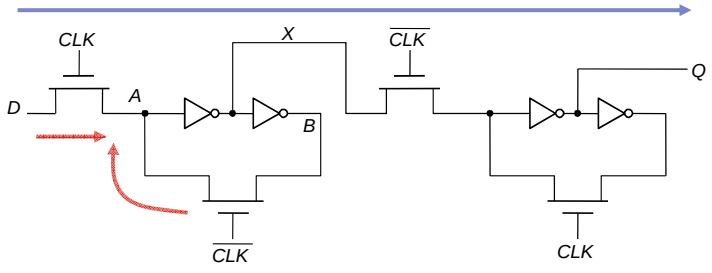
+ latch is transparent when $\phi = 1$



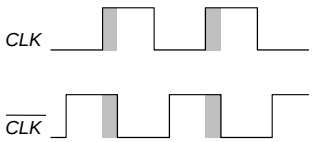
To avoid race conditions, we need to make sure that the clocks are completely non-overlapping

Otherwise consecutive latches may be transparent simultaneously

Avoiding Clock Overlap



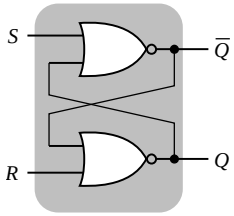
(a) Schematic diagram

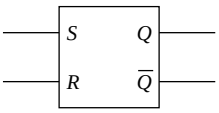


(b) Overlapping clock pairs

Overpowering the Feedback Loop

NOR-based set-reset





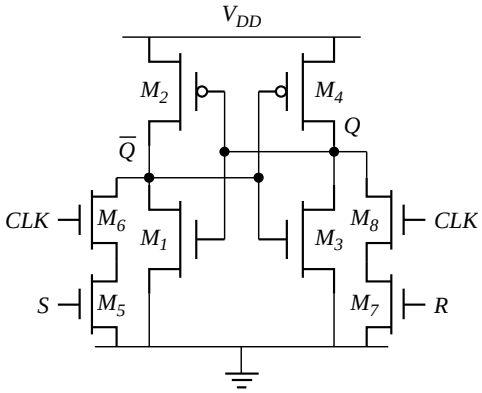
S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

Forbidden State

Cross-coupled NORs

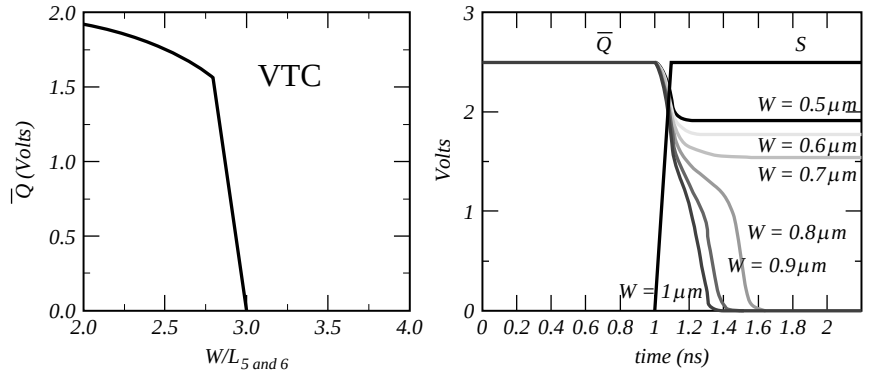
Clocked SR latch

Adding clock to synchronize



This is not used in datapaths any more, but is a basic building memory cell

Sizing Issues



$W/L_2 = 1.5$ (a)

(b)

Output voltage dependence on transistor width

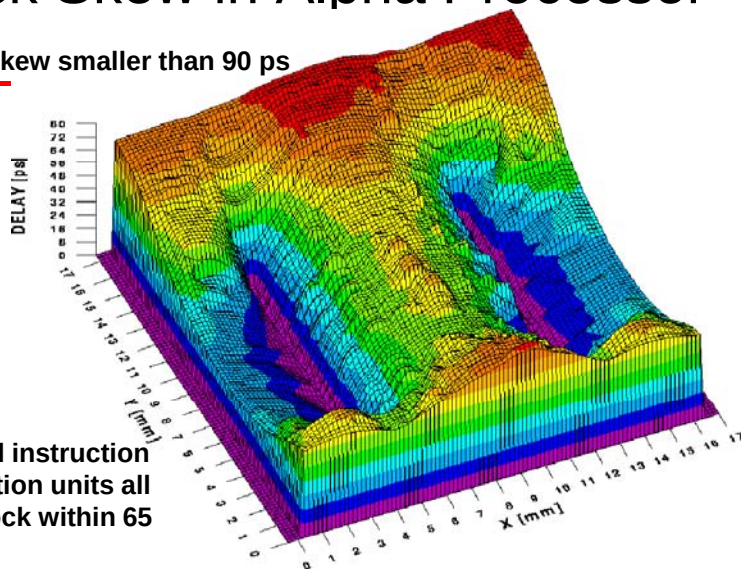
Transient response

Lecture Summary

- Latch topologies are based on cross-coupled inverter pairs to hold state
- New states are overwritten by either decoupling the pair (break the loop) or by overpowering the loop
  - Breaking the loop is cleaner (less contention, power) but results in more complex topologies
- Edge-triggered registers are slower than latches but are more robust/easy to design with since they are only transparent for a very limited duration

Clock Skew in Alpha Processor

- **Absolute skew smaller than 90 ps**



- **The critical instruction and execution units all see the clock within 65 ps**