C u r r i c u l u m V i t a e

August 2, 2020

Personal

Name: **Igor L. Markov** E.mail address: imarkov@umich.edu
WWW home page: http://www.eecs.umich.edu/~imarkov

Education

- Ph. D. in Computer Science, UCLA, 2001
- Master of Arts in Mathematics, UCLA, 1994.
- Diploma with Honors in Mathematics, Kyiv National University, 1994.

Work experience

Facebook, Menlo Park, CA, 2018- Research Scientist working on Newsfeed Integrity. Modeling online interactions with latent-space embeddings. Population-wide models of social phenomena based on patterns of online interactions. Behavioral reputation scores. ML classifiers for clickbait and engagement bait, as well as COVID-related text

Univ. of Michigan Ann Arbor, EECS Dept., 2012-2018 Full Professor.

Google, 2014 - 2017 Software Engineer working on Search.
Developed new types of multicriteria indexing and retrieval (US Patent 10235342B1), implemented in C++, launched in production worldwide. Was responsible for pre-release performance testing of flagship search products. Served on promo committee.

Stanford Univ., EE Dept., November 2013 - December 2014 Visiting Professor.
Taught EE 271 - Introduction to VLSI.

Moscow University, Dept. of Computational Mathematics and Cybernetics, May 2013 Visiting Professor.

Univ. of Michigan Ann Arbor, EECS Dept., 2006-2012 Associate Professor.

Synopsys, Inc., Sunnyvale, CA (NASDAQ: SNPS), May-August 2008 (via acquisition of Synplicity)
US Patents US8141024B2, US8453084B2, US8584071B2, US9285796B2

Synplicity, Inc., Sunnyvale, CA (NASDAQ: SYNP), January-May 2008 Principal engineer: ECAD algorithms and SW.

National Taiwan University, EE Dept., September-October 2007 Visiting Associate Professor.

Univ. of Michigan Ann Arbor, EECS Dept., 2000-2006 Assistant Professor.

UCLA, Computer Science Department, 1996-2000 Research in VLSI CAD. Research Assistant.

UCLA, Mathematics Department, 1994-96 Teaching Assist./Assoc.: College Mathematics and Computer Programming.

Parametric Technology Corp., Waltham, MA (NASDAQ: PMTC), 1995 SW engineer: solid-modeling CAD and computer graphics.

Professional societies: IEEE Fellow, ACM Distinguished Scientist

Honors, Awards and Selected Invited Lectures

- IBM University Partnership Award, **2001**.
- The *IEEE/ACM Design Automation Conference fellowship*, **2001**.
- Invited speaker at the IBM Annual All-site Meeting in Fishkill, NY **2001**.
- Invited papers/talks at *Int'l Symp. on Quality Electronic Design* **2003**, *Int'l Symp. on Physical Design* **2003** and *Int'l Workshop on Logic Synthesis* **2003**.
- Distinguished Lecture in Quantum Information Processing, *National Institute of Standards and Technology* (NIST), Radiation Physics Division, January **2004**.

- The **2004** *IEEE Circuits and Systems (CaS) Society Donald O. Pederson Award* (presented at DAC 2004) for the paper, "Synthesis of Reversible Logic Circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 6, pp. 710-722, June 2003 (with V.V. Shende, A.K. Prasad, and J.P. Hayes).
- Three-lecture tutorial at a summer school on symmetries in AI at the Univ. St. Andrews, Scotland, June **2004**.
- Invited speaker at the Intel research symposium in Haifa, Israel, June **2004**.
- The 2004 ACM *Special Interest Group on Design Automation (SIGDA) Outstanding New Faculty Award* (presented at ICCAD in November **2004**).
- *Best-paper award at DATE* **2005**, for the paper "Accurate Reliablity Evaluation and Enhancement via Probabilistic Transfer Matrices" by S. Krishnaswamy, G. F. Viamontes, I. L. Markov and J. P. Hayes.
- *NSF CAREER Award* **2005**.
- ACM Recognition of Service Award **2005**.
- Synplicity Inc. Faculty Award **2005**.
- ACM SIGDA *Technical Leadership Award* (presented at ICCAD in November **2005**).
- IEEE *Senior Member*, November **2005**.
- First place at the ISPD **2007** global routing contest.
- Invited talks at EDPS **2007**, **2008**, **2010**.
- ACM SIGDA, Advisory Board **2005-2006** and Executive Board **2007-2009**, Communications chair **2009-2012**.
- Invited attendee at the Google Faculty Research Summit in Mountain View, CA, July **2007**.
- ACM *Senior Member* **2007**, ACM Distinguished Scientist **2011**.
- A series of 8 invited lectures at Taiwan Universities in September-October **2007**: National Taiwan Univ. (EE/EDA, EE/CS and CSIE), National Cheng-Kung Univ. (EE and CS), Sun Yat-sen Univ. (CS), National Chiao Tung Univ. and Tsing-Hua Univ.
- Invited presentation at the meeting of the IEEE Kansai chapter in Kyoto, Japan, October **2007**.
- Invited talk at SASIMI 2007 in Sapporo, Japan, October **2007**.
- Communications of ACM (CACM) member of editorial board, January **2008**.
- EECS Outstanding Achievement Award from the Univ. of Michigan, January **2008**.
- Microsoft *A. Richard Newton* Breakthrough Research Award, March **2008**.
- Microsoft *A. Richard Newton* Breakthrough Research Award, March **2008**.
- Best-paper award at Int'l Symposium on Physical Design (ISPD), Portland, OR, April **2008** (with Steve Plaza and Prof. Valeria Bertacco).
- Invited talk at VTS 2008 in San Diego, CA, April **2008**.
- Invited mini-course on Physical Design of Integrated Circuits in Bento Gonçalves, Brazil, May **2008**.
- Invited speaker at the Intel research symposium in Haifa, Israel, June **2008**.
- Invited attendee at the Microsoft Faculty Research Summit in Redmond, WA, July **2008**.
- First place at the ISPD **2009** clock-network synthesis contest.
- ACM SIGDA Service Award **2009**.
- Presenter at the National Science Foundation workshop on the Future of Electronic Design Automation; Arlington, VA, July **2009**.
- IEEE CEDA Early Career Award **2009** for outstanding contributions to algorithms, methodologies and software for the physical design of integrated circuits, presented at ICCAD **2009**.
- First place at the ISPD **2010** clock-network synthesis contest.

- *Best-paper award* at the Int'l Conf. on Computer-Aided Design (ICCAD) **2010**, San Jose, CA.
- Panelist, session chair, panel organizer and invited workshop speaker at DAC **2011**.
- Invited tutorial presenter at ICCAD **2011** and **2012**.
- GSRC A. Richard Newton impact award **2012**.
- Best paper award at *the Turing Centenary Conference*, Manchester, UK, **2012**.
- First pace at the ICCAD **2012** place-and-route contest.
- IEEE *Fellow*, November **2012**.
- First and second places at the ISPD **2013** gate-sizing contest (in two categories resp.)
- A mini-course at Moscow State University, May **2013**.
- DAC *Prolific Author Award*, June **2013**.
- Invited talk at ML Conf, Seattle, May **2016**.
- Invited talk at AI Conf, San Francisco, June **2017**.
- Invited talk at Microsoft, Redmond, August **2018**.
- Invited talk at IBM TJ Watson Center, September **2018**.
- Invited talk at RIKEN-Berkeley symposium, Lawrence Berkeley Natioal Lab, January **2019**.
- Invited talk at Amer. Phys. Soc. meeting, March **2019**.
- *Top Writer*, Quora, **2013-2018**.
- Best-paper award nominations at DAC **1997**, ASPDAC **1999**, ASPDAC **2000**, DAC **2003**, DAC **2004**, DATE **2005**, ISPD **2006**, ISPD **2008**, ICCAD **2010**, ISPD **2011**, ICCAD **2011**, DATE **2012**, ISPD **2012**.

Honors and Awards Won by Students

- Arathi Ramani and Saurabh Adya: *Design Automation Conf. (DAC) fellowship*, **2001**
- DoRon Motter: *Motorola fellowship*, **2001**
- DoRon Motter: 1^{st} place at *ICCAD CADathlon* **2002**
- Vivek Shende and Aditya Prasad: *IEEE CaS Donald O. Pederson paper-of-the-year award* (IEEE Trans. on Computer-Aided Design), **2003**
- George Viamontes: *US Dept. of Energy High-performance Computing Fellowship*, **2003**
- Matt Hardy: 1^{st} place at the *student design contest at the Design Automation Conf.* (DAC) **2004**
- Saurabh Adya: *graduate mentorship award from the University of Michigan*, **2004**
- Hayward Chan: honorable mention from the *Computing Research Association* (CRA) for work on block-packing with symmetries, **2004**
- Gabe Black and Jarrod Roy: 1^{st} place at *ICCAD CADathlon* **2004** (shared with MIT)
- Smita Krishnaswamy and George Viamontes: best paper award at the *Design Automation and Test in Europe Conf.* (DATE) **2005**
- Jarrod Roy: 1^{st} place at *ICCAD CADathlon* **2005**
- Jarrod Roy: *Rackham Graduate fellowship*, **2006**
- Aaron Ng: Nominated for the best paper award at the *Int'l Symp. on Physical Design* (ISPD) **2006**
- Kai-Hui Chang and David Papa: 1^{st} place at the *IWLS* **2006** *Implementation Challenge*
- Jin Hu: *Rackham Graduate fellowship*, **2006**
- Kai-Hui Chang and George Viamontes: 2^{nd} place at *ICCAD CADathlon* **2006**

- Jarrod Roy: winner of the *ISPD* **2007** *routing contest* (1^{st} place in the 2D category, 3^{rd} place in the 3D category)
- Michael Moffitt: winner of the *ISPD* **2007** *routing contest* (1^{st} place in the 3D category, 2^{nd} place in the 2D category)
- Michael Moffitt: winner of the *IBM Joseph Raviv postdoctoral fellowship*, **2007**
- Smita Krishnaswamy and Steve Plaza: 2^{nd} place at the *IWLS* **2007** *Implementation Challenge*
- Héctor Garcia: *Rackham Graduate fellowship*, **2007**
- Kai-hui Chang: *EDAA Outstanding Ph.D. Dissertation Award*, presented at DATE **2008** in Munich, Germany.
- Steve Plaza: *best paper award* at the Int'l Symposium on Physical Design (ISPD) **2008**, Portland, OR.
- Dongjin Lee: 1^{st} place at the *ISPD* **2009** *clock-network synthesis contest* in San Diego, CA.
- Kai-hui Chang: *ACM SIGDA Outstanding Ph.D. Dissertation Award*, presented at DAC **2009**, San Francisco, CA.
- Hector Garcia: 1^{st} Place in Technical Paper Competition at *SHPE* **2009** in Washington, DC.
- Smita Krishnaswamy: *EDAA Outstanding Ph.D. Dissertation Award*, presented at DATE **2010** in Dresden, Germany.
- Dong-Jin Lee and Myung-Chul Kim: 1^{st} place at the *ISPD* **2010** *clock-network synthesis contest*, San Francisco, CA.
- Dong-Jin Lee and Myung-Chul Kim: *best paper award* at the Int'l Conf. on Computer-Aided Design (ICCAD) **2010**, San Jose, CA.
- Dong-Jin Lee and Myung-Chul Kim: 2^{nd} place at the ICCAD **2010** CADathlon contest, San Jose, CA.
- David Papa: *EDAA Outstanding Ph.D. Dissertation Award*, presented at DATE **2011** in Grenoble, France.
- Jin Hu: *Outstanding Graduate Student Instructor Award*, **2011**
- Héctor Garcia: *Rackham Centennial fellowship*, **2012**
- Myung-Chul Kim, Jin Hu and Dong-Jin Lee: 1^{st} place at the *ICCAD* **2012** *place-and-route contest* organized by IBM Research
- Pankit Thapar and Benjamin vander Sloot: 1^{st} and 2^{nd} places at the *ISPD* **2013** *gate-sizing contest* organized by Intel Labs
- Daniel MacLennan, Peter Xie and Andrew Segavac: 3^{rd} place at the *ICCAD* **2013** *logic-synthesis contest* organized by Cadence Design Systems

Research interests

- Machines that make machines
- Algorithms, tools and methodologies for Electronic Design Automation, including 3D integrated circuits
- Information retrieval
- Machine learning
- Algorithms for search and combinatorial optimization
- Numerical methods
- Quantum information and computation
- Intellectual property protection and IC security

Teaching interests

Undergraduate	Graduate
Algorithms and Data Structures, Digital Electronics	Analysis and Design of Algorithms
Object-oriented programming, Graph Algorithms	CAD for VLSI, Combinatorial Optimization
Discrete Mathematics, Mathematical Programming	Quantum Information Processing

- Guided graduate student seminars on (i) quantum computing,
  (ii) physical synthesis, verification and test of integrated circuits
- Taught large undergraduate courses on logic circuits, VLSI, algorithms and data structures, etc.

Professional Service

SERVICE AT GOOGLE

- Promotions committee
- Performance monitoring for Search

SERVICE AT THE UNIVERSITY OF MICHIGAN

- Member of the Fulbright Committee, 2001
- Undergraduate student advisor at the Department of EECS, 2001-2003, 2017-2018
- Member of the Computing Infrastructure committee at the Department of, EECS 2003-2005
- Member of the Graduate Committee at the CSE Division, 2005-2006
- Internal referee for fivefaculty/lecturer reviews, 2005-2016
- Member/chair of major review committees at the CSE Division, 2006, 2008, 2009, 2017
- Member of a major review committee at the ECE Division, 2011
- Chair of the undergraduate program in Computer Engineering, 2006-2013
- Chair of the undergraduate program in Computer Science (LSA), 2015
- Member of the Research Strategy Committee at the College of Engineering, 2007
- Member of the committee reviewing graduate programs in Computer Science and Engineering, 2011
- Member of the committee reviewing the Computer Science/LSA program, 2011
- Director of the Sun Microsystems *Center of Excellence* at the University of Micigan, 2007-2009
- College of Engineering Representative for several faculty candidates
- Member of the University-wide committee on Augmented, Virtual and Mixed reality, 2017-2018
- Member of several dozen Ph.D. committees at the EECS, IOE and Mechanical Engineering Departments
- Member of qualifying examination committees (every semester)
- Also see **Work with Graduate and Undergraduate Students** below

MEMBERSHIP IN OFF-CAMPUS DISSERTATION AND THESIS COMMITTEES

- Universidade Federal do Rio Grande do Sul (UFGRS), Porto Alegre, Brazil
  Doctoral Committee for *Renato Hentschke* — June 2007
- University of Michigan Dearborn; Master's Thesis Committee for *Héctor Garcia* — August 2007
- University of Waterloo, Canada, Doctoral Committee for *Kristofer Vorwerk* — July 2009
- University of Toronto, Canada, Doctoral Committee for *Marcel Gort* — March 2014
- EPFL, Switzerland Doctoral Committee for *Ana Petkovska* — June 2017

EDITORIAL ASSIGNMENTS

- Member of the Editorial Board of *ACM Journal on Emerging Technologies in Computing*, 2010-2014
- Member of the Editorial Board of *IEEE Design & Test*, 2009-current.
- Member of the Editorial Board of *Communications of ACM*, 2008-curent.
- Member of the Editorial Board of *IEEE Transactions on Computer-Aided Design*, 2008-2013
- Member of the Editorial Board of *IEEE Transactions on Computers*, 2007-2011.
- Associate Editor of *ACM Transactions on Design Automation of Electronic Systems* (TODAES), 2007-2011
- Guest Editor, *Integration: the VLSI Journal*, 2005-2006
- Editor of the *ACM SIGDA newsletter* (over 2,700 subscribers), 2005-2007;
  Associate Editor, 2002-2005. Contributed the article "*What is Post-Silicon Debug?*" (May 2008)

- Editor of the online *GSRC Bookshelf for CAD Algorithms* `http://vlsicad.eecs.umich.edu/BK`, 2000-2007.

OTHER BOARD & TASK FORCE MEMBERSHIPS

- *IEEE committee for selecting IEEE Fellows*, 2014-2015, 2018-2020
- *ACM committee on Ethics an Plagiarism*, 2014-2017
- *ACM Computing Classification System* Committee, chair of the Hardware track, 2011
- *ACM Special Interest Group on Design Automation* (SIGDA) advisory board, 2005-2006, Executive Board, 2007-current (re-elected in 2009)
- Chair of the SIGDA Technical Committee on Emerging Technologies in Computing, 2010-2011
- *NSF workshop on the Future of Electronic Design Automation*, Arlington, VA, 2009
- *ACM Task Force on revitalizing the Communications of the ACM* (organized by ACM Pres. David Patterson, chaired by Prof. Moshe Vardi), 2007
- SIGDA liaision to the CADathlon programming contest at ICCAD, 2006
- *Digital Logic* advisory board with McGraw Hill Corp., focusing on undergraduate courses in Digital Logic, 2005-2006
- *ACM Student Research Competition* at DAC 2010 (judge)

ORGANIZATIONAL ACTIVITIES AND PROGRAM COMMITTEE CHAIRMANSHIPS

- Moderator for *Emerging Technologies*, Computing Research Repository CoRR (http://arxiv.org/corr) (2011-)
- Topic chair for IC Physical Design at *ACM/IEEE Design Automation and Test in Europe Conf.* (DATE) 2009-11
- Topic chair for New, Emerging, Specialized Design Technologies *ACM/IEEE Design Autom. Conf.* (DAC), 2009-2010
- Topic chair for VLSI Floorplanning and Placement *ACM/IEEE Int'l Conf. on Computer-Aided Design* (ICCAD) 2010
- Track chair for Post-CMOS VLSI, *ACM Great Lakes Symposium on VLSI* (GLSVLSI), 2009-2011
- *ACM Int'l Workshop on Logic and Synthesis* (IWLS): publications chair (2008), special sessions chair (2009), general chair (2010), technical program committee co-chair (2011)
- Vice-chair for Tools and Methodologies at *IEEE Intl. Conf. on Computer Design* (ICCD), 2005
- Co-founder of the *ACM/IEEE Intl. Workshop On System-Level Interconnect Prediction* (SLIP), served as publicity chair, publication chair, special sessions chair (2000-2003) program committee chair (2004) and general chair (2005)
- Organizer of special sessions at the *ACM/IEEE Design Automation Conference* 2003, 2006, 2009 and 2010
- Session chair/moderator: DATE 2003-04,2008; SLIP 2000-05,2007; ISPD 2002-03,2005,2008-11; ISCAS 2002-03; ICCAD 2003-05, 2007; ASPDAC 2007; ICCAD 2007; ISPD 2010, DAC 2011

MEMBERSHIP IN PROGRAM COMMITTEES

- *ICCAD* tutorial selection committee, 2011
- *ACM TODAES* best-paper selection committee, 2008, 2010 (chair)
- *NanoArch* best-paper selection committee, 2009
- *ACM/IEEE Design Autom. Conf.* (DAC), 2004-05 (Placement and Floorplanning), 2006,2009-10 (Emerging Tech.)
- *ACM/IEEE Design Automation and Test in Europe* (DATE) Conf., 2003-2005 (Physical Design), 2007 (Circuit Test), 2008-2011 (Physical Design), 2014-2016, 2018-2019 (Physical Design and Logic Synthesis)
- *ACM/IEEE Asia and South Pacific Design Autom. Conf.* (ASPDAC), 2008,09 (Verification)
- *IEEE Symp. on Defect and Fault Tolerance in VLSI Systems* (DFT), 2008,09
- *ACM/IEEE Intl. Conf. on Computer-Aided Design of Integrated Circuits* (ICCAD), 2003-2005, 2009-2010
- *ACM/IEEE Intl. Symposium on Physical Design* (ISPD), 2002-2005, 2008-2011, 2018
- *The Satisfiability Symposium* (SAT), 2010-11

- *IEEE/ACM Symposium on Nanoscale Architecture* (NanoArch), 2007-2010
- *Intl. Symmetry Conference* 2007
- *ACM International Conference on Computing Frontiers* 2007
- *ACM/IEEE Great Lakes Symposium on VLSI* (GLSVLSI), 2002-04,2009-11
- *AAAI Workshop on Symmetry in Constraint-Satisfaction Problems* (SymCon), since 2003-2009
- *ACM/IEEE Intl. Workshop on Logic and Synthesis* (IWLS), since 2002
- *ACM/IEEE Intl. Workshop On System-Level Interconnect* (SLIP), since 1999
- *Workshop on Theory of Quantum Computation, Communication and Cryptography* (TQC), 2008.
- *IEEE DATC Electronic Design Processes Workshop* (EDP) 2008-
- *IEEE Workshop on Design and Test of Nano Devices, Circuits and Systems* (NDCS), 2008
- *Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms* (ERDIAP), 2011

REVIEWING, REVIEW PANELS, REFERENCES

- Book reviews for MIT Press, Cambridge Univ. Press, Oxford Univ. Press
- Proposal reviewer/panelist at the US National Science Foundation (NSF) and the US Dept. of Defense (DoD), Proposal reviewer for Nat'l Sciences and Engneering Research Council Canada (NSERC), Proposal reviewer for the Research Competitiveness Service (RCS) of American Association for the Advancement of Science (AAAS)
- IEEE senior member review panelist
- Reviewer for journals and Magazines: *ACM Transactions on Design Automation, ACM Transactions on Reconfigurable Systems, ACM Journal of Emerging Technologies in Computing, AIMS Advances in Mathematics and Communications, Nature, Nature Physics, APS Physical Review A, Journal of Statistical Physics, IOP Journal of Physics A: Mathematical and Theoretical, New Journal of Physics, IEEE Transactions on Computers, IEEE Transactions on CAD, IEEE Transactions on VLSI, IEEE Transactions on Circuits and Systems I, IEEE Transactions on Circuits and Systems II, IEEE Transactions on Information Forensics and Security, IEEE Transactions on Nanotechnology, IEEE Transactions on Nanobioscience, IEEE Design and Test, Nature Photonics, Quantum Information and Computation, Quantum Information Processing, Theoretical Computer Science, Discrete and Applied Mathematics, Constraints, Annals of Operations Research, IEE Proceedings: Computers and Digital Techniques, IEE Proceedings: Circuits, Devices and Systems, IEE Electronic Letters, Journal of Electronic Testing, Journal of Universal Computer Science, IOP Journal of Physics A: Mathematical and Theoretical, Journal of Multiple-Valued Logic and Soft Computing, Journal of Formal Methods in System Design, Journal of Parallel and Distributed Computing, Integration: the VLSI Journal, Microelectronics Journal, International Journal of Electronics, The Computer Journal*
- Reviewer for conferences: *ACM/IEEE Design Automation Conf. (DAC), ACM/IEEE Intl. Conf. on Computer-Aided Design (ICCAD), IEEE/ACM Design Automation & Test in Europe (DATE), IEEE/ACM Intl. Symposium on Circuits and Systems (ISCAS), ACM Intl. Symposium on Computer Architecture (ISCA), ACM Architectural Support for Programming Languages and Operating Systems (ASPLOS), AAAI Intl. Joint Conf. on Artificial Intelligence (IJCAI), Uncertainty in Artificial Intelligence (UAI), International Test Conference (ITC), Quantum Information Processing (QIP)*
- Reference for internal promotions at IBM, 2007, 2008
- Reference for univ'ty appointments and tenure promotions at top universities in the US, Canada, Australia, China, Israel.

MISCELANEOUS SERVICE

- Co-developed (with Dr. Lou Scheffer from Cadence) a software system for DUplicate text DEtection (DUDE) that has been used by all major ACM SIGDA conferences and IEEE Transactions on Computer-Aided Design to filter submitted manuscripts. For more details, see `http://sigda.eecs.umich.edu/DUDE/`

Research Funding

- Int'l Business Machines Corp. (IBM), **2000-2003**.
- Defense Advanced Projects Agency (DARPA), *Quantum Information Science and Technology*, **2001-2005**.
- Semiconductor Industry Association (SIA/MARCO) and DARPA via *the Gigascale Silicon Research Center* (GSRC), **2001-2006**.
- National Science Foundation (NSF) *Information Technology Research* (ITR), **2002-2006**.
- National Science Foundation (NSF) *Computer Architecture* (CA), **2002-2005**.
- Synplicity, Inc., **2003-2008**.
- National Science Foundation (NSF) *Design Automation* (DA/SGER), **2003-2004**.
- National Science Foundation (NSF) *CAREER*, **2005-2010**.
- Univ. of Michigan, Division of Computer Science and Engineering, *High-visibility Projects in CSE*, **2004-2005**.
- AirForce Research Laboratory (AFRL), **2006-2013**.
- University of Michigan, Undergraduate Research Opportunity (UROP) **2006-2007**.
- IEEE Council on EDA via *MP Associates*, **2007**.
- Microsoft Corp., **2008**.
- Sun Microsystems, **2008, 2009**.
- eASIC, **2009**.
- Texas Instruments, **2009**.
- National Science Foundation (NSF), *EAGER* **2009-2011**.
- National Science Foundation (NSF), **2012-2015**.
- Semiconductor Research Corp. (SRC), **2012-2015**.
- Mentor Graphics, **2012-2013**.
- Equipment donations from IBM (**2002**), Intel (**2004, 2008**), Altera (**2005**), AMD (**2006**) and Sun (**2007-2008**).

Work with Graduate Students

- Graduated twelve Ph.D. students – Dr. Arathi Ramani (Microsoft), Dr. Saurabh Adya (Synopsys), Dr. George Viamontes (Lockheed Martin), Dr. Kai-hui Chang (Avery Design Systems), Dr. Steve Plaza (Synopsys Advanced Technology Group), Dr. Smita Krishnaswamy (IBM Research, Columbia U., Yale U.), Dr. Jarrod Roy (IBM Austin), Dr. David Papa (IBM Research / ARL), Dr. Dongjin Lee (Samsung Group), Dr. Myung-Chul Kim (IBM Research / ARL), Dr. Jin Hu (IBM Corp), Dr. Hector J. Garcia (Amazon, Ameritrade, Univ. of Michigan)

Work with Undergraduate Students

- Organized research projects for six freshmen and sophomores under the Undergraduate Research Opportunity Program (UROP) at the University of Michigan in AY 2006/2007.
- Organized directed studies projects (EECS 499) and summer research projects (SURE) for 20+ talented undergraduate students. Some of them are now employed at Amazon.com, Google.com, Microsoft, Dept. of Defense, Toyota Research, and some went to graduate school at Stanford, Princeton, UT Austin, and Univ. of Michigan.
- Shared the 2004 Donald O. Pederson "paper-of-the-year" award (presented at DAC) with two undergraduates Vivek Shende and Aditya Prasad (now at Princeton/Math and Amazon.com resp.)
- Together with undergraduate co-authors, published three peer-reviewed workshop papers (IWLS 2002-03, 2014 and SymCon 2003), conference papers (ICCAD 2002, DATE 2004, DATE 2013, SPIE QIC 2004, GLSVLSI 2004, ICCAD 2014), and journal papers (IEEE Trans. on CAD, Quantum Information and Computation, APS Physical Review A).
- Undergraduate student Hayward H. Chan received an honorable mention from CRA in Fall 2004 for his work on block packing with symmetries.
- Provided reference letters to a number of undergraduate students applying to graduate school, as well as for various awards and scholarships.

Patents and Patent Applications:

- I. L. Markov and K. S. McElvain, US Patent 8,141,024, "Temporally Assisted Sharing in Electronic Systems", issued Mar 20, 2012.
- K.-H. Chang, I. Wagner, I. L. Markov, and V. Bertacco, U.S. Patent 8,365,110, "Automatic Error Diagnosis and Correction for RTL Designs," issued Jan 29, 2013.
- I. L. Markov and K. S. McElvain, US Patent 8,453,084, "Approximate Functional Matching in Electronic Systems" issued May 28, 2013. vspace-1mm
- J. A. Roy, I. L. Markov, F. Koushanfar US Patent 8,732,468, "Protecting Bus-based Hardware IP by Secret Sharing," issued May 20, 2014.
- Hector J. Garcia and I. L. Markov, US Patent 9,477,796, "Methods for general stabilizer-based quantum computing simulation," Oct 25, 2016
- I. Markov and A. Csomai, US Patent 10235432B1, "Document retrieval using multiple sort orders," Mar 19, 2019

Publications:[1]

Electronic versions are at `http://www.eecs.umich.edu/~imarkov/pubs/`

Books and Book Chapters (dissertations not included)

B15. (with L. Lavagno, G. E. Martin, L. K. Scheffer (eds)), "Electronic Design Automation for Integrated Circuits Handbook," CRC Press,2d ed., **2016**, (ISBN 978-1482254501).

B14. A. A. Kennings, I. L. Markov, "Circuit Placement," in Encyclopedia of Algorithms, Springer, 2nd ed., **2016**, pp. 301-306. (ISBN 978-1-4939-2865-1).

B13. (with S. Krishnaswamy and J. P. Hayes), "Design, Analysis and Test of Logic Circuits Under Uncertainty," 134 pages, Springer **2013**, (ISBN 978-9048196432).

B12. (with D. A. Papa), "Multi-Objective Optimization in Physical Synthesis of Integrated Circuits," 164 pages, Springer **2013**, (ISBN 978-1461413554).

B11. (with H. Katebi), "Large-scale Boolean Matching" in *Advanced Techniques in Logic Synthesis, Optimizations and Applications*, S. Khatri and K. Gulati, eds; Springer, **2011**.

B10. (with A. B. Kahng, J. Lienig and J. Hu), *VLSI Physical Design: from Graph Partitioning to Timing Closure*, 312 pages, Springer **2011** (ISBN 978-90-481-9590-9).

B9. (with G. F. Viamontes and J. P. Hayes), *Quantum Circuit Simulation*, Springer **2009** (ISBN: 978-9048130641).

B8. (with K.-H. Chang and V. Bertacco), *Functional Design Errors in Digital Circuits: Diagnosis, Correction and Layout Repair*, Springer **2008** (ISBN: 978-1-4020-9364-7).

B7. (with A. A. Kennings), "Circuit Placement," in *Encyclopedia of Algorithms*, M.-Y. Kao, ed.; pp. 143-146, Springer, **2008**.

B6. (with J. A. Roy), "Partitioning-driven Techniques for VLSI Placement," in *Handbook of Algorithms for VLSI Physical Design Automation*, C. Alpert, D. Mehta and S. Sapatnekar, eds; CRC Press, **2008**.

B5. (with J. A. Roy and D. A. Papa), "Capo: Congestion-aware Placement for Standard-cell and RTL Netlists with Incremental Capability," in *Modern Circuit Placement: Best Practices and Results*, G.-J. Nam and J. Cong, eds; Springer, **2007**.

B4. (with D. A. Papa), "Hypergraph Partitioning and Clustering," in *Approximation Algorithms and Metaheuristics*, T. Gonzalez, ed.; pages 61-1 through 61-19, CRC Press, **2007**.

B3. (with A. Ramani), "Automatically Exploiting Symmetries in Constraint Programming," in *Lecture Notes in Computer Science, vol. 3419*, B. Faltings, A. Petcu, F. Fages and F. Rossi, eds; pp. 98-112, Springer, **2005**.

[1] Two publications unrelated to main research interests (in *IEEE Computer* and *Proc. Kiev Math. Inst.*) not listed.

B2. (with D. B. Motter), "A Compressed Breadth-first Search For Satisfiability," in *Lecture Notes in Computer Science, vol. 2409*, D. M. Mount and Cl. Stein, eds; Springer, pp. 29-42, **2002**.

B1. (with A. E. Caldwell and A. B. Kahng), "Design and Implementation of the Fiduccia-Mattheyses Heuristic for VLSI Netlist Partitioning," in *Lecture Notes in Comp. Science, vol. 1619*, M. T. Goodrich, C. C. McGeoch, eds; pp. 177-193, Springer, **1999**.

Papers in journals and magazines

J91. (with M. M. Sabry et al), "The N3XT Approach to Energy-Efficient Abundant-Data Computing," *Proc. IEEE* 107(1), pp. 19-48, **2019**.

J90. (with T. N. Mudge, F. T. Chong, R. Sendag, J. J. Yi, and D. Chiou), "Impact of Future Technologies on Architecture," *IEEE Micro* 36(4): 48-56, **2016**.

J89. (with M. M. Sabry et al), "Energy-Efficient Abundant-Data Computing: The N3XT 1,000x," IEEE Computer 48(12), pp. 24-33, **2015**.

J88. (with J. Hu and M.-C. Kim), "Progress and Challenges in VLSI Placement Research," *Proc. IEEE* 103(11), pp. 1985-2003, **2015**.

J87. (with S. M. Plaza), "Solving the Third-Shift Problem in IC Piracy With Test-Aware Logic Locking," *IEEE Trans. on CAD of Integrated Circuits and Systems* 34(6), pp. 961-971, **2015**.

J86. (with H. J. Garcia), "Simulation of Quantum Circuits via Stabilizer Frames," *IEEE Trans. on Computers*, 64(8), pp. 2323-2336, **2015**.

J85. Igor L. Markov, "Limits to Fundamental Limits on Computation", *Nature* 512, pp. 147-154, August **2014**.

J84. (with H. J. Garcia and A. W. Cross), "On the Geometry of Stabilizer States," *Quantum Information and Computation*, vol. 14, no. 7-8, pp. 683-720, **2014**.

J83. (with R. R. Nadakuditi), "On Bottleneck Analysis in Stochastic Stream Processing," *ACM Trans. on Design Automation of Electronic Sys.* (TODAES), vol. 18, no. 3, article #34, July **2013**.

J82. (with M.-C. Kim and D.-J. Lee), "SimPL: An Algorithm for Placing VLSI Circuits," *Communications of the ACM*, vol. 56 no. 6, pp. 105-113, June **2013**.

J81. (with M. Saeedi), "Synthesis and Optimization of Reversible Circuits - A Survey," *ACM Computing Surveys* vol. 45, no. 2, February **2013**.

J80. I. L. Markov, "Know Your Limits: A Review of 'Limits to Parallel Computation: P-Completeness Theory'," *IEEE Design and Test*, vol. 30, no. 1, pp. 78-83, January **2013**.

J79. (with M. Saeedi), "Faster Quantum Number Factoring via Circuit Synthesis," *Physical Review A* 87, 012310, **2013**.

J78. I. L. Markov, "Too Much Automation?" *IEEE Design and Test of Computers*, vol. 29, no. 2, **2012**, pp. 96-98.

J77. (with M. Saeedi), "Constant-optimized Quantum Circuits for Modular Multiplication and Exponentiation," *Quantum Information & Computation*, vol.12, no.5&6, **2012**, pp.361-394.

J76. (with D.-J. Lee), "Obstacle-aware Clock-tree Shaping during Placement," *IEEE Trans. on Computer-Aided Design*, 31(2), pp. 50-60, **2012**.

J75. (with J. Knechtel and J. Lienig), "Assembling 2D Blocks into 3D Chips," *IEEE Trans. on Computer-Aided Design*, 31(2), pp. 205-216,**2012**.

J74. (with M.-C. Kim and D.-J. Lee), "SimPL: An Effective Placement Algorithm," *IEEE Trans. on Computer-Aided Design*, vol. 31(1), pp.50-60, **2012**.

J73. I. L. Markov, "Getting Your Bits in Order," *IEEE Design and Test of Computers*, vol. 28, no. 4, pp. 98-101, **2011**.

J72. (with D. A. Papa, C. Sze, N. Viswanathan, Z. Li, G.-J. Nam, C. J. Alpert), "Physical Synthesis with Clock-network Optimization for Large SoCs," IEEE Micro 31(4), pp. 51-62, **2011**.

J71. (with Y. Shi), "Constant-Degree Graph Expansions that Preserve Treewidth," *Algorithmica* vol. 59, no. 5, pp. 461-470, **2011**.

J70. I. L. Markov, "EDA: Synergy or sum of the parts?" *IEEE Design and Test of Computers*, vol. 28, no. 1, **2011**, pp. 78-79.

J69. (with D.-J. Lee),"Contango: Integrated Optimization for SoC Clock Networks," *VLSI Design*, vol. 2011, no. 407507, 12pp, **2011**.

J68. (with D. A. Papa, M. D. Moffitt, and C. J. Alpert), "Speeding up Physical Synthesis with Transactional Timing Analysis," to appear in *IEEE Design and Test of Computers*, **2010**.

J67. (with J. A. Roy and F. Koushanfar), "Ending Piracy of Integrated Circuits," *IEEE Computer*, October **2010**, pp. 30-38.

J66. (with S. Yamashita), "Fast Equivalence-checking of Quantum Circuits," *Quantum Information and Computation*, **2010**. vol. 9, no. 9& 10 (2010), pp. 721-734.

J65. "Chips in 3D" [review of Three-Dimensional Integrated Circuit Design: EDA, Design and Microarchitectures by Y. Xie, J. Cong, and S. Sapatnekar, eds.] *IEEE Design and Test of Computers*, vol. 27, no. 4, July-Aug **2010**, pp. 68-69.

J64. (with F. Koushanfar), "Designing Chips that Protect Themselves," *ACM DAC Knowledge Center*, March **2010**.

J63. (with K.-H. Chang, V. Bertacco and A. Mishchenko), "Logic Synthesis and Circuit Customization Using Extensive External Don't-Cares," to appear in *ACM Trans. on Design Autom. Elec. Sys.* (TODAES) 15 (3), May **2010**.

J62. "Master Numerical Tasks with Ease, [review of Advanced Excel for Scientific Data Analysis, 2nd ed. (de Levie, R.; 2008)]" *IEEE Design and Test of Computers*, vol. 27, no. 1, Jan-Feb **2010** pp. 93-95.

J61. "A Physical-design Picture Book" (review of Practical Problems in VLSI Physical Design Automation by S.K. Lim; 2008) *IEEE Design and Test of Computers*, vol. 26, no. 4, July-Aug **2009** pp. 100-101.

J60. (with V. V. Shende), "On the CNOT-cost of TOFFOLI gates," *Quantum Information and Computation*, vol. 9, no. 5-6, pp. 461-486, May **2009**.

J59. (with J. A. Roy, A. N. Ng, R. Aggarwal, and V. Ramachandran), "Solving Modern Mixed-size Placement Instances," *Integration*, vol. 42 no. 2, pp. 262-275, **2009**.

J58. (with K-H. Chang, D. A. Papa and V. Bertacco), "Invers: An Incremental Verification System with Circuit Similarity Metrics and Error Visualization," *IEEE Design and Test of Computers*, vol. 26, no. 2, pp. 34-43, March **2009**.

J57. (with F. A. Aloul, A. Ramani and K. A. Sakallah), "Dynamic Symmetry-Breaking for Boolean Satisfiability," *Annals of Mathematics and Artificial Intelligence*, vol. 51, no. 1, **2009**, pp. 59-73.

J56. (with S. Krishnaswamy, S. Plaza and J. P. Hayes), "Signature-based SER Analysis and Design of Logic Circuits," *IEEE Trans. on Computer-Aided Design*, vol.28, no.1, pp. 74-86, January **2009**.

J55. (with D. A. Papa, T. Luo, M. D. Moffitt, C. N. Sze, Z. Li, G.-J. Nam, and C. J. Alpert), "RUMBLE: An Incremental, Timing-driven, Physical-synthesis Optimization Algorithm," *IEEE Trans. on Computer-Aided Design*, 27(12), pp. 2156-2168, December **2008**.

J54. (with S. M. Plaza and V. M. Bertacco), "Optimizing Non-Monotonic Interconnect using Functional Simulation and Logic Restructuring," *IEEE Trans. on Computer-Aided Design*, 27(12), pp. 2107-2119, December **2008**.

J53. (with M. D. Moffitt, J. A. Roy and M. E. Pollack), "Constraint-driven Floorplan Repair," *ACM Trans. on Design Automation of Electronic Systems* 13(4), October **2008**.

J52. (with J. A. Roy and D. A. Papa), "Fine Control of Local Whitespace in Placement," *VLSI Design*, vol. **2008**, article 517919, 10 pp. DOI:10.1155/2008/517919.

J51. (with K-H. Chang and V. Bertacco), "Automating Post-Silicon Debugging and Repair," *IEEE Computer*, vol. 41, no. 7, pp. 47-54, July **2008**.

J50. (with Y.-Y. Shi), "Simulating Quantum Computation by Contracting Tensor Networks," *SIAM Journal on Computing*, vol. 38, no. 3, pp. 963-981, June **2008**.

J49. (with J. A. Roy) "High-performance Routing at the Nanometer Scale," *IEEE Trans. on Computer-Aided Design*, vol. 27, no. 6, pp. 1066-1077, June **2008**.

J48. (with K-H. Chang and V. Bertacco), "SafeResynth: A New Technique for Physical Synthesis", *Integration: the VLSI Journal*, vol. 41, pp. 544-556. **2008**.

J47. (with K.-H. Chang and V. Bertacco), "Fixing Design Errors with Counterexamples and Resynthesis," *IEEE Trans. on Computer-Aided Design*, ol. 27, no. 1, pp. 184-188, **2008**.

J46. (with K. Patel and J. Hayes), "Optimal Synthesis of Linear Reversible Circuits," *Quantum Information and Computation*, vol. 8, no. 3-4, pp. 282-294, **2008**.

J45. (with S. Krishnaswamy, G. F. Viamontes, and J. P. Hayes), "Probabilistic Transfer Matrices in Symbolic Reliability Analysis of Logic Circuits," *ACM Trans. on Design Automation of Electronic Systems*, vol.13, no.1, #8 **2008**.

J44. (with J. A. Roy), "ECO-system: Embracing the Change in Placement", *IEEE Trans. on Computer-Aided Design*, vol. 26, no. 12, pp. 2173-2185, December **2007**.

J43. (F. A. Aloul, A. Ramani, and K. A. Sakallah), "Symmetry-Breaking for Pseudo-Boolean Formulas", *ACM Journal on Experimental Algorithms* 12, #1.3 **2007**.

J42. (with F. A. Aloul and K. A. Sakallah), "Solution and Optimization of Systems of Pseudo-Boolean Constraints," *IEEE Trans. on Computers*, vol. 56, no. 11, pp. 1415-1424, October **2007**.

J41. (with K.-H. Chang and V. Bertacco), "Post-placement Rewiring by Exhaustive Search for Functional Symmetries," *ACM Transactions on Design Automation of Electronic Systems*, 12(3), #32, August **2007**.

J40. (with S. Krishnaswamy and J. P. Hayes), "Tracking Uncertainty with Probabilistic Logic Circuit Testing," *IEEE Design and Test of Computers*, vol. 24, no. 4, pp.312-321, July-August **2007**.

J39. (with L. K. Scheffer, D. Stroobandt), "Guest Editors' Introduction: Special issue on System-Level Interconnect," *Integration: the VLSI Journal*, 40/4, p. 381, **2007**.

J38. (with J. A. Roy), "Seeing the Forest and the Trees: Steiner Wirelength Optimization in Placement," *IEEE Trans. on Computer-Aided Design*, vol. 26 no. 4, pp. 632-644, April **2007**.

J37. (with K.-H. Chang and V. Bertacco), "Simulation-based Bug Trace Minimization with BMC-based Refinement", *IEEE Trans. on Computer-Aided Design*, vol. 26, no. 1, pp. 152-165, January **2007**.

J36. (with A. K. Prasad, V. V. Shende, K. N. Patel, J. P. Hayes), "Data Structures and Algorithms for Simplifying Reversible Circuits," *ACM Journal of Emerging Technologies in Computing Systems*, vol. 2, no. 4, pp. 277-293, October **2006**.

J35. (with A. Ramani, F. A. Aloul and K. A. Sakallah), "Breaking Instance-Independent Symmetries in Exact Graph Coloring", *Journal of Artificial Intelligence Research*, vol. 26, pp. 191-224, **2006**.

J34. (with S. N. Adya and P. G. Villarrubia), "On Whitespace and Stability in Physical Synthesis", *Integration: the VLSI Journal*, vol. 39/4, pp. 340-362, **2006**.

J33. (with J. A. Roy, S. N. Adya and D. A. Papa), "Min-cut Floorplacement", *IEEE Trans. on CAD*, vol. 25, no. 7, July **2006**.

J32. (with V. V. Shende and S. S. Bullock), "Synthesis of Quantum Logic Circuits", *IEEE Trans. on CAD*, vol. 25, no. 6, June **2006**, pp. 1000-1010.

J31. (with F. A. Aloul and K. A. Sakallah) "Efficient Symmetry Breaking for Boolean Satisfiability", *IEEE Trans. on Computers*, vol. 55, no. 5, pp. 541-558, **2006**.

J30. (with K. M. Svore, A. W. Cross, I. L. Chuang and A. V. Aho), "A Layered Software Architecture for Quantum Computing Design Tools", *IEEE Computer*, vol. 39, no. 1, pp. 74-83, January **2006**.

J29. (with G. F. Viamontes and J. P. Hayes), "Is Quantum Search Practical?", *IEEE/AIP Computing in Science and Engineering*, May/June **2005**, pp. 62-70.

J28. (with D. B. Motter and J. A. Roy), "Resolution Cannot Polynomially Simulate Compressed-BFS," *Annals of Mathematics and Artificial Intelligence*, vol. 44, no.1-2, pp. 121-156, May **2005**.

J27. (with G. F. Viamontes and J. P. Hayes), "Graph-based Simulation of Quantum Computation in the Density Matrix Representation", *Quantum Information and Computation*, vol.5, no.2 pp. 113-130, February **2005**.

J26. (with S. N. Adya), "Combinatorial Techniques for Mixed-size Placement," *ACM Trans. on Design Automation of Electronic Systems*, vol. 10, no. 5, January **2005**.

J25. (with V. V. Shende), "Quantum Circuits for Incompletely Specified Two-Qubit Operators", *Quantum Information and Computation*, vol.5, no.1, pp. 49-57, January **2005**.

J24. (with F. A. Aloul and K. A. Sakallah), "MINCE: A Static Global Variable-Ordering for SAT Search and BDD Manipulation", *Journal of Universal Computer Science*, vol. 10, no. 12, pp. 1559-1562, December **2004**.

J23. (with K. N. Patel), "Error Correction and Crosstalk Avoidance in DSM Busses," *IEEE Trans. on VLSI* vol. 12, no.10, pp. 1076-1081, October **2004**.

J22. (with K. N. Patel and J. P. Hayes), "Fault Testing for Reversible Circuits," *IEEE Trans. on CAD*, 23(8), pp. 1220-1230, August **2004**.

J21. (with V. V. Shende and S. S. Bullock), "Recognizing Small-circuit Structure in Two-qubit Operators," *APS Physical Review A* 70, 012310-012314, **2004**. Reprinted in *APS/AIP Virtual Journal of Quantum Information*, August **2004**.

J20. (with V. V. Shende and S. S. Bullock), "Minimal Universal Two-qubit Controlled-NOT-based Circuits," *APS Physical Review A* 69, 062321-62329, **2004**. Reprinted in *APS/AIP Virtual Journal of Quantum Information*, July **2004**.

J19. (with S. N. Adya et al.) "Benchmarking for Large-scale Placement and Beyond," *IEEE Trans. on CAD*, 23(4), pp. 472-488, April **2004**.

J18. (with S. S. Bullock) "Asymptotically Optimal Circuits for Arbitrary n-qubit Diagonal Computations," *Quantum Information and Computation*, vol. 4, no. 1, pp. 27-47, January **2004**.

J17. (with S. N. Adya) "Fixed-outline Floorplanning : Enabling Hierarchical Design," *IEEE Trans. on VLSI*, vol. 11(6), pp. 1120-1135, December **2003**.

J16. (with A. E. Caldwell and A. B. Kahng) "Hierarchical Whitespace Allocation in Top-down Placement," *IEEE Trans. on CAD*, vol. 22(11), pp. 716-724, November **2003**.

J15. (with G. F. Viamontes and J. P. Hayes), "Improving Gate-Level Simulation of Quantum Circuits," *Quantum Information Processing*, vol. 2(5), pp.347-380, October **2003**.

J14. (with F. A. Aloul, A. Ramani and K. A. Sakallah) "Solving Difficult Instances of Boolean Satisfiability in the Presence of Symmetry," *IEEE Trans. on CAD*, vol. 22(9), pp. 1117-1137, September **2003**.

J13. (with S. S. Bullock) "An Arbitrary Two-qubit Computation in 23 Gates or Less," *APS Physical Review A*, vol. 68, no. 1, 012318-012325, July **2003**. Reprinted in *APS/AIP Virtual Journal of Quantum Information*, August **2003**.

J12. (with V. V. Shende, A. K. Prasad and J. P. Hayes) "Synthesis of Reversible Logic Circuits," *IEEE Trans. on CAD*, vol. 22(6), p. 710-722, June **2003**. **IEEE CAS Donald O. Pederson "paper of the year" award**.

J11. (with Y. Cao et al.) "Improved A Priori Interconnect Predictions and Technology Extrapolation in the GTX System", *IEEE Trans. on VLSI*, vol. 11(1), pp. 3-14. **2003**.

J10. (with A. E. Caldwell and A. B. Kahng), "Toward CAD-IP Reuse: The MARCO GSRC Bookshelf of Fundamental CAD Algorithms", *IEEE Design and Test of Computers*, pp. 72-81, May **2002**.

J9. (with A. A. Kennings), "Smoothening Max-terms and Analytical Minimization of Half-Perimeter Wirelength", *VLSI Design*, vol. 14(3), pp. 229-237, **2002**.

J8. (with A. B. Kahng et al.), "Constraint-Based Watermarking Techniques for Design Intellectual Property Protection", *IEEE Trans. on CAD*, vol. 20(10), pp. 1236-1252, October **2001**.

J7. (with R. Baldick, A. B. Kahng and A. A. Kennings), "Efficient Optimization by Modifying the Objective Function", *IEEE Trans. on Circuits and Systems*, vol. 48(8), pp. 947-957, **2001**,

J6. (with A. E. Caldwell and A. B. Kahng), "Iterative Partitioning With Varying Node Weights", *VLSI Design*, vol.11, no.3, pp. 249-58, **2000**.

J5. (with C. J. Alpert, A. E. Caldwell and A. B. Kahng), "Hypergraph Partitioning With Fixed Vertices", *IEEE Trans. on CAD*, vol. 19, no. 2, (2000), pp. 267-272, February-March **2000**.

J4. (with C. J. Alpert et al.), "Analytical Engines Are Unnecessary in Top-Down Partitioning-Based Placement", *VLSI Design*, 10(1), pp. 99-116, January **1999**.

J3. (with A. E. Caldwell and A. B. Kahng), "Design and Implementation of Move-based Heuristics for VLSI Hypergraph Partitioning", *ACM Journal of Experimental Algorithms*, vol. 5, **2000** (online publication).

J2. (with A. E. Caldwell, A. B. Kahng, S. Mantik and A. Zelikovsky), "On Wirelength Estimations for Row-Based Placement", *IEEE Trans. on CAD* 18(9), pp. 1265-1278, **1999**.

J1. (with C. J. Alpert, T. Chan, A. B. Kahng and P. Mulet), "Faster Minimization of Linear Wirelength for Global Placement" *IEEE Trans. on CAD* 17(1), pp. 3-13, **1998**.

Refereed papers in conference proceedings

C134. (with S. Hillmich, R. Wille), "Just Like the Real Thing: Fast Weak Simulation of Quantum Computation," *DAC* 2020.

C133. (with A. Fatima, S. V. Isakov, and S. Boixo), "Massively Parallel Approximate Simulation of Quantum Circuits," *DAC* 2020.

C132. (with A. Zulehner, S. Hillmich, and R. Wille), "Approximation of Quantum States Using Decision Diagrams," *ASP-DAC* 2020, pp. 121-126.

C131. (with S. Osmolovskyi, J. Knechtel, and J. Lienig), "Optimal die placement for interposer-based 3D ICs," *ASP-DAC* **2018**, pp. 513-520.

C130. (with R.I. Bahar, A.K. Jones, S. Katkoori, P.H. Madden and D.Marculescu) "Workshops on Extreme Scale Design Automation (ESDA) Challenges and Opportunities for 2025 and Beyond," *Computing Community Consortium* (CCC), **2014**.

C129. (with M. Wang and A. Yates) "SuperPUF: Integrating Heterogeneous Physically Unclonable Functions," *ICCAD* pp. 454-461, **2014**.

C128. (with S.M. Plaza) "Protecting Integrated Circuits from Piracy with Test-aware Logic Locking," *ICCAD*, pp. 262-269, **2014**.

C127. (with P. Codenotti, H. Katebi, K. A. Sakallah) "Conflict Analysis and Branching Heuristics in the Search for Graph Automorphisms," ICTAI, pp. 907-914, **2013**.

C126. (with H. Katebi and K. Sakallah), "Generalized Boolean Symmetries Through Nested Partition Refinement," pp. 763-770, in Proc. *Int'l. Conf. Comp.-Aided Design* (ICCAD), San Jose, CA, **2013**.

C125. (with A. B. Kahng, S. Kang, H. Lee, P. Thapar), "High-Performance Gate Sizing with a Signoff Timer," pp. 450-457, in Proc. *Int'l. Conf. Comp.-Aided Design* (ICCAD), San Jose, CA, **2013**.

C124. (with H. J. Garcia), "Quipu: High-performance Simulation of Quantum Circuits using Stabilizer Frames," in Proc. *Int'l Conf. Computer Design* (ICCD), pp. 404-410, Asheville, NC, **2013**.

C123. (with. I. R. Bahar, A. K. Jones, S. Katkoori, P. H. Madden, and D. Marculescu) "Scaling the Impact of EDA Education: Preliminary Findings from the CCC Workshop Series on Extreme Scale Design Automation," in Proc. *Conf. on Microelectronic Systems Education* (MSE), **2013**.

C122. (with J. Hu and M.-C. Kim),"Taming the Complexity of Coordinated Place and Route," in Proc. *Design Automation Conference* (DAC), pp. 150-155, **2013**.

C121. (with Y. Yao, M.-B. Kim, J. Li, F. Koushanfar), "ClockPUF: Physical Unclonable Functions based on Clock Networks," in Proc. *Design Automation and Test in Europe* (DATE), pp. 422-427, **2013**.

C120. (with J. Hu and M.-C. Kim), "Progress and Challenges in VLSI Placement Research," in *Proc. Int'l. Conf. Comp.-Aided Design* (ICCAD), **2012**.

C119. (with J. Knechtel, J. Lienig, and M. Thiele) "Multiobjective Optimization of Deadspace, a Critical Resource for 3D-IC Integration," in *Proc. Int'l. Conf. Comp.-Aided Design* (ICCAD), **2012**.

C118. (with J. Hu, A. B. Kahng, S. Kang, and M.-C. Kim), "Sensitivity-guided Metaheuristics for Accurate Discrete Gate Sizing," in *Proc. Int'l. Conf. Comp.-Aided Design* (ICCAD), **2012**.

C117. (with H. Katebi and K. A. Sakallah), "Graph Symmetry Detection and Canonical Labeling: Differences and Synergies," *the Turing Centenary Conference*, EPIC vol.10, pp. 181-195, Manchester, UK, **2012** (**best paper award**).

C116. (with M.-C. Kim), "ComPLx: A Competitive Primal-dual Lagrange Optimization for Global Placement," in Proc. *Design Autom. Conf.* (DAC), pp. 747-755, San Francisco, CA, **2012**.

C115. (with H. Katebi and K. A. Sakallah), "Conflict Anticipation in the Search for Graph Automorphisms," *Int'l Conf. on Logic for Programming, Artificial Intelligence and Reasoning* (LPAR), LNCS vol. 7180, pp. 243-257, Mérida, Venezuela, **2012**.

C114. (with T. Güneysu and A. Weimerskirch), "Securely Sealing Multi-FPGA Systems," in Proc. *Int'l Symp. on Applied Reconfigurable Computing* (ARC), LNCS vol. 7199, pp. 276-289, **2012**.

C113. (with K.-H. Chang and H.-Z. Chou), "RTL Analysis and Modifications for Improving At-speed Test," (**BPA nominee**), in Proc. *Design Autom. and Test in Europe Conf.* (DATE), pp. 400-405, **2012**.

C112. M.-C. Kim, N. Viswanathan, C. J. Alpert, I. L. Markov and S. Ramji, "MAPLE: Multilevel Adaptive PLacEment for Mixed-Size Designs," (**BPA nominee**), pp. 193-200, in Proc. *Int'l Symp. Physical Design* (ISPD), **2012**.

C111. (with D.-J. Lee), "Algorithmic Tuning of Clock Trees and Derived Non-Tree Structures," *Int'l. Conf. Comp.-Aided Design* (ICCAD), pp. 279-282, November **2011**.

C110. (with M.-C. Kim, J. Hu, D.-J. Lee), "A SimPLR method for Routability-driven Placement" (**BPA nominee**), *Int'l. Conf. Comp.-Aided Design* (ICCAD), pp. 67-73, November **2011**.

C109. (with D.-J. Lee), "Multilevel Tree Fusion for Robust Clock Networks," *Int'l. Conf. Comp.-Aided Design* (ICCAD), pp. 632-639, November **2011**.

C108. (with D.-J. Lee), "Obstacle-aware Clock-tree Shaping during Placement" (**BPA nominee**), *Int'l. Symp. on Physical Design* (ISPD), pp. 123-130, March **2011**.

C107. (with J. Knechtel and J. Lienig), "Assembling 2D Blocks into 3D Chips," *Int'l. Symp. on Physical Design* (ISPD), pp. 81-88, March **2011**.

C106. (with M.-C. Kim and D.-J. Lee), "'SimPL: An Effective Placement Algorithm," (**Best Paper Award**) in *Proc. Int'l. Conf. on Computer-Aided Design* (ICCAD), pp. 649-656, November **2010**.

C105. (with D.-J. Lee and M.-C. Kim), "Low-Power Clock Trees for CPUs," in *Proc. Int'l. Conf. on Computer-Aided Design* (ICCAD), November **2010**.

C104. (with D. A. Papa and S. Krishnaswamy) "SPIRE: A Retiming-based Global Physical Synthesis Transformation System," in *Proc. Int'l. Conf. on Computer-Aided Design* (ICCAD), pp. 373-380, November **2010**.

C103. (with H. Katebi and K. A. Sakallah) "Symmetry and Satisfiability: An Update," in Proc. *Satisfiability Symposium* (SAT), pp. 113-127, Edinburgh, Scotland, July **2010**.

C102. (with S. Yamashita) "Fast Equivalence-checking for Quantum Circuits," in Proc. *Int'l Symp. on Nanoscale Architectures* (NanoArch), pp. 23-28, Anaheim, CA, June **2010**.

C101. (with R. R. Nadakuditi) "On the Costs and Benefits of Stochasticity in Stream Processing," in Proc. *Design Autom. Conf.* (DAC), pp. 320-325, Anaheim, CA, June **2010**.

C100. (with J. Hu and J. A. Roy), "Completing High-quality Routes," in Proc. *Int'l. Symp. on Physical Design* (ISPD), pp. 35-41, San Francisco, CA, March **2010**.

C99. (with D.-J. Lee),"Contango: Integrated Optimizations for SoC Clock Networks," in Proc. *Design Autom. and Test in Europe* Conf. (DATE), pp. 1468-1473, Dresden, March **2010**.

C98. (with H. Garcia), "Spinto: a High-performance Solver for Energy Minimization in Ising Spin-glasses", in Proc. *Design Autom. and Test in Europe* Conf. (DATE), pp. 160-165, Dresden, March **2010**.

C97. (with H. Katebi), "Large-scale Boolean Matching," in Proc. *Design Autom. and Test in Europe* Conf. (DATE), pp. 771-776, Dresden, March **2010**.

C96. (with J. A. Roy, N. Viswanathan, G.-J. Nam, C. J. Alpert), "CRISP: Congestion Reduction by Iterated Spreading during Placement," in *Proc. Int'l. Conf. on Computer-Aided Design* (ICCAD), pp. 357-362, November **2009**.

C95. (with S. Krishnaswamy and J.P. Hayes), "Improving Testability and Soft-Error Resilience through Retiming," in Proc. *Design Autom. Conf.* (DAC), pp. 924-929, July **2009**.

C94. (with K.-H. Chang and V. Bertacco), "Customizing IP Cores for System-on-Chip Designs Using Extensive External Don't-Cares," in Proc. *Design Autom. and Test in Europe* (DATE), pp 582-585, April **2009**.

C93. (with J.-S. Seo, D. Blaauw, and D. Sylvester), "On the Decreasing Significance of Large Standard Cells in Technology Mapping," in Proc. *Int'l. Conf. on Computer-Aided Design*, pp. 116-121, November **2008**.

C92. (with J. A. Roy and I. L. Markov), "Circuit CAD Tools as a Security Threat," in Proc. *Hardware-Oriented Security and Trust Workshop* (HOST), pp. 68-69, Anaheim, CA **2008**.

C91. (with S. Krishnaswamy and J. P. Hayes), "On the Role of Timing Masking in Reliable Logic Circuit Design," *Proc. Design Autom. Conf.* (DAC), pp. 846-861, Anaheim, CA, **2008**.

C90. (with P. T. Darga and K. A. Sakallah), "Faster Symmetry Discovery using Sparsity of Symmetries," *Proc. Design Autom. Conf.* (DAC), pp. 149-154, Anaheim, CA, **2008**.

C89. (with J. A. Roy and F. Koushanfar), "Protecting Bus-based Hardware IP by Secret Sharing," *Proc. Design Autom. Conf.* (DAC), pp. 924-929, Anaheim, CA, **2008**.

C88. (with J. P. Hayes), "Why Nanoscale Physics Favors Quantum Information," *Proc. VLSI Test Symposium* (VTS), p. 107, San Deigo, CA, **2008**.

C87. (with J. Hu and J. A. Roy), "Sidewinder: A Scalable Wire Router Based on ILP", *Proc. Int'l Workshop on System-Level Interconnect Prediction* (SLIP), pp. 73-80. Newcastle, England, **2008**.

C86. (with K.-H. Chang and V. Bertacco), "Reap What You Sow: Spare Cells for Post.-Silicon Metal Fix," *Proc. Int'l Symposium on Physical Design* (ISPD), pp. 103-110, Portland, Oregon, **2008**.

C85. (with S. M. Plaza and V. Bertacco), "Optimizing Non-Monotonic Interconnect using Functional Simulation and Logic Restructuring," *Proc. Int'l Symposium on Physical Design* (ISPD), pp. 95-102, Portland, Oregon, **2008** (**Best Paper Award**).

C84. (with M. D. Moffitt and J. A. Roy) "The Coming of Age of (Academic) Global Routing", *Proc. Int'l Symposium on Physical Design* (ISPD), pp. 148-155, Portland, Oregon, **2008**.

C83. (with D. A. Papa, T. Luo, M. D. Moffitt, C. N. Sze, Z. Li, G.-J. Nam, and C. J. Alpert) "RUMBLE: An Incremental, Timing-driven, Physical-synthesis Optimization Algorithm," *Proc. Int'l Symposium on Physical Design* (ISPD), pp. 2-9, Portland, Oregon, **2008**.

C82. (with J. A. Roy and F. Koushanfar), "EPIC: Ending Piracy of Integrated Circuits," *Proc. Design Autom. and Test in Europe* (DATE), pp. 664-669, Munich, Germany, **2008**.

C81. (with S. M. Plaza and V. Bertacco), "Random Stimulus Generation using Entropy and XOR constraints," *Proc. Design Autom. and Test in Europe* (DATE), pp. 664-669, Munich, Germany, **2008**.

C80. (with K.-H. Chang, I. Wagner and V. Bertacco), "Automatic Error Diagnosis and Correction for RTL Designs," *Proc. High-Level Design Validation and Test* workshop (HLDVT), pp. 65-72, Irvine, CA, **2007**.

C79. (with S. Krishnaswamy, S. M. Plaza and J. P. Hayes), "Enhancing Design Robustness with Reliability-aware Resynthesis and Logic Simulation," *Proc. Int'l Conf. on Computer-Aided Design* (ICCAD), pp. 149-154, San Jose, CA, **2007**.

C78. (with K-H. Chang and V. Bertacco), "Automating Post-Silicon Debugging and Repair," *Proc. Int'l Conf. on Computer-Aided Design* (ICCAD), pp. 91-98, San Jose, CA, **2007**.

C77. (with J. A. Roy), 'High-performance Routing at the Nanometer Scale," *Proc. Int'l Conf. on Computer-Aided Design* (ICCAD), pp. 496-502, San Jose, CA, **2007**.

C76. (with G. F. Viamontes and J. P. Hayes), "Equivalence Checking of Quantum Circuits and States," *Proc. Int'l Conf. on Computer-Aided Design* (ICCAD), pp. 69-74, San Jose, CA, **2007**.

C75. (with K.-H. Chang, D. A. Papa and V. Bertacco), "InVerS: An Incremental Verification System with Circuit Similarity Metrics and Error Visualization", *Proc. Int'l Symp. Quality Electronic Design* (ISQED), pp. 487-492, San Jose, CA **2007**.

C74. (with K.-H. Chang and V. Bertacco), "Safe Delay Optimization for Physical Synthesis", *Proc. Asia and South Pacific Design Automation Conf.* (ASPDAC), pp. 944-949, Yokohama, Japan, January **2007**.

C73. (with S. Plaza, K.-H. Chang and V. Bertacco), "Node Mergers in the Presence of Don't Cares", *Proc. Asia and South Pacific Design Automation Conf.* (ASPDAC), pp. 414-419, Yokohama, Japan, January **2007**.

C72. (with K.-H. Chang and V. Bertacco), "Fixing Design Errors with Counterexamples and Resynthesis", *Proc. Asia and South Pacific Design Automation Conf.* (ASPDAC), pp. 628-633, Yokohama, Japan, January **2007**.

C71. (with J. A. Roy), "ECO-System: Embracing the Change in Placement", *Proc. Asia and South Pacific Design Automation Conf.* (ASPDAC), pp. 147-152, Yokohama, Japan, January **2007**.

C70. (single-author), "Almost-symmetries of Graphs", *Proc. Int'l Symmetry Conf. (ISC)*, pp. 60-70, Edinburgh, Scotland, January **2007**.

C69. (with M. D. Moffitt, A. N. Ng, and M. E. Pollack), "Constraint-driven Floorplan Repair", *Proc. Design Automation Conf.* (DAC), pp. 1103-1108, San Francisco, CA, July **2006**.

C68. (with R. Das and J. P. Hayes), "On-Chip Test Generation Using Linear Subspaces", *Proc. European Test Symposium* (ETS), pp. 111-117, Southampton, UK, May **2006**.

C67. (with J. A. Roy, D. A. Papa, A. N. Ng, I. L Markov), "Satisfying Whitespace Requirements in Top-down Placement", *Proc. Int'l Symp. on Physical Design* (ISPD), pp. 170-177, San Jose, CA, April **2006 (invited)**.

C66. (with J. A. Roy and J. F. Lu), "Seeing the Forest and the Trees: Steiner Wirelength Optimization in Placement", *Proc. Int'l Symp. on Physical Design* (ISPD), pp. 78-85, San Jose, CA, April **2006**.

C65. (with A. N. Ng, R. Aggarwal and V. Ramachandran), "Solving Hard Instances of Floorplacement",(**BPA nominee**), *Proc. Int'l Symp. on Physical Design* (ISPD), pp. 170-177, San Jose, CA, April **2006**.

C64. (with D. A. Papa and P. Chong), "Utility of OpenAccess in Academic Research", *Proc. Asia and South Pacific Design Conf.* (ASPDAC), pp. 440-441, Yokohama, Japan **2006** (**invited**).

C63. (with K.-H. Chang and V. Bertacco), "Post-Placement Rewiring and Rebuffering by Exhaustive Search For Functional Symmetries", *Proc. Int'l Conf. Computer-Aided Design* (ICCAD), pp. 56-63, San Jose, CA, November **2005**.

C62. (with K.-H. Chang and V. Bertacco), "Simulation-based Bug Trace Minimization with BMC-based Refinement", *Proc. Int'l Conf. Computer-Aided Design* (ICCAD), pp. 1045-1051, San Jose, CA, November **2005**.

C61. (with S. Krishnaswamy and J. P. Hayes), "Testing Logic Circuits for Transient Faults", in *Proc. IEEE Eur. Test Symp.* (ETS), pp. 102-107, Tallinn, Estonia, May **2005**.

C60. (with J. A. Roy, D. A. Papa, S. N. Adya, H. H. Chan, J. F. Lu, A. N. Ng), "Capo: Robust and Scalable Open-Source Min-cut Floorplacer", in *Proc. Intl. Symposium on Physical Design* (ISPD), pp. 224-227, San Francisco, April **2005**.

C59. (with Zh. Xiu, D. A. Papa, P. Chong, A. Kuehlmann, R. A. Rutenbar), "Early Research Experience with OpenAccess Gear: An Open Source Development Environment for Physical Design," in *Proc. Intl. Symposium on Physical Design* (ISPD), pp. 94-100, San Francisco, April **2005** (**invited**).

C58. (with H. H. Chan and S. N. Adya), "Are Floorplan Representations Important in Digital Design?", in *Proc. Intl. Symposium on Physical Design* (ISPD), pp. 129-136, San Francisco, April **2005**.

C57. (with A. N. Ng), "Toward High Quality Tools and Tool Flows Through High-Performance Computing", *Proc. Intl. Symposium on Quality Electronic Design* (ISQED), pp. 22-27, San Jose, March **2005**.

C56. (with S. Krishnaswamy and J. P. Hayes), "Accurate Reliablity Evaluation and Enhancement via Probabilistic Transfer Matrices", *Proc. Design Automation and Test in Europe* (DATE), pp. 282 - 287, Munich, Germany, March **2005** (**best paper award**).

C55. (with D. Maslov), "Uniformly-switching Logic for Cryptographic Applications", in *Proc. Design Automation and Test in Europe* (DATE), Munich, Germany, pp. 432-433, March **2005**.

C54. (with F. A. Aloul, A. Ramani, and K. A. Sakallah), "Dynamic Symmetry-Breaking for Improved Boolean Optimization", *Proc. Asia and South Pacific Design Autom. Conf.* (ASPDAC), pp. 445-450, Shanghai, China, January **2005**.

C53. (with V. S. Shende and S. S. Bullock), "'Synthesis of Quantum Logic Circuits", *Proc. Asia and South Pacific Design Autom. Conf.* (ASPDAC), pp. 272-275, Shanghai, China, January **2005**.

C52. (with S. N. Adya, D. A. Papa, J. A. Roy and S. Chaturvedi), "Unification of Partitioning, Placement and Floorplanning", *Intl. Conf. Computer-Aided Design* (ICCAD), San Jose, CA, November **2004**, pp. 550-557.

C51. (with P. T. Darga, M. H. Liffiton and K. A. Sakallah), "Exploiting Structure in Symmetry Detection for CNF," *Proc. Design Autom. Conf.* (DAC), San Diego, California, June **2004**, pp. 518-523.

C50. (with Y. Oh, M. Mneimneh, Z. S. Andraus, and K. A. Sakallah), "AMUSE: A Minimally Unsatisfiable Subformula Extractor," *Proc. Design Autom. Conf.* (DAC), (**BPA nominee**), San Diego, California, June **2004**, pp. 530-534.

C49. (A. B. Kahng and S. Reda), *Proc. Great Lakes Symp. on VLSI* (GLSVLSI), Boston, Massachusetts, April **2004**, pp. 214-219.

C48. (with H. H. Chan), "Practical Slicing and Nonslicing Block-Packing without Simulated Annealing," *Proc. Great Lakes Symp. on VLSI* (GLSVLSI), Boston, Massachusetts, April **2004**, pp. 282-287.

C47. (with D. A. Papa and S. N. Adya), "Constructive Benchmarking for Placement," *Proc. Great Lakes Symp. on VLSI* (GLSVLSI), Boston, Massachusetts, April **2004**, pp. 113-118.

C46. (with V. V. Shende and S. S. Bullock), "Finding Small Two-Qubit Circuits," *Proc. SPIE vol. 5436 (Conf. on Quantum Information and Computation)*, pp. 348-359, Orlando, Florida, April **2004**.

C45. (with G. F. Viamontes and J. P. Hayes), "Graph-based Simulation of Quantum Computation in the State-vector and Density-matrix Representation," *Proc. SPIE vol. 5436 (Conf. on Quantum Information and Computation)*, pp. 285-296, Orlando, Florida, April **2004**.

C44. (with A. Ramani, F. A. Aloul and K. A. Sakallah), "Breaking Instance-Independent Symmetries in Exact Graph Coloring," *Proc. Design Autom. and Test in Europe* (DATE), Paris, France, February **2004**, pp. 324-329.

C43. (with V. V. Shende and S. S. Bullock), "Smaller Two-Qubit Circuits for Quantum Communication and Computation," *Proc. Design Autom. and Test in Europe* (DATE), Paris, France, February **2004**, pp. 980-985.

C42. (with S. Reda and A. B. Kahng), "Boosting: Min-cut Placement with Improved Signal Delay," *Proc. Design Autom. and Test in Europe* (DATE), Paris, France, February **2004**, pp. 1098-1103.

C41. (with G. F. Viamontes and J. P. Hayes), "High-performance QuIDD-based Simulation of Quantum Circuits," *Proc. Design Autom. and Test in Europe* (DATE), Paris, France, February **2004**, pp. 1354-1359.

C40. (with F. A. Aloul, A. Ramani and K. A. Sakallah), "Symmetry-Breaking for Pseudo-Boolean Formulas," *Proc. Asia and South Pacific Design Autom. Conf.* (ASPDAC), Yokohama, Japan, January **2004**, pp. 884-887.

C39. (with S. N. Adya and P. G. Villarrubia), "On Whitespace and Stability in Physical Synthesis", *Proc. Intl. Conf. on Computer-Aided Design (ICCAD)*, San Jose, November **2003**, pp. 311-318.

C38. (with F. A. Aloul and K. A. Sakallah), "Efficient Symmetry Breaking for Boolean Satisfiability," *Proc. Intl. Joint Conf. on Artificial Intelligence (IJCAI)*, Acapulco, Mexico, August **2003**, pp. 271-282.

C37. (with A. Ramani), "Combining Two Local Search Approaches to Hypergraph Partitioning," *Proc. Intl. Joint Conf. on Artificial Intelligence (IJCAI)*, Acapulco, Mexico, August **2003**, pp. 1546-1548.

C36. (with S. Bullock), "An Arbitrary Two-qubit Computation In 23 Elementary Gates Or Less," *Proc. ACM/IEEE Design Automation Conf.*, Anaheim, CA, June **2003** (**BPA nominee**), pp. 324-329.

C35. (with F. A. Aloul and K. A. Sakallah), "Shatter: Efficient Symmetry-Breaking for Boolean Satisfiability", *Proc. ACM/IEEE Design Automation Conf.*, Anaheim, CA, June **2003**, pp. 836-839.

C34. (with K. N. Patel and J. P. Hayes), "Fault Testing for Reversible Circuits," *Proc. IEEE VLSI Test Symposium (VTS)*, Napa, CA, April **2003**, pp. 410-416.

C33. (with F. A. Aloul and K. A. Sakallah), "FORCE: A Fast and Easy-To-Implement Variable-Ordering Heuristic," *Proc. ACM Great Lakes Symp. on VLSI (GLSVLSI)*, Washington, DC, April **2003**, pp. 116-119.

C32. (with S. N. Adya, M. Yildiz, P. G. Villarrubia, P. N. Parakh and P. H. Madden), "Benchmarking For Large-Scale Placement and Beyond", *Proc. ACM/IEEE Intl. Symp. on Physical Design (ISPD)*, Monterey, CA, April **2003**, pp. 95-103 (**invited**).

C31. (with K. N. Patel) "Error-Correction and Crosstalk Avoidance in DSM Busses," *Proc. System-Level Interconnect Prediction (SLIP)*, Monterey, CA, April **2003**, pp. 9-14.

C30. (with A. B. Kahng) "The Impact of Interoperability on CAD-IP Reuse: An Academic Viewpoint", in Proc. *Intl. Symp. on Quality Electronic Design (ISQED)*, San Jose, CA, March **2003** (**invited**), pp. 208-213.

C29. (with S. N. Adya) "Improving Min-cut Placement for VLSI Using Analytical Techniques," in *Proc. IBM Austin Center for Advanced Studies Conference (ACAS)*, Austin, TX, February **2003**, pp. 55-62.

C28. (with G. F. Viamontes, M. Rajagopalan and J. P. Hayes), "Gate-level Simulation of Quantum Circuits", *Proc. Asia and South-Pacific Design Automation Conf.*, Kitayushu, Japan, January **2003**, pp. 295-301.

C27. (with F. A. Aloul, A. Ramani and K. A. Sakallah), "Generic ILP versus Specialized 0-1 ILP: an Update" in Proc. *ACM/IEEE Intl. Conf. Comp.-Aided Design (ICCAD)*, San Jose, CA, November **2002**, pp. 450-457.

C26. (with V. V. Shende, A. K. Prasad and J. P. Hayes), "Reversible Logic Circuit Synthesis", in Proc. *ACM/IEEE Intl. Conf. Comp.-Aided Design (ICCAD)*, San Jose, CA, November **2002**, pp. 353-360.

C25. (with F. A. Aloul and K. A. Sakallah), "Efficient Gate and Input Ordering for Circuit-to-BDD Conversion", in Proc. *IEEE Intl. Conf. Computer Design (ICCD)*, Freiburg, Germany, September **2002**, pp. 64-69.

C24. (with G. F. Viamontes, M. Rajagopalan and J. P. Hayes), "High-Performance Simulation of Quantum Computation Using QuIDD", in Proc. *Quantum Communication, Measurement and Computation (QCMC)*, July 2002, **2003**, pp. 311-314.

C23. (with F. A. Aloul, A. Ramani and K. A. Sakallah), "Solving Difficult SAT Instances In The Presence of Symmetry", in Proc. *ACM/IEEE Design Automation Conf.*, June **2002**, pp. 731-736.

C22. (with S. N. Adya), "Consistent Placement of Macro-blocks Using Floorplanning and Standard-Cell Placement", Proc. *ACM/IEEE Intl. Symp. on Physical Design (ISPD)*, April **2002**, pp. 12-17.

C21. (with A. B. Kahng and S. Mantik), "Min-max Placement For Large-scale Timing Optimization", Proc. *ACM/IEEE Intl. Symp. on Physical Design*, April **2002**, pp. 143-148.

C20. (with A. B. Kahng), "Analytical Minimization of Signal Delays in VLSI Placement", in *Proc. IBM Austin Center for Advanced Studies (ACAS) Conference*, February **2002**, p. 62-68.

C19. (with F. A. Aloul and K. A. Sakallah), "Faster SAT and Smaller BDDs via Common Function Structure", in Proc. *ACM/IEEE Intl. Conf. on Computer-Aided Design*, **2001**, pp. 443-448.

C18. (with S. N. Adya), "Fixed-outline Floorplanning Through Better Local Search", in Proc. *IEEE Intl. Conf. on Computer Design (ICCD)*, **2001**, pp. 328-334.

C17. (with A. E. Caldwell et al.), "GTX: The MARCO GSRC Technology Extrapolation System", in Proc. *ACM/IEEE Design Automation Conf.*, June **2000**, pp. 693-698.

C16. (with A. E. Caldwell and A. B. Kahng), "Can Recursive Bisection Alone Produce Routable Placements?", in Proc. *ACM/IEEE Design Automation Conf.*, June **2000**, pp. 731-736.

C15. (with O. Coudert, C. Meinel and E. Sentovich), "Web-based frameworks to enable CAD RD", in Proc. *ACM/IEEE Design Automation Conf.*, Los Angeles, June **2000**, p. 711 (**invited**).

C14. (with A. A. Kennings), "Analytical Minimization of Half-Perimeter Wirelength", in Proc. *IEEE/ACM Asia and South Pacific Design Automation Conf.*, Japan, January **2000**, pp. 179-184 (**BPA nominee**).

C13. (with A. E. Caldwell and A. B. Kahng), "Improved Algorithms for Hypergraph Bipartitioning", in Proc. *IEEE/ACM Asia and South Pacific Design Automation Conf.*, Japan, Jan. **2000**, pp. 661-666.

C12. (with A. E. Caldwell, A. B. Kahng and A. A. Kennings), "Hypergraph Partitioning for VLSI CAD: Methodology for Heuristic Development, Experimentation and Reporting", in Proc. *ACM/IEEE Design Automation Conf.*, June **1999**, pp. 349-354.

C11. (with A. E. Caldwell and A. B. Kahng), "Hypergraph Partitioning With Fixed Vertices", in Proc. *ACM/IEEE Design Automation Conf.*, June **1999**, pp. 355-359.

C10. (with A. E. Caldwell and A. B. Kahng), "Optimal Partitioners and End-Case Placers for Standard-Cell Layout", in Proc. *ACM/IEEE Intl. Symp. on Physical Design*, April **1999**, pp. 90-96.

C9. (with C. J. Alpert, A. E. Caldwell and A. B. Kahng), "Partitioning With Terminals: A 'New' Problem and New Benchmarks", in Proc. *ACM/IEEE Intl. Symp. on Physical Design*, April **1999**, pp. 151-157.

C8. (with R. Baldick, A. B. Kahng and A. A. Kennings), "Function Smoothing with Applications to VLSI Layout", in Proc. *IEEE/ACM Asia and South Pacific Design Automation Conf.*, Hong Kong, Jan. **1999**, pp. 225-228 (**BPA nominee**).

C7. (with A. E. Caldwell and A. B. Kahng), "Relaxed Partitioning Balance Constraints in Top-Down Placement", in Proc. *IEEE Intl. ASIC Conference*, Rochester, September **1998**, pp. 229-232.

C6. (with A. B. Kahng et al.), "Watermarking Techniques for Intellectual Property Protection", in Proc. *ACM/IEEE Design Automation Conference*, San Francisco, June **1998**, pp. 776-781.

C5. (with A. B. Kahng et al.), "Robust IP Watermarking Methodologies for Physical Design", in *Proc. ACM/IEEE Design Automation Conference*, San Francisco, **1998**, pp. 782-787.

C4. (with A. E. Caldwell, A. B. Kahng, S. Mantik and A. Zelikovsky), "On Wirelength Estimations for Row-Based Placement", in *Proc. ACM/IEEE Intl. Symposium on Physical Design*, Monterey, April **1998**, pp. 4-11.

C3. (with A. E. Caldwell, A. B. Kahng and S. Mantik), "Implications of Area-Array I/O for Row-Based Placement Methodology", in *Proc. IEEE Symp. on IC/Package Design Integr.*, Santa Cruz, February **1998**, pp. 93-98.

C2. (with C. J. Alpert et al.), "Quadratic Placement Revisited", in *Proc. ACM/IEEE Design Automation Conference* (**BPA nominee**), Anaheim, June **1997**, pp. 752-757.

C1. (with C. J. Alpert et al.), "Faster Minimization of Linear Wirelength for Global Placement", in *Proc. ACM/IEEE Intl. Symp. on Physical Design*, Napa, April **1997**, pp. 4-11.